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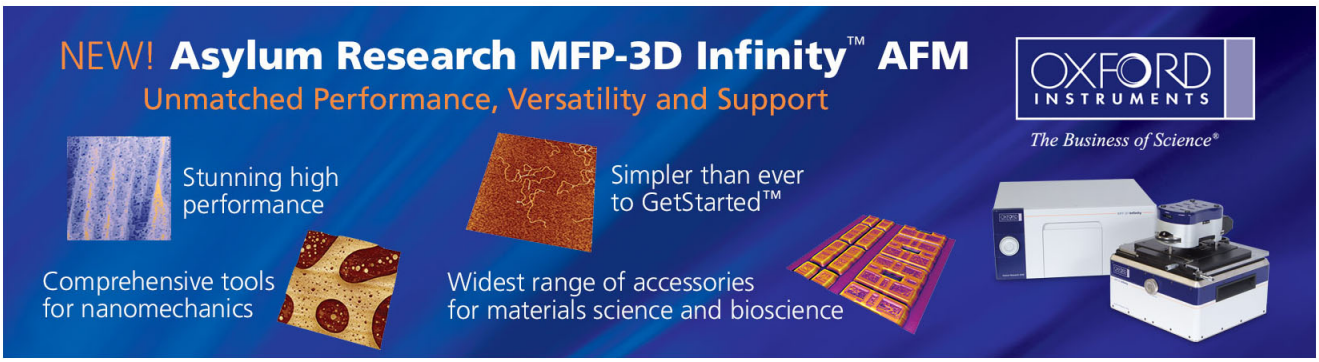

Low voltage lead titanate/Si one-transistor ferroelectric memory with good device characteristics

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We have developed one-transistor ferroelectric memory using lead titanate (PTO) as a gate dielectric directly formed on Si without any buffer layer. The PTO/Si metal–oxide–semiconductor field-effect transistor memory has shown a large threshold voltage shift of 1.6 V at only ±4 V program/erase voltages. The corresponding good interface was achieved by lowering the anneal temperature to 450 °C. Besides the sharp capacitance change of 0.17 μF/V cm^2, it was also evidenced by the high mobility of 169 cm^2/V s close to high-κ HfO_2. In addition, long retention $>$1000 s and endurance $>10^{11}$ stress cycles in the device suggested good memory characteristics. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1814440]

Among various memory devices, ferroelectric memories are particularly remarkable due to the unique nonvolatile behavior, good scale down potential, and fast switching time. Currently, high capacity (>1 Mbyte) ferroelectric RAM has been demonstrated in the cell configuration consisting of one-transistor (1T) and one-capacitor. But in order to further scale down the cell size, it is necessary to integrate the ferroelectric materials in the 1T ferroelectric metal–oxide–semiconductor field-effect transistor (FeMOSFET).[1–9] However, the strong interface reaction between ferroelectric materials and Si remained the major technology obstacle for this 1T memory in the last decade.[3] Recently, the adoption of a buffer gate dielectric between ferroelectric materials and Si shed a light to overcome the interdiffusion problem as a result of the inevitable high anneal temperature of ferroelectrics.[4–8] For example, using Al_2O_3 as the good dielectric and diffusion barrier,[10,11] we have achieved the record large ferroelectric memory window of 13 V in this kind of stack gate structure.[8] Unfortunately, the relatively large writing voltage was usually required owing to the voltage drop on the Al_2O_3 dielectric so as to hinder the widely industrial applications. On the other hand, although the low temperature process has already been demonstrated in the organic permanent memory transistor, it still requires relatively high operation voltage caused by thick gate insulator.[9] Besides the good threshold voltage shift (ΔV_T) at a low writing voltage, the high carrier mobility is also requested in mainstream MOSFET technology.[12] Therefore, it is really challenging to develop a next-generation low voltage 1T FeMOSFET memory.

It has been reported that $Pb(Zr,Ti)O_3$ solid solution with higher Ti fraction would need a lower anneal temperature. Supposedly, this low anneal temperature should be helpful to prevent the formation of interfacial layer,[13] which is essential to decrease the programming voltage in the low voltage operation. To study this effect, we have calculated the electric field (E_{ferro}) in the ferroelectric material:

$$E_{ferro} = V_g / \left(d_{ferro} + \frac{\varepsilon_{ferro}}{\varepsilon_{interface}} d_{interface} \right). \quad (1)$$

The E_{ferro}, ε_{ferro}, and d_{ferro} are the electric field, dielectric constant, and thickness in ferroelectric layer, where the $\varepsilon_{interface}$ and $d_{interface}$ are the dielectric constant, and thickness in interfacial layer. Because the ΔV_T is from ferroelectric polarization, a larger E_{ferro} is desired. Thus, decreased $d_{interface}$ and ε_{ferro} are the solution to increase the desired E_{ferro}. This can be also obtained by lowering the anneal temperature of lead titanate (PTO) simultaneously though the ferroelectric property of PTO may be degraded by trading off the E_{ferro}. Thus in this letter we investigated lead titanate as a ferroelectric gate material directly grown on Si substrates with the low temperature annealing. Particularly, while the anneal temperature could be lowered down to 450 °C, it indicates the potential application for embedded memories and could also help terminate the contamination to integrated circuit.

P-type 4 in. Si wafers with a resistivity of approximately 10 Ω cm were used in this study. After device isolation and source–drain n^+ region definition, the around 90-nm-thick PTO layer was deposited by spin coating, dried at 90 °C for 30 s, and annealed at 450 °C. The entire process details were

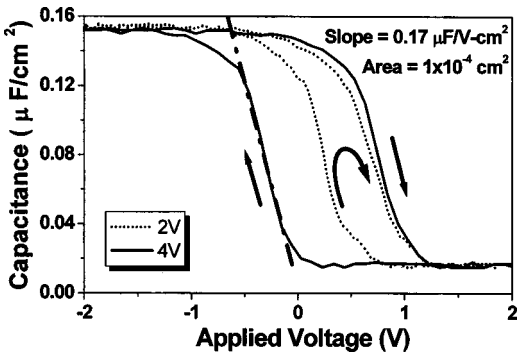

FIG. 1. 1 MHz *C–V* characteristics of PTO/Si FeMOS capacitor. The capacitor size is 10^{-4} cm^2 and the gate length of the FeMOSFET is 10 μm.

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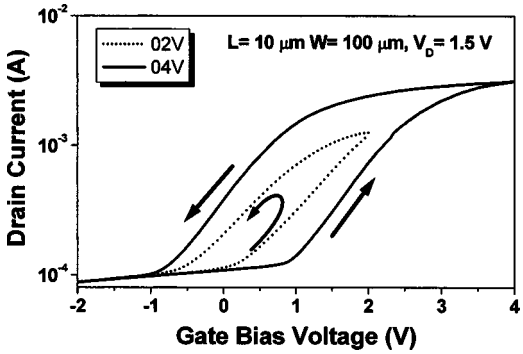


FIG. 2. I_D–V_G characteristics of PTO/Si FeMOSFETs. The capacitor size is 10^{-4} cm^2 and the gate length of the FeMOSFET is 10 μm.

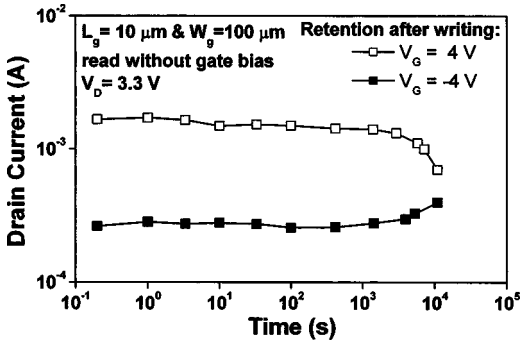


FIG. 4. The measured retention characteristics of the PTO/Si memory at ±4 V writing voltages.

described in our previous reports.[5–7] HF-vapor passivation[10,11] was used to suppress the native oxide formation before PTO formation. Finally, Al electrodes were formed and the device size was 10 μm$\times$100 μm. The device performance was characterized by capacitance–voltage (C–V) and current–voltage (I–V) measurements.

Figures 1 and 2 show the device memory characteristics measured from 1MHz C–V of FeMOS capacitor and drain current–gate bias voltage (I_D–V_G) characteristics of FeMOSFET, respectively. The very high I_D in Fig. 2 is due to high-κ property of PTO that is important for VLSI scaling down.[10–13] The ferroelectric characteristics are evidenced from the clockwise C–V hysteresis loops and counterclockwise I_D–V_G hysteresis loops, as shown by arrows. For a low ±4 V program and erase voltage, a memory window of 1.6 V is obtained from both the flatband voltage shift in C–V curves. Additionally, the ΔV_T change in I_D–V_G characteristics indicates the excellent memory device performance. The possible reason for such low writing voltage is because the gate voltage is directly applied on the ferroelectric material instead of generating the voltage drop on the interfacial layer or inserted dielectric diffusion barrier.[8] Although the PTO annealed at low temperature could have a relatively poor crystallinity or small permanent polarization, from the device point-of-view, avoiding the interfacial oxide layer is much more important than the crystal structure because a small polarization of ferroelectrics is still enough for memory operation.[4] The excellent device characteristics can also be evidenced by the very sharp capacitance change ($\Delta C/\Delta V$) of 0.17 μF/V cm^2, implying very sensitive ferroelectric domain switching under voltage sweeping.

To further study the interface quality, we have measured the effective mobility of the 1T PTO/Si FeMOSFET. Figure 3 shows the effective mobility (μ_{eff}) dependence on effective electric field (E_{eff}) obtained from the I_D–V_G measurements. The effective mobility peak of 169 cm^2/V s is obtained, which is comparable to the best data in high-κ HfO_2 MOSFET.[12] This high mobility indicates that good interface between PTO and Si can be achieved at such low anneal temperature. It is noteworthy that the extraordinary high-κ and high mobility nature would play a crucial role for further device scaling down into the sub-0.1 μm range.

In the roadmap of nonvolatile memories, data retention is another important factor. Figure 4 displays the time-dependent current changes and retention characteristics of the PTO/Si memory. The open and closed data points represent the drain currents after applying program/erase voltage of ±4 V to gate. As shown in Fig. 4, it can be observed that the drain currents do not significantly fall down or go up-

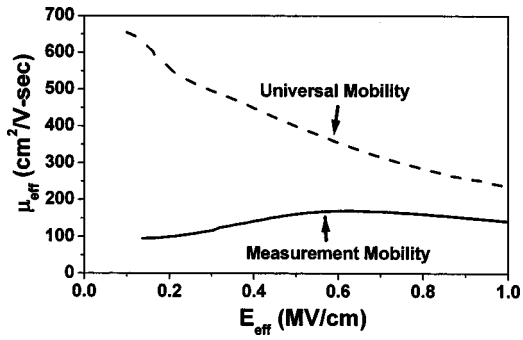
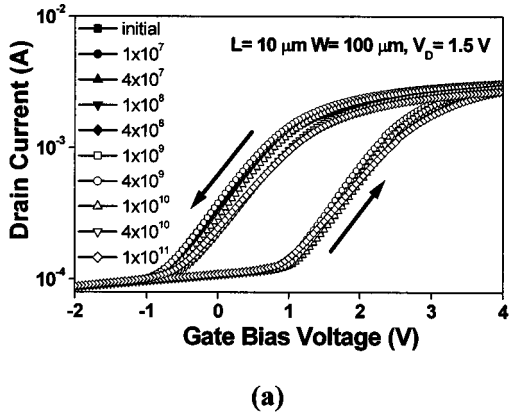


FIG. 3. The effective mobility of the low temperature formed PTO/Si FeMOSFETs.



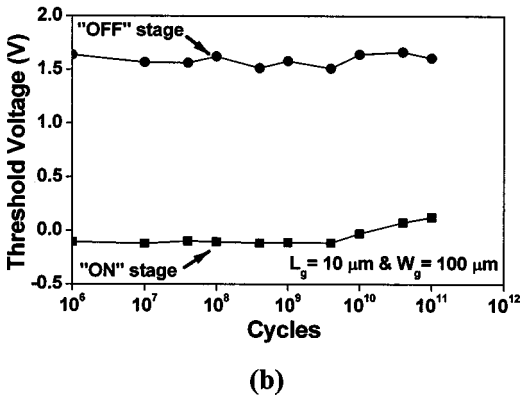


FIG. 5. (a) The endurance characteristics and (b) threshold voltage changes of PTO/Si FeMOSFETs after 1 MHz±4 V writing with different stress cycles.

ward within the time range of 1000 s. Consequently, a retention time of >1000 s can be claimed from the time-independent current values. The good retention could also support the absence of the interfacial layer that not only behaves as a series capacitor but also generates a depolarization field.

We have further done the measurement of the endurance of 1T PTO/Si memory. Figures 5(a) and 5(b) illustrate the endurance characteristics in I_D–V_G and ΔV_T of PTO/Si memory, respectively. The ON and OFF states in V_T before and after stress are determined from the I_D–V_G hysteresis loops under the stress condition of ±4 V at 1 MHz. As shown in Fig. 5(a), the nearly identical I_D–V_G curves after repeated cycling are in agreement with the good endurance $>10^{11}$ cycles in Fig. 5(b). This good endurance is attributed to the fact that the low program/erase electric fields could generate the relatively small amount of defects in the PTO/Si memory structure.

In conclusion, a ferroelectric PTO/Si 1T memory with large memory window, high mobility, sharp capacitance change, and good endurance has been demonstrated. Unlike using the buffer layer in stack gate structure, the low temperature annealing for the single-layer ferroelectric gate has been proved to be extremely essential in preventing the formation of an interfacial layer. The good memory characteristics in this FeMOSFET show the technical potential for next-generation memory application.

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