# A New CMOS Pixel Structure for Low-Dark-Current and Large-Array-Size Still Imager Applications

Yu-Chuan Shih, *Student Member, IEEE,* and Chung-Yu Wu, *Fellow, IEEE*

***Abstract*—A new pixel structure for still CMOS imager application called the psedoactive pixel sensor (PAPS) is proposed and analyzed in this paper. It has the advantages of a low dark current, high signal-to-noise ratio, and a high fill factor over the conventional passive pixel sensor imager or active pixel sensor imager. The readout circuit called the zero-bias column buffer-direct-injection structure is also proposed to suppress both the dark current of the photodiode and the leakage current of row switches by keeping both biases of photodiode and the parasitic p-n junction in the column bus at or near zero voltage. The improved double delta sampling circuits are also used to suppress fixed pattern noise, clock feedthrough noise, and channel charge injection. An experimental chip of the proposed PAPS CMOS imager with the format of 352 $\times$ 288 (CIF) has been fabricated by using a 0.25-$\mu$m single-poly-five-level-metal (1P5M) n-well CMOS process. The pixel size is 5.8 $\mu$m $\times$ 5.8 $\mu$m. The pixel readout speed is from 100 kHz to 10 MHz, corresponding to the maximum frame rate above 30 frames/s. The proposed still CMOS imager has a fill factor of 58%, chip size of 3660 $\mu$m $\times$ 3500 $\mu$m, and power dissipation of 24 mW under the power supply of 3.3 V. The experimental chip has successfully demonstrated the function of the proposed new PAPS structure. It can be applied in the design of large-array-size still CMOS imager systems with a low dark current and high resolution.**

***Index Terms*—CMOS images, dark current, pseudoactive pixel sensor (PAPS), readout circuit.**

## I. Introduction

RECENTLY, CMOS imagers, which integrate photosensors, optics, analog readout circuits [1]–[4], digital control systems, and intelligent signal processing circuits [5], [6] on a single chip have become increasingly attractive due to their low cost [1], low voltage [7], [8], and low power consumption [9]. Such CMOS imager chips have great potential in various applications, including cameras, medical examination, military systems, and other strategic or security equipments. With the rapid scaling down of CMOS technology, the design of multimillion-pixel and high-quality CMOS imagers [10], [11] with performance approaching that of charge couple device (CCD) imagers has become more and more challenging. Generally, small pixel size, low dark current, and high fill factor are required in the design of high-resolution and high-quality CMOS imagers.

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The authors are with the Nanoelectronics and Gigascale Systems Laboratory, Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: m8511619@alab.ee.nctu.edu.tw; cywu@alab.ee.nctu.edu.tw).

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Temporal noise sets the fundamental limit on image sensor performance at room temperature [12]. The dominant source of temporal noise in high illumination is the shot noise that is proportional to the sum of photocurrent and dark current in a photodiode [12]. A large dark current in the photodiode array of a CMOS imager could lead to high noise, low signal-to-noise ratio (SNR), nonuniformity, low scalability, and reduced dynamic range. Therefore, reducing the dark current in the photodiode also eliminates the temporal noise in CMOS imager at room temperature.

The dark current is dominantly generated from the reverse-biased photodiode and parasitic pn junctions in the pixel. Generally, higher (lower) reverse-biased voltage leads to larger (smaller) dark current. In the conventional active pixel sensor (APS) [1], [10], [11], the dark current is dominantly generated from the photodiode, which is different in every pixel due to the different reverse-biased voltages of photodiodes when the incident light on every pixel is not the same. Thus, the effect of the dark current cannot be reduced even under the use of dummy photodiode in the pixel. In the passive pixel sensor (PPS) [1], the dark current is generated from both the photodiode and the parasitic p-n junction in the column bus. The two effects are also different in every pixel during the signal readout operation.

Several techniques have been proposed to cancel the dark current such as the differential passive pixel imager with fixed pattern noise (FPN) reduction [13] and the phototransistor pixel sensor with dark current cancellation [14]. The differential passive pixel imager still cannot effectively reduce the dark current due to the mismatch between the photodiode in the photodiode array and that in the dummy shielded pixel. The structure of phototransistor pixel sensor with dark current cancellation contains one dummy shielded photodiode in each pixel [14]. The total dark current still cannot be effectively cancelled because the reverse-biased voltage of the photodiode differs from that of the dummy shielded photodiode. In addition, the large pixel size in this structure degrades the image resolution and increases cost.

The fill factor is another parameter considered in the design of the high-resolution and large-array-size CMOS imager. A high fill factor could lead to a high spectral sensitivity under the same pixel size. In other words, the pixel must be composed of devices as few as possible. Among the APS CMOS imagers, the pixel structure composed of one photodiode and three MOSFETs cannot be effectively shrunk to satisfy the requirements of small pixels with the advancement of CMOS technology because most of the pixel area is filled by the three MOSFETs and the contacts for connections. In the conventional PPS CMOS imager, there is one MOSFET and one photodiode. Although the fill factor is high, the noise from the capacitive column bus is large [1]. In addition, the passive pixel cannot be shrunk too

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small and the array size cannot be too large because the small capacitance of photodiode and the large capacitance of column bus will result in high readout noise [1].

Several other pixel structures for the design of large-array-size CMOS imager such as the differential passive pixel imager [13] and the imager with pixel-level analog–digital converter (ADC) [15] have been proposed to reduce pixel area and maintain high performance. However, the effect of dark current is still the problem to be solved.

It is the aim of this paper to propose a new pixel structure called the psedoactive pixel sensor (PAPS) for the large-array-size still CMOS imagers with low dark current and high fill factor [4]. A new readout circuit is also proposed to readout the sensor current to the column bus and performs the outside-pixel integration using the APS-like structure. The new readout circuit keeps the biases of both photodiode and parasitic pn junctions in the column bus at or near zero bias to achieve low dark current, low column leakage current, and high linearity. The improved double delta sampling (DDS) circuit is used to reduce FPN, clock feedthrough noise, and the noise from the effect of channel charge injection. From the experimental results, it has been shown that the proposed new pixel structure and readout circuit can be applied to the design of low-dark-current and large-array-size still CMOS imagers.

The rest of this paper is organized as follows. In Section II, the new structure of the proposed PAPS is described and the principles to reduce dark current and increase fill factor are presented. The operation of improved DDS circuits is also described. In Section III, the chip architecture is described. In Section IV, the simulation results, chip layout, and experimental results are presented, analyzed, and compared to verify the advantageous performance of the proposed new pixel structure and readout circuit. Finally, the conclusion is given.

## II. Pixel Structure and Readout Circuits

### *A. PAPS Structure*

The proposed PAPS structure is shown in Fig. 1. The pixel structure is composed of one photodiode and one row select switch. The integration capacitor and source follower in the APS structure are moved out of the pixel. The cathode of the photodiode is connected to the pixel bias voltage $V_{\rm pix}$, whereas the anode is connected to the column bus through the select switch. The column bus biased at $V_{\rm com}$ which is nearly the same as $V_{\rm pix}$. Thus, the effective voltage drop across the pixel is zero or nearly zero. This structure is the same as that of the PPS, but the pixel voltage drop is kept at zero. Moreover, the readout operation is different from that of the conventional PPS structure, as will be described later.

In order to achieve a small pixel size, only a single type of MOSFET is used as the select switch within the pixel. As shown in Fig. 1, the pMOSFET is selected as the row switch in the pixel because the voltage at the n-well of the pMOSFET can be connected to the positive voltage $V_{\rm pix}$ to keep both source and drain junctions at the bias voltage of 0 V. Furthermore, to achieve the antiblooming effect, the p+-diffusion/n-well junction is used as the photodiode to ensure that the excess charges generated by strong incident light can be drained away by the vertical substrate p-n-p bipolar-junction transistor (BJT)[2]. This prevents

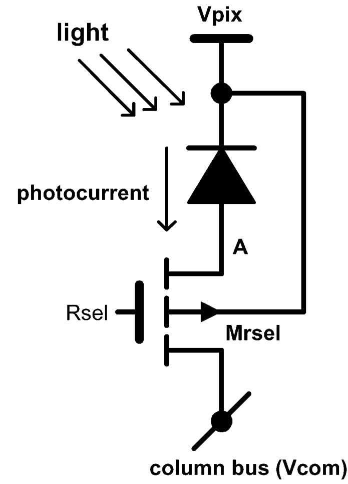


Fig. 1. Circuit of PAPS.

the excess charges from leaking to the neighboring pixels or directly to the column bus. The p+-diffusion of the photodiode can be connected to the source of $M_{\rm rsel}$ to increase the fill factor.

In the n-well CMOS technology, the p+/n-well p-n junction is used as the photodiode. In a test chip, 10 000 photodiodes are connected in parallel to form a photodiode array. The current-to-voltage (*I–V*) characteristics of a single photodiode can be obtained by dividing the measured total current by 10 000. The measured dark current $I_d$ of the photodiode shielded from light and the measured photocurrent $I_p$ of the photodiode generated under the light of 20-mW bulb are shown in Fig. 2(a) and (b), respectively. As shown in Fig. 2(a), the dark current is increased with the reverse-biased voltage $V_R$ because higher electric field is generated in the pn junction depletion region when the reverse-biased voltage is higher. For the same reasons, the photocurrent is also increased with the reverse-biased voltage.

In Fig. 2(a), the dark current $I_d$ of the photodiode approaches zero when the reverse-biased voltage $V_R$ is decreased toward zero. However, the photocurrent of $I_{p1}$ at the reverse-biased voltage of 0 V is not much smaller than that of $I_{p2}$ at the reverse-biased voltage of 3 V as shown in Fig. 2(b). The measured values of $I_{d1}, I_{d2}, I_{p1}, I_{p2}, I_{p1}/I_{d1}$, and $I_{p2}/I_{d2}$ are listed in Table I. From the measurement results, it is found that the ratio of the photocurrent $I_{p1}$ to the dark current $I_{d1}$ at the reverse bias of 0 V is much larger than $I_{p2}/I_{d2}$ at the reverse bias of 3 V. Generally, the p-n junction photodiode has the characteristic as

$$\frac{I_p}{I_d}\bigg|_{|V_R|=0} > \frac{I_p}{I_d}\bigg|_{|V_R|>0}. \tag{1}$$

Thus, biasing the photodiode at or near zero voltage can achieve lower dark current, lower shot noise [12], and higher SNR as compared with that at higher reverse-biased voltage.

From the above results, it is shown that both photodiode and all the parasitic pn junctions in the row select switches must be operated at the reverse bias of 0 V to effectively reduce the dark current. Thus, the voltage difference between the cathode of the photodiode and the column bus is operated at 0 V in the proposed PAPS structure in order to maintain the zero bias of both photodiode and parasitic pn junctions as shown in Fig. 1. When the row select switch of $M_{\rm rsel}$ is on, the voltage at the source of

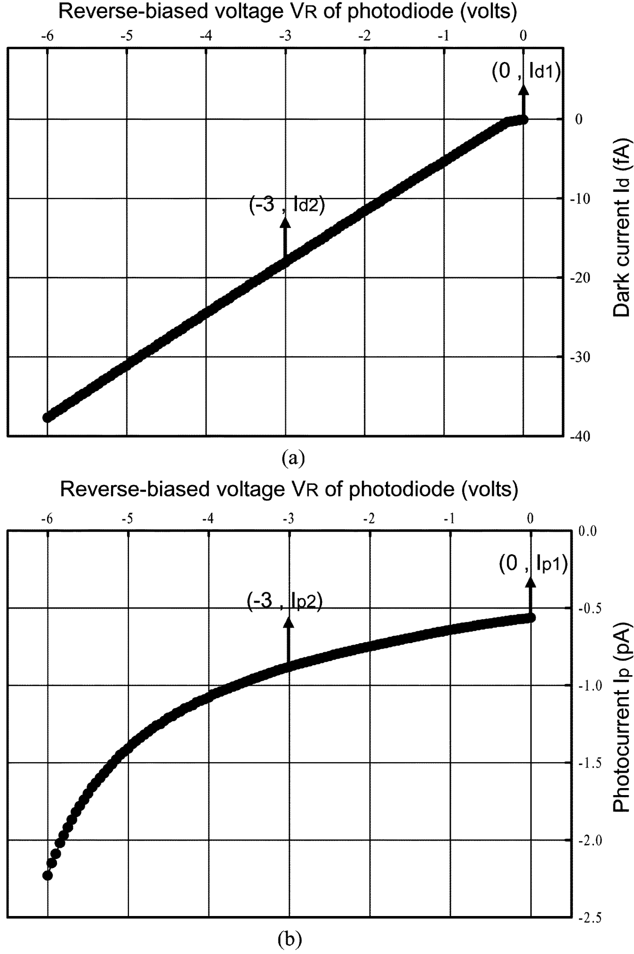


Fig. 2. Measured (a) dark current $I_d$ and (b) photocurrent $I_p$ of the fabricated p+/n-well photodiode.

TABLE I
VALUES OF $I_{d1}, I_{d2}, I_{p1}, I_{p2}, I_{p1}/I_{d1}$, AND $I_{p2}/I_{d2}$

| | |
|---|---|
| Id1 | 0.13 fA |
| Id2 | 18.10 fA |
| Ip1 | 570 fA |
| Ip2 | 880 fA |
| Ip1/Id1 | 4384.61 |
| Ip2/Id2 | 48.62 |

$M_{\rm rsel}$ is the same as that of the column bus which is $V_{\rm pix}$. The photodiode, the parasitic pn junction between the source and the substrate of $M_{\rm rsel}$, and the parasitic p-n junction between the drain and the substrate of $M_{\rm rsel}$ are all operated at the reverse-biased voltage of 0 V. The photocurrent is then delivered to the column bus for charge integration while both dark current of the photodiode and leakage current of the parasitic pn junctions are decreased to near 0 A.

When the row select switch of $M_{\rm rsel}$ is turned off by setting the signal of $R_{\rm sel}$ at $V_{\rm dd}$, the circuit diagram of PAPS is shown in Fig. 3. In Fig. 3, the source of $M_{\rm rsel}$, n-well, and the drain of $M_{\rm rsel}$ form the parasitic lateral p-n-p BJT device Q1 with base and collector connected to $V_{\rm pix}$ and $V_{\rm com}$, respectively, and the emitter connected to node A. The source of $M_{\rm rsel}$, n-well, and p-substrate form the parasitic vertical p-n-p BJT device Q2 with the p-substrate collector connected to ground. Under incident light, the photodiode is forward-biased with the voltage drop equal to VF and operated as a solar cell. Thus the current of $I_F$ is expressed as [16]

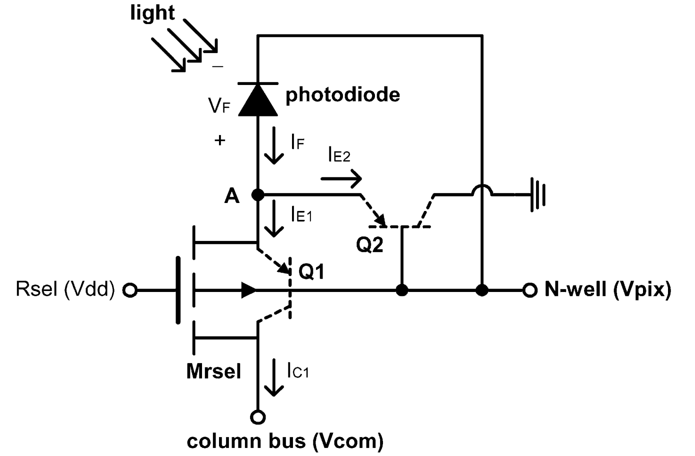


Fig. 3. Circuit diagram of PAPS when the row select switch of $M_{\rm rsel}$ is off.

$$I_F = I_p0 - I_{\rm SP}\left(e^{\frac{V_F}{V_T}} - 1\right) \tag{2}$$

where $I_{\rm SP}$ is the reverse saturation current of photodiode, $I_{p0}$ is the photocurrent when the photodiode is biased at 0 V, and $V_T$ is the voltage equivalent of temperature. With $V_F$ as the forward substrate bias between source and body of $M_{\rm rsel}$, the threshold voltage $V_{\rm tp}$ of $M_{\rm rsel}$ is decreased due to the body effect. But the row select switch device $M_{\rm rsel}$ is still kept off because the voltage at the node $A$, which is $V_{\rm pix} + V_F$, is smaller than $V_{\rm dd} + V_{\rm tp}$. However, the collector current $I_{C1}$ of Q1 flows into the column bus as the dark current. As shown in Fig. 3, the current of $I_F$ in the photodiode is equal to the sum of the emitter current $I_{e1}$ of Q1 and $I_{e2}$ of Q2. Furthermore, both of the parasitic lateral p-n-p BJT device Q1 and parasitic vertical p-n-p BJT device Q2 are operated in the forward-active region because their emitter-base junctions are forward-biased and collector-base junctions are reverse-biased. From the simplification of Ebers-Moll current equation, we have

$$\begin{aligned} I_F &= I_{p0} - I_{\rm SP}\left(e^{\frac{V_F}{V_T}} - 1\right) \\ &= I_{e1} + I_{e2} \\ &= I_{S1}\left(e^{\frac{V_F}{V_T}} - 1\right) + I_{S2}\left(e^{\frac{V_F}{V_T}} - 1\right) \end{aligned} \tag{3}$$

where $I_{S1}$ and $I_{S2}$ are the reverse saturation current of parasitic lateral BJT device Q1 and parasitic vertical BJT device Q2, respectively. From (3), the total equivalent dark current $I_{\rm TED}$ from the parasitic BJT device Q1 flowing into the column bus can be expressed as

$$\begin{aligned} I_{\rm TED} &= (N_p - 1)I_{C1} \\ &= (N_p - 1)\alpha I_{e1} \\ &= (N_p - 1)\alpha I_{p0}\frac{I_{S1}}{I_{\rm SP} + I_{S1} + I_{S2}} \\ &= 2.107 \times 10^{-5} \times (N_p - 1)I_{p0} \end{aligned} \tag{4}$$

TABLE II
VALUES OF $I_{\rm sp}, I_{s1}, I_{s2}, \alpha$, AND WIDTH/LENGTH OF MRSEL

| | |
|---|---|
| $I_{SP}$ | $1.97\times10^{-17}$ A |
| $I_{S1}$ | $4.20\times10^{-22}$ A |
| $I_{S2}$ | $3.02\times10^{-20}$ A |
| $\alpha$ | 0.99 |
| width/length of Mrsel | 0.5 μm / 0.35 μm |

Fig. 4. ZCBDI readout circuit with the $P+/N$-well photodiode.

where $N_p$ is the number of pixels connected to the same column and $\alpha$ is the common-base current gain of Q1.

The values of $I_{\rm SP}, I_{S1}, I_{S2}$, and $\alpha$ in the proposed PAPS CMOS imager with 0.25-$\mu$m CMOS technology and channel width (length) of $M_{\rm rsel}$ are given in Table II. From (4), the ratio of $I_{p0}/I_{\rm TED}$ is larger than that of APS CMOS imager if $N_p$ is smaller than 2000. Thus, the dark current contributed by the current $I_{\rm TED}$ in the proposed PAPS CMOS imager is smaller than the dark current of APS CMOS imager if $N_p$ is smaller than 2000 which is equivalent to a 4M-pixel imager if a square pixel array is used. Thus, the proposed PAPS CMOS imager can be applied to the large-array-size imager with the dark current contributed by $I_{\rm TED}$ in (4) smaller than the dark current of APS CMOS imager.

The value of $I_{S1}$ can be decreased by increasing the channel length of $M_{\rm rsel}$. A lower $I_{S1}$ leads to a larger ratio of $I_{p0}/I_{\rm TED}$ in (4) and thus larger of $N_p$. However, the fill factor is decreased to about 54% if the channel length of $M_{\rm rsel}$ is 0.7-$\mu$m. This fill factor is still larger than that of the APS CMOS imager.

### *B. ZCBDI Structure*

Fig. 4 shows the PAPS pixel and the column readout circuit called the zero-bias column buffer-direct-injection (ZCBDI) structure with the p+/n-well photodiode. The bias voltage $V_{\rm pix}$ in the pixel is maintained at 1.8 V. On the left-hand side of the pixel circuit, all the deselected pMOSFETs as the row select switches in the same column are added to include their leakage currents to the column bus. For a $352\times288$ (CIF) imager, the total number of deselected pMOSFETs is 287. The common n-well of all selected and deselected pMOS row switches is connected to 1.8 V to maintain zero reverse bias in the source/drain p-n junctions. Thus the total column leakage current due to the deselected pMOS switches can be reduced to a very low level.

The column readout circuit is composed of the BDI [17], [18] readout structure, the nMOS transistor $M_{\rm rst}$ as the reset switch, the APS-like structure with the pMOS source follower $M_{p1}$ and $M_{p2}$, and an optional integration capacitor Cint with a switch. In the BDI readout structure, the inverting input of a gain stage with gain $A$ is connected to the column bus and the noninverting input is connected to the bias voltage $V_{\rm com}$. The output of the gain stage is connected to the gate of $M_{\rm in}$ as a common-gate input stage. The gain stage is implemented by a CMOS differential pair to reduce the chip area. Through the BDI circuit, the bias of column bus is controlled by the input voltage $V_{\rm com}$ of the differential pair. The value of $V_{\rm com}$ is set to be 1.8 V by a low-noise constant voltage source to maintain the voltage of column bus at or near 1.8 V. The additional power consumption of the differential pair in each column readout circuit can be reduced by proper design of gain stage with low bias current. The ZCBDI readout structure is similar to the readout circuit used in infrared focal plane array to obtain stable zero detector bias [19].

In addition, to maintain the stable bias at the column bus, the input impedance in the BDI readout structure is decreased by a factor of $A$ due to the negative-feedback structure. The injection current from the pixel is mainly drained toward the column bus due to the low input impedance. The current injection efficiency of the BDI readout structure which is the current ratio between $I_{\rm in}$ and $I_r$ in Fig. 4 is expressed as [19], [20]

$$\eta(s)=\frac{(1+A)g_mR_o}{1+(1+A)g_mR_o}\left(\frac{1}{1+s/2\pi F_{\rm BW}}\right) \quad (5)$$

$$F_{\rm BW}=\frac{1+(1+A)g_mR_o}{2\pi R_oC_T} \quad (6)$$

where $A$ is the gain of the buffer, $g_m$ is the transconductance of $M_{\rm in}$, $C_T$ is the capacitance at the column bus, and $R_o$ is the output resistance of $M_{\rm rsel}$. From (5), the current injection efficiency is increased by the gain of the buffer. In this design, the gain of $A$ is about 100, which makes the injection efficiency close to 1.

Both the photocurrent from the selected pixel and the leakage current from the deselected pixels are injected into the integration capacitance through the BDI readout structure. However, from (4), the ratio between the photocurrent $I_{p0}$ from the selected pixel and the total equivalent dark current $I_{\rm TED}$ from the deselected pixels is large if the number of pixels connected to the same column is small. Thus, the current from the deselected pixels is negligibly small as compared with the photocurrent from the selected pixel due to the zero or near zero bias in parasitic p-n junctions. The integration capacitance is composed of the gate capacitance of $M_{p1}$ and the optional capacitance of $C_{\rm int}$ with a switch. The optional capacitor of $C_{\rm int}$ is used to prevent saturation when the incident light is strong and the integration time is long such as the application of still imager in the environment of strong light. This leads to increase the dynamic range of the incident light. In this design, the value of $C_{\rm int}$ is designed as 0.2 pF, which only occupies small area of the total chip.

The photocurrent generated from the selected pixel is integrated on the integration capacitor after the reset operation when

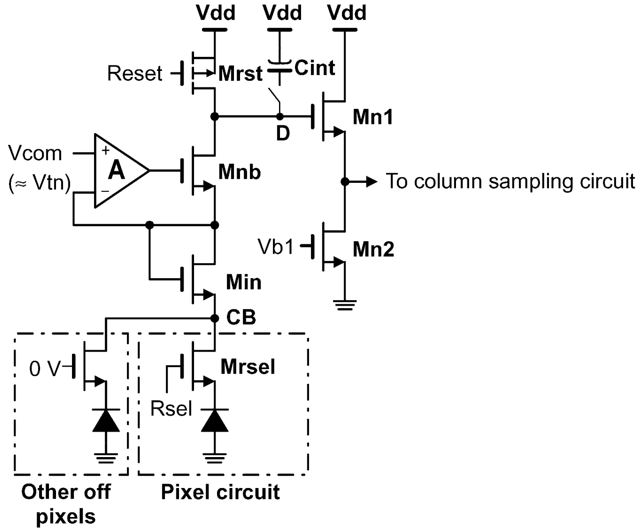


Fig. 5. Modified ZCBDI readout circuit with the $N+/P$-substrate photodiode.

$M_{\rm rst}$ is open. After the integration, the integrated voltage is transferred through the source follower composed of $M_{p1}$ and $M_{p2}$. The reset switch and the source-follower form an APS-like structure to integrate the photocurrent outside the pixel. At the end of the integration, the reset switch $M_{\rm rst}$ is turned on and the voltage at the integrating capacitor is also transferred through the source follower to perform the operation of DDS.

The source follower is composed of the two pMOSFETs of $M_{p1}$ and $M_{p2}$ with their n-well substrates connected to the sources as shown in Fig. 4. Thus, the gain of the source follower can be designed to be nearly 1 without the gain loss due to the body effect. The output of the source follower is connected to column sampling circuits in the next stage of DDS operation circuit.

The ZCBDI readout circuit can be modified for the applications to the n+/p-substrate photodiode which has lower dark current and higher quantum efficiency. The modified ZCBDI readout circuit for the n+/p-substrate photodiode is shown in Fig. 5 where an extra nMOS device $M_{\rm in}$ is added. In Fig. 5, the modified ZCBDI readout circuit is composed of the BDI [17], [18] readout structure, the pMOS transistor $M_{\rm rst}$ as the reset switch, the APS-like structure with the nMOS source follower $M_{n1}$ and $M_{n2}$, and an optional integration capacitor $C_{\rm int}$ with a switch. The value of $V_{\rm com}$ is set to be slightly larger than the threshold voltage $V_{\rm tn}$ of $M_{\rm in}$. Thus the bias at the column bus of node CB is equal to near zero voltage. The photodiode is biased at zero or near zero voltage when the row select switch of $M_{\rm rsel}$ is on. The impedance seen from the node of CB to $V_{\rm dd}$ is increased by $(1/g_{\rm min})$ where $g_{\rm min}$ is the transconductance of $M_{\rm in}$. To avoid the degraded injection efficiency, the channel geometric ratio $W/L$ of $M_{\rm in}$ should be large enough to increase $g_{\rm min}$.

### C. Improved DDS Operation Circuit

The improved DDS operation circuit is shown in Fig. 6. The column sampling circuit is used in each column whereas the output correlated double sampling (CDS) circuit is shared by all the columns. In the column sampling circuit as shown in Fig. 6, the nMOS devices of $MS$ and $MR$ controlled by the signals of SHS and SHR, respectively, are sampling switches whereas $M_{\rm vce}$ controlled by $V_{\rm ce}$ is the equalization switch. The signals generated by the integration of photocurrent and the reset signal transferred through the source follower $M_{p1}/M_{p2}$ are sampled by the two nMOS devices of $MS$ and $MR$, respectively. Both the effects of clock feedthrough and channel charge injection resulted from the sampling operation of $MS$ and $MR$ in the original DDS circuit [21] will degrade the performance of signal readout. In the improved DDS circuit of Fig. 6, the effect of signal-dependent channel charge injection caused by $MS$ and $MR$ during the falling edges of SHS and SHR is reduced by the two added dummy nMOS devices $Ma$ and $Mb$ with their drain and source connected together and their gates connected to the outputs of the two inverters invA and invB, respectively. The size of $Ma$ and $Mb$ is designed to be about one half of the size of $MS$ and $MR$, respectively, because only the channel charges injected to the source regions of $MS$ and $MR$ are to be compensated by those to both drain and source regions of $MS$ and $MR$, respectively.

The signals after the sampling are held at the nodes of $A$ and $B$ until they are readout to the output CDS circuit when the column switches $M_{n1}$ and $M_{n3}$ are on. Since the column readout sampling is performed simultaneously in each column and the sampled column signals are readout to the output CDS circuit successively, the signal from the last column is held for the longest time that is almost equal to the integration time of the photocurrent. The held signal voltages at the last column will be decreased by the leakage currents at the nodes of $A$ and $B$. An extra capacitor of 0.12 pF is added to the nodes of $A$ and $B$ to avoid the held voltage level from decreasing lower than 1 LSB of the output analog-to-digital converter. The extra capacitor of 0.12 pF is determined by the leakage current Ileak at the nodes of $A$ and $B$, the gain $G_{\rm PGA}$ of the programmable gain amplifier (PGA) before the ADC, the node capacitances at the nodes of $A$ and $B$ $C_{\rm hold}$, and the integration time of photocurrent $T_{\rm int}$. The equation can be represented as

$$(C_{\rm hold} + 0.12\, pF)V_{\rm 1LSB} = G_{\rm PGA}(I_{\rm leak} \times T_{\rm int}). \quad (7)$$

The values of $C_{\rm hold}$ and $I_{\rm leak}$ are determined from the process parameter. All the values of $C_{\rm hold}, V_{\rm 1LSB}, G_{\rm PGA}, I_{\rm leak}$, and $T_{\rm int}$ are summarized in Table III.

The photosignal (reset) voltage is sampled to the gate of $M_{n2}(M_{n4})$ of the second source follower composed of $M_{n2}$, $M_{n1}$, and $M_{n5}(M_{n4}, M_{n3}$, and $M_{n6})$ and sent out to the output CDS circuit through the column select switches $M_{n1}(M_{n3}), C_{\rm sela}$, and $C_{\rm selb}$. The second source follower is composed of nMOS devices because pMOS devices are used in the first source follower. Thus, the voltage dynamic range at the output of the second source follower is not reduced by the level shifting of threshold voltage. In the conventional n-well CMOS process, the substrates of all nMOS devices must be connected to the ground together due to the use of a single p-well. Under this circumstance, the source follower composed of nMOS devices suffers from the gain attenuation due to the body effect. However, the 0.25-$\mu$m 1P5M CMOS technology used in the design of the imager chip has the mask of deep n-well beneath the p-well. In other words, the potential of the p-well at the top

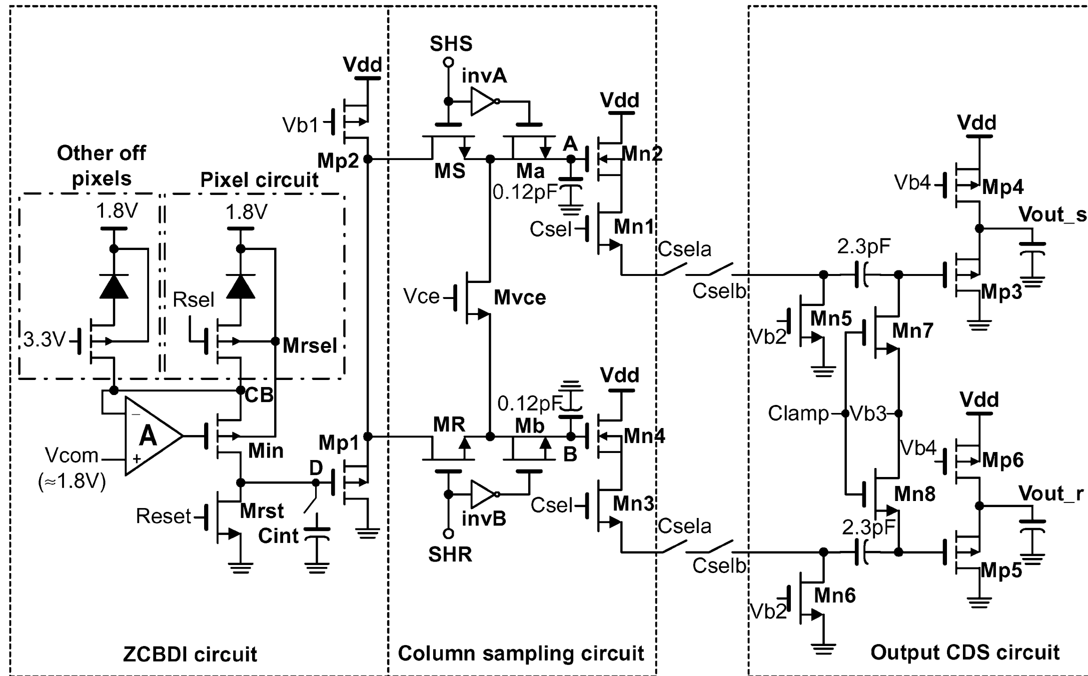


Fig. 6. PAPS structure with ZCBDI readout circuit and the improved DDS circuit.

TABLE III
VALUES OF $C_{\rm HOLD}$, $V_{\rm 1LSB}$, $G_{\rm PGA}$, $I_{\rm leak}$, AND $T_{\rm int}$

| | |
|---|---|
| Chold | 0.24 pF |
| V1LSB | 0.3 mV |
| GPGA | 8 |
| Ileak | 0.45 fA |
| Tint | 30 ms |

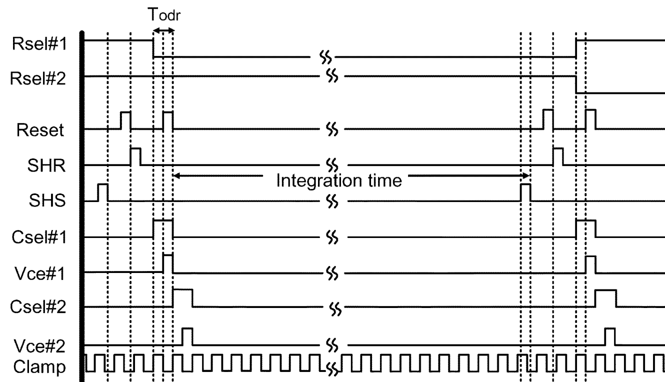


Fig. 7. Major timing diagram of the column readout circuit and the output driver circuit.

of deep n-well can be set to any value. Thus, the substrates of $M_{n2}$ and $M_{n4}$ can be connected to their source and the gain in the nMOS source follower is not attenuated by the body effect. The dynamic range of the output voltage is almost equal to that of the voltage at the integrating capacitor although two types of the source follower are used in the design of column readout circuit. The equalization of both photosignal path and reset signal path controlled by $V_{\rm ce}$ is performed after the readout of the held voltage. The equalized voltage at the two nodes of $A$ and $B$ is then readout to the output CDS circuit.

To reduce the load of the column sampling circuits to the output CDS circuit in the high-resolution CMOS imager and increase the readout speed, every eight column switches are connected together to one switch $C_{\rm sela}$ whereas eight $C_{\rm sela}$ switches are further connected to one switch $C_{\rm selb}$ [21]. In the output CDS circuit, the nMOS devices $M_{n7}(M_{n8})$ controlled by the signal Clamp is to clamp the voltage at the gate of $M_{p3}(M_{p5})$ in the output source follower $M_{p3}$ and $M_{p4}$ ($M_{p5}$ and $M_{p6}$) to $V_{b3}$. The capacitor of 2.3 pF are used to perform the operation of CDS.

The major operational timing diagram is shown in Fig. 7. First, the row select signal $R_{\rm sel}$#1 is low and the reset control signal is high to reset the voltage at the integrating capacitor to 0 V. After the reset operation, the photocurrents of all pixels in Row#1 are integrated at the gate of $M_{p1}$ of Fig. 6 during the integration time. Then, the control signal of SHS is on to sample the photo-signal in the output of the first source follower $M_{p1}/M_{p2}$ to the node $A$ of Fig. 6 as $VS$. After that, the reset control signal is on again and then the control signal of SHR is on to sample the reset signal in the output of the first source follower to the node $B$ of Fig. 6 as $VR$ when the reset control signal is off. As in the APS structure, the duration of reset time is kept long enough to eliminate the amount of residual charges due to incomplete reset. That is, the amount of (KTC noise generated by the trapping of the switch thermal noise in the integration-reset function at the node $D$ of Fig. 6 is the same in $VS$ and $VR$ if the settling time of the voltage at the node D of Fig. 6 during the reset operation is shorter than the reset time [12]. Thus the KTC noise due to the reset operation can be reduced by the CDS operation. The reset signal must be sampled after the reset control signal is off because the effect of clock feedthrough on $VS$ and $VR$ from the reset control signal is the same which can be reduced

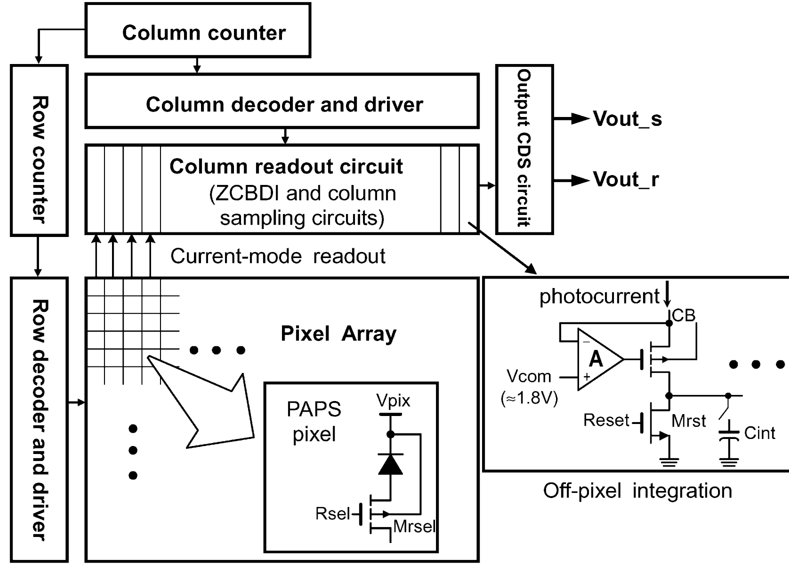


Fig. 8. Block diagram of the proposed PAPS CMOS imager.

by the CDS operation. The integration time $T_{\rm int}$ and frame rate are expressed as

$$T_{\rm int} = {\rm NT}_{\rm odr} \quad (8)$$

$$\text{Frame rate} = 1/[M(N+3)T_{\rm odr}] \quad (9)$$

where $M, N$, and $T_{\rm odr}$ are the row number of imager, column number of imager, and the reciprocal of output data rate, respectively. The registration time of one image is equal to the reciprocal of frame rate.

In the still imager application, the integration time can be adjusted according to the background light intensity. The photogenerated charges in the PAPS CMOS imager can be the same as that in the conventional APS CMOS imager by increasing the integration time. Under this circumstance, the value of SNR is increased due to the lower dark current which leads to lower shot noise. But the frame rate is smaller than that of APS CMOS imager. If a high frame rate is required, the background light intensity should be increased to decrease the required integration time. Under these circumstances, the optional capacitor $C_{\rm int}$ is not used because the voltage saturation at the node $D$ of Fig. 4 will not be occurred.

The clamp signal in the output CDS circuit is then turned on to clamp the gate voltages of $M_{\rm P3}$ and $M_{\rm P5}$ to $V_{\rm b3}$. Then, $C_{\rm sel}, C_{\rm sela}$, and $C_{\rm selb}$ are on to transfer the signal from the column sampling circuit to the output CDS circuit. Finally, $C_{\rm lamp}$ is off and $V_{\rm ce}$ is on, the voltage at both nodes of $A$ and $B$ of Fig. 6 becomes $({\rm VS}+{\rm VR})/2$. If no loss in the stored charges of the capacitor, then the voltage change at the capacitor of 2.3 pF is transferred to the output node of the output source follower composed of $M_{p3}$ and $M_{p4}(M_{p5}$ and $M_{p6})$ as shown in Fig. 6. Thus, we have [21]

$$V_{{\rm out}_s} \cong \frac{{\rm VR}-{\rm VS}}{2} + V_{\rm b3} + V_{\rm cf}, M_{\rm vce} + V_{\rm SG}, M_{p3} \quad (10)$$

$$V_{{\rm out}_r} \cong \frac{{\rm VS}-{\rm VR}}{2} + V_{\rm b3} + V_{\rm cf}, M_{\rm vce} + V_{\rm SG}, M_{p5} \quad (11)$$

where $V_{\rm cf}, M_{\rm vce}$ is the effect of clock feedthrough on the node of $A$ and $B$ of Fig. 6 when the MOSFET of $M_{\rm vce}$ is on and $V_{\rm SG}, M_{p3}(V_{\rm SG}, M_{p5})$ is the voltage drop between source and gate of $M_{p3}(M_{p5})$. As may be seen from (10) and (11), the CDS operation is realized in the output CDS circuit. The FPN in the nMOS source follower of column sampling circuit can be reduced by this CDS operation. The two output signals are sent out and subtracted each other by the subtraction circuit in the off-chip data acquisition (DAQ) card. Thus, the complete operation of the DDS circuit is realized. The FPN caused in the pMOS source follower of ZCBDI circuit in Fig. 6 can be reduced by the subtraction in DAQ card. The effect of clock feedthrough by switching the signal of $V_{\rm ce}$ to equalize the voltages at the two nodes of $A$ and $B$ can also be reduced from the subtraction. The final result after the subtraction of the DAQ card can be written as [21]

$$V_{{\rm out}_r} - V_{{\rm out}_s} \cong {\rm VS} - {\rm VR} + V_{\rm SG}, M_{p5} - V_{\rm SG}, M_{p3}. \quad (12)$$

## III. Chip Architecture

The block diagram of the proposed PAPS CMOS imager is shown in Fig. 8. The $352 \times 288$ (CIF) format of CMOS imager is taken as an example to realize the new PAPS structure. As shown in Fig. 8, the proposed PAPS pixel is composed of one photodiode and one select switch. The integration capacitor is put in the column readout circuit to perform off-pixel integration. The row decoder and the row counter on the left side of pixel array are used to generate the control signals for the row switches. The column decoder and the column counter on the top side of pixel array are used to generate the control signals for the column reset operation, the column switches, the improved DDS circuit of Fig. 6, and the row counter. Each column of the pixel array has a column readout circuit including the ZCBDI circuit to lower the leakage current in the column bus and the column sampling circuits to reduce the FPN. The column readout circuit generates two analog output voltages. One is the signal proportional to the gray scale intensity of the

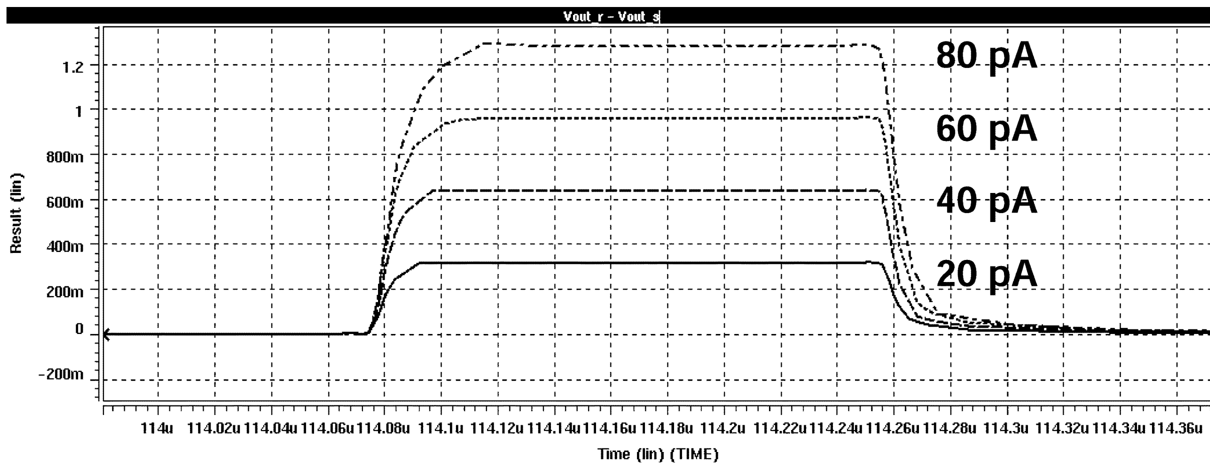


Fig. 9. Simulation results of the voltage difference between $V_{\mathrm{out_}r}$ and $V_{\mathrm{out_}s}$ of Fig. 6 for the input photocurrent from 20 to 80 pA.

image whereas the other is the signal proportional to the reset voltage at the integration capacitor. The output CDS circuit is used to drive the external loads and perform the CDS operation.

The image information is transformed as the photocurrent in the pixel array by using the photodiode. The photocurrent is delivered to the column bus and converted into a voltage signal proportional to the intensity of image after the current integration outside the pixel. The current-mode readout from pixel to column readout circuit avoids the voltage swing in the highly capacitive column bus. The photosignal and reset signal are used for the operation of the improved DDS. The two signals generated in the output CDS circuit are delivered to the PGA, ADC, and display system outside the chip to generate the raw image.

## IV. Simulation and Experimental Results

The simulation results of the voltage difference between $V_{\mathrm{out_}r}$ and $V_{\mathrm{out_}s}$ of the output CDS circuit in Fig. 6 are shown in Fig. 9, where the input photocurrent is from 20 to 80 pA under the readout frame rate of 30 frames/s. As may be seen from these figures, the linearity of the readout circuit is greater than 90% and the maximum output swing is greater than 1.2 V. The readout speed is from 100 kHz to 10 MHz, corresponding to the maximum frame rate above 30 frames/s.

In the experimental chip, a CIF CMOS imager using the proposed PAPS structure is designed and fabricated by using 0.25-$\mu$m 1P5M n-well CMOS process. The depth of n+ diffusion, p+ diffusion, n-well, and deep n-well of this CMOS process are summarized in Table IV. The pixel size is 5.8 $\mu$m $\times$ 5.8 $\mu$m and can be further shrunk. The layout diagram of a single pixel is shown in Fig. 10 where the source of row select transistor is connected directly to the p+ diffusion of the photodiode without contacts to increase sensor area and fill factor. The corner of the photodiode is clipped at 135° to reduce the effect of leakage current at the right angle. The fill factor in the PAPS pixel is 58% that is larger than that of APS pixel reported so far. The fill factor can be designed larger by moving the n-well contact outside the pixel. Thus, the pixel size in the proposed PAPS structure can be designed smaller than that of APS pixel if their fill factor is the same.

TABLE IV
Depth of n+ Diffusion, p+ Diffusion, n-Well, and Deep n-Well in 0.25-$\mu$m 1P5M n-Well CMOS Process

| N+ diffusion | 0.1 μm |
|---|---|
| P+ diffusion | 0.1 μm |
| N-well | 1.2 μm |
| Deep N-well | 2.5 μm |

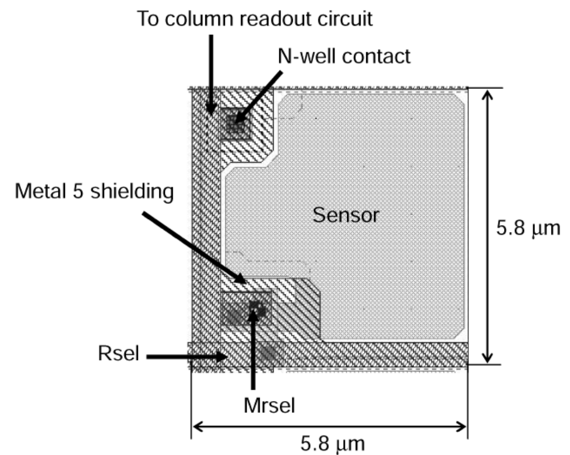


Fig. 10. Layout of PAPS pixel.

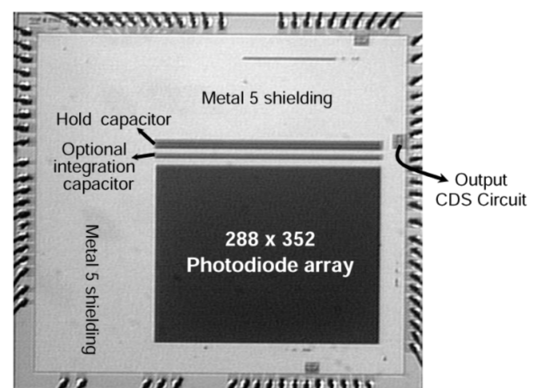


Fig. 11. Die photograph of the test chip.

To obtain the uniform characteristics of the sensor array, two layers of dummy photodiodes are added around the active sensor

Fig. 12. (a) Original image and (b) grayscale image captured by the test chip under the light intensity of 0.57 mW/cm$^2$ and $V_{\rm com}$ of 1.79 V.

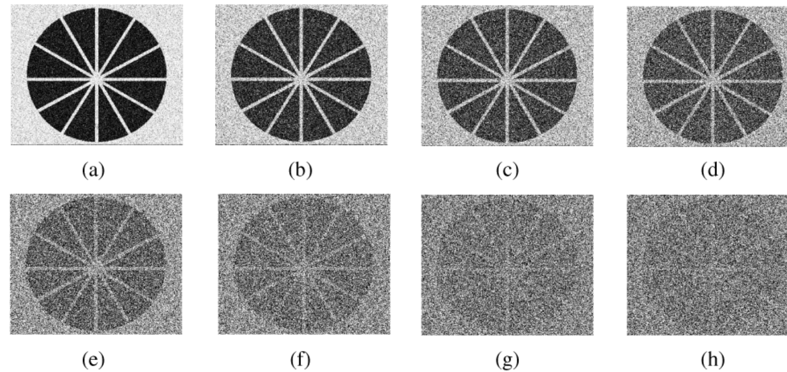

Fig. 13. Image captured by the test chip under the light intensity of 0.57 mW/cm$^2$ and $V_{\rm com}$ of (a) 1.79 V, (b) 1.75 V, (c) 1.70 V, (d) 1.65 V, (e) 1.60 V, (f) 1.55 V, (g) 1.50 V, and (h) 1.45 V.

array. The p+ regions of the dummy photodiodes are connected to n-well to maintain zero bias such as the photodiodes in the active sensor array. The dummy photodiodes are completely shielded by metal 5. In addition, double guard rings are inserted around the sensor cell array to reduce substrate coupling of the digital switching noise. The analog-to-digital converter is not implemented to simplify the design of the test chip. The final chip photograph is shown in Fig. 11 where the area except the regions of sensor and capacitor are covered by metal 5 from light shielding. The total chip size is 3660 $\mu$m $\times$ 3500 $\mu$m.

To test the fabricated CIF PAPS CMOS imager chip, a DAQ card with the function of ADC is utilized to capture the image. The original image and the measured grayscale image captured by the fabricated $352 \times 288$ (CIF) PAPS CMOS imager chip under the light intensity of 0.57 mW/cm$^2$ and $V_{\rm com}$ of 1.79 V are shown in Fig. 12(a) and (b), respectively. The blurs produced in Fig. 12(b) is due to light bulb and can be avoided by using more uniform light sources. The measured images under the light intensity of 0.57 mW/cm$^2$ and different values of $V_{\rm com}$ are shown in Fig. 13(a)–(h). When the value of $V_{\rm com}$ is 1.79 V, the image quality in Fig. 13(a) is good and no observable FPN is presented. With the decrease of $V_{\rm com}$ from 1.79 V to 1.45 V as shown in Fig. 13(b)–(h), the image quality is degraded by the effect of leakage current in the parasitic pn junctions of deselected row switches. The image cannot be clearly seen when the value of $V_{\rm com}$ is smaller than 1.45 V because the leakage current from the parasitic pn junctions of deselected pixels is larger than the photocurrent from the selected pixel. Thus, the function of the proposed new PAPS CMOS imager is successfully verified.

The measurement results of the proposed PAPS CMOS imager with the value of $V_{\rm com}$ equal to 1.79 V are summarized in Table V, where the corresponding parameters of the APS CMOS imager are also given for comparisons. The total power dissipation of the fabricated CMOS imager chip is equal to 24 mW under the power supply of 3.3 V. The dark current was measured by varying the master clock rate and thus linearly controlling the integration time in the dark [21]. An output-referred dark-current-induced-signal of 5.8 mV/s. was measured at room temperature. Based on the conversion gain, the dark current in PAPS CMOS imager is equal to 93 pA/cm$^2$ which is smaller than that of APS [22], [23] and PPS CMOS imager. The sensitivity is 0.16 V/lu $\cdot$ s and the optical dynamic range defined as the ratio of the brightest illuminance without reaching the saturation level of output voltage to the weakest with the output voltage larger than noise level is equal to 72 dB. The sensitivity in the PAPS CMOS imager is smaller than that of APS and PPS CMOS imager due to the low quantum efficiency of $P+/N$-well photodiode. But the optical dynamic range in PAPS CMOS imager is larger than that of APS [22], [23] and PPS CMOS imager because the dark current in PAPS structure is smaller and the use of the optional capacitor of $C_{\rm int}$ in Fig. 4. There are two sources of FPN, namely, pixel FPN, which is caused by mismatch in the pixel circuit, and column FPN, caused by mismatch in the column readout circuit [22]. The FPN is 5.3 mV which is smaller than that of APS CMOS imager with DDS circuits [22] due to the larger pixel FPN in APS CMOS imager although the PAPS CMOS imager has major FPN due to column differences which is larger than that of APS CMOS imager. Thus the proposed

TABLE V
MEASUREMENT RESULTS OF THE PROPOSED PAPS CMOS IMAGER WITH THE VALUE OF $V_{\rm com}$ EQUAL TO 1.79 V AND ITS COMPARISONS WITH THAT OF APS CMOS IMAGER [23]

| Pixel Structure | PAPS | APS [23] |
|---|---|---|
| Technology | 0.25 μm 1P5M N-well CMOS | 0.35 μm 1P3M N-well CMOS |
| Power Supply | 3.3 V | 3.3 V |
| Integration Capacitor | 8.2~208.2 fF | – |
| Output Swing | 1.2 V | 0.8 V (estimate) |
| Readout Speed | 30 frames/sec | 30 frames/sec |
| Linearity | 92% | 80% (estimate) |
| Dark Current | 93 pA/cm$^2$ (room temperature) | 370 pA/cm$^2$ (room temperature) |
| Sensitivity | 0.16 V/lu·s | 0.52 V/lu·s |
| Optical Dynamic Range | 72 dB | 53 dB |
| Fixed Pattern Noise (FPN) | 5.3 mV | 8 ~ 24 mV (estimate) |
| Chip Size | 3660 μm x 3500 μm | 5840 μm x 5010 μm |
| Pixel Size | 5.8 μm x 5.8 μm | 7.4 μm x 7.4 μm |
| Array Size | 352 x 288 (CIF) | 640 x 480 |
| Fill Factor | 58% | 25% ~47% (estimate) |
| Operating Temperature | 25°C | 25°C |
| Power Dissipation | 24 mW | 31 mW |

PAPS CMOS imager can be used in the low-dark-current and high-resolution still imager applications by keeping the value of $V_{\rm com}$ equal to or slightly smaller than 1.8 V.

## V. CONCLUSION

A new pixel structure for still CMOS imager application called the PAPS structure has been proposed and analyzed. In the PAPS structure, the PPS-like pixel circuit, the APS-like column circuit, and the new readout structure called the ZCBDI are used to reduce column leakage current, decrease pixel area, and increase fill factor. The gain loss in the source follower of nMOS devices can be avoided by using the mask of deep n-well to increase the output voltage dynamic range. The improved DDS circuits are also used to suppress FPN, clock feedthrough noise, and channel charge injection. An experimental chip of CIF PAPS CMOS imager is designed, fabricated, and measured. The measurement results verify the function of the new proposed PAPS structure.

With the advantageous characteristics of small pixel area, high fill factor, and low dark current, it is expected that the proposed new PAPS CMOS imager structure can be applied to the design of high-quality and large-array-size still CMOS imagers.

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**Yu-Chuan Shih** (S'98) was born in Chiayi, Taiwan, R.O.C., in 1974. He received the B.S. and M.S. degrees in electronics engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1996 and 1998, respectively. He is currently working toward the Ph.D. degree at the institute of electronics in the same university.

His main research interests include infrared readout circuits, CMOS sensor chips, and analog-to-digital converters.

**Chung-Yu Wu** (S'76–M'76–SM'96–F'98) was born in 1950. He received the M.S. and Ph.D. degrees from the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1976 and 1980, respectively.

He was a Postdoctoral Researcher at the University of California at Berkeley in summer of 2002. Since 1980, he has served as a Consultant to high-tech industry and research organizations and has built up strong research collaborations with high-tech industries. From 1980 to 1983, he was an Associate Professor at National Chiao-Tung University. During 1984 to 1986, he was a Visiting Associate Professor in the Department of Electrical Engineering, Portland State University, Portland, OR. Since 1987, he has been a Professor at National Chiao-Tung University. From 1991 to 1995, he was rotated to serve as the Director of the Division of Engineering and Applied Science on the National Science Council, Taiwan. From 1996 to 1998, he was honored as the Centennial Honorary Chair Professor at National Chiao-Tung University. He has published more than 250 technical papers in international journals and conferences. He also has 19 patents including nine U.S. patents. His research interests are nanoelectronics and very large-scale integration including circuits and systems in low-power/low-voltage mixed-signal design, and systems, biochips, neural vision sensors, RF circuits, and computer-aided design analysis.

Dr. Wu was a recipient of IEEE Fellow Award in 1998 and Third Millennium Medal in 2000. In Taiwan, he received numerous research awards from Ministry of Education, National Science Council, and professional foundations. He is a member of Eta Kappa Nu and Phi Tau Phi.