Design of Miniaturized Common-Mode Filter by Multilayer Low-Temperature Co-Fired Ceramic

Bin-Chyi Tseng, *Member, IEEE,* and Lin-Kun Wu, *Member, IEEE*

***Abstract*—A miniaturized common-mode filter composed of multiple substrates with positive and negative coils formed on alternate substrates is proposed in this paper. The pattern of each positive coil is interlaced with that of each negative coil, whereby when the positive and negative coils are alternately stacked, the positive coil do not overlap the negative coil. With such offset configuration, the parasitic capacitance introduced between positive and negative traces is reduced, so the thickness of each substrate can be decreased and the size of the entire filter is effectively reduced. Good agreements between simulated and measured results are demonstrated. Further, the effectiveness of this filter is confirmed by eye diagram and radiation emission measurements.**

***Index Terms*—Common-mode filter, differential signal, low-temperature co-fired ceramic (LTCC), mixed-mode S parameters, multilayer.**

I. Introduction

With increasing demands on system functionality and data storage, higher datarates in electronic devices is requested. In proportion to the higher operating speed and frequency band, more unwanted electromagnetic radiation is introduced. High-speed data transmission, together with ever lower logic threshold voltage makes today's electronic sets extremely vulnerable to the problem of unwanted noise. In high-speed transmission, signal integrity of the transferred data is a critical issue, and even the total system may suffer from malfunction when sufficient radiation noise is picked up by the interface cables or digital devices [1].

In high-speed data communication, differential signaling has found increasing applications (e.g., IEEE 1394, USB 2.0, gigabit Ethernet, etc.). In principle, common-mode noise picked up by the differential pair will be subtracted. For this reason, differential circuit inherently exhibits better immunity to noise and has been, therefore, gaining popularity in recent years as datarate demands increases.

Although, the ideal differential transmission pair can enhance the immunity capability in noisy environments, discrepancy occurs in delay or pathloss between the paired traces, following imbalanced phase and/or amplitude resulting in the source, load, or the circuit path common-mode current will be introduced [2]. These currents are conducted on the differential pair in the same direction and can act as dominant source of radiated emission at high frequencies. Several published papers [3]–[6] have investigated and analyzed the common-mode current influences. To comply with the various electromagnetic compatibility (EMC) standards, these common-mode currents need to be restricted and suppressed low enough.

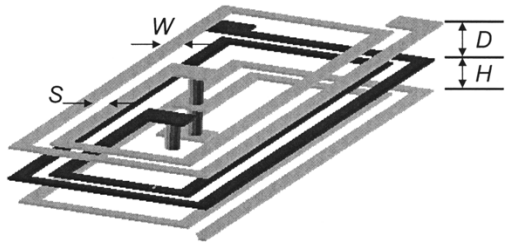

Fig. 1. Three-dimensional (3-D) perspective view of multilayer structure. The gray lines represent $+\mathrm{Ve}$ coil and the black lines represent $-\mathrm{Ve}$ coil.

Common-mode toroid choke, in the form of 1 : 1 longitudinal transformer, is one of the most general methods used to reduce common-mode current [7]. The effectiveness of the common-mode toroid choke relies on the assumption that the high permeability makes the self and mutual inductance equal. The higher permeability ferrite cores can concentrate more flux in the core and reduce any leakage flux. At frequencies on the order of gigahertz or more, the highly degraded effective permeability and severe material loss of ferrite core might compromise the effectiveness of such ferrite choke. Furthermore, the short wavelength of a high-frequency signal may become comparable to the electrical length of the choke coils. Consequently, any small variation in reproducibility of coils and ferrite material may result in significantly degraded performance. Further, the size of the toroid is difficult to reduce, which contribute to effort toward developing alternative multilayer structures with much improved process tolerance and high-frequency material loss [8], [9].

In this paper, the design of a common-mode filter using multilayer low-temperature co-fired ceramic (LTCC) technology for high-datarate applications is presented. The design is to achieve sufficient common-mode suppression while introducing minimal pass-band insertion loss and mode conversion to the desired differential-mode signal. This paper consists of following: in Section II, the designing and equivalent circuit modeling of multilayer LTCC common-mode filter is presented, followed by the miniaturized offset design. Section III discusses the extraction of the equivalent circuit model parameters and illustrates some measured results with the specifications defined at USB-IF.[1] Finally, Section IV gives a summary and some concluding remarks.

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[1]USB-IF, http://www.usb.org

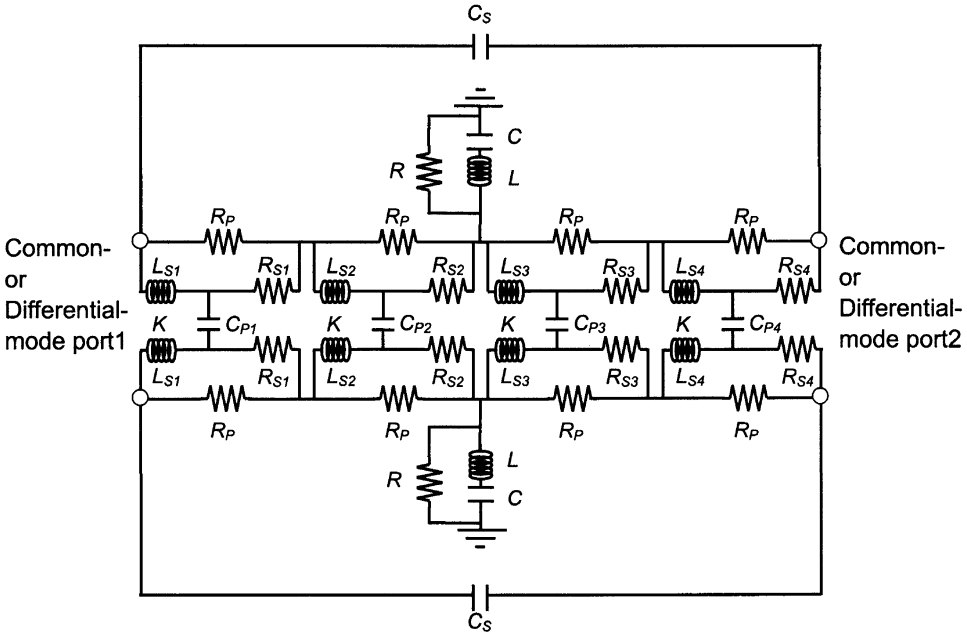

Fig. 2. Equivalent lumped-circuit model.

II. Design and Modeling

A. Equivalent Circuit Model of Multilayer Common-Mode Filter

Fig. 1 shows the structure of multilayer common-mode filter and its equivalent circuit model, which is represented as a coupled equivalent lumped circuit, is demonstrated in Fig. 2. The multiple equivalent lumped-circuit sections are used to represent the plurality of differential pairs in the designed multilayer structure. Each section contains a pair of coupled inductances L_S with series resistances R_S accounting for wiring resistance, shunt resistance R_P signifying the dielectric loss, and a parallel capacitance C_P representing capacitive coupling between positive and negative coils in adjacent layers. In addition, series capacitance C_S denotes the parasitic winding capacitance of each coil. The grounded R and shunt LC of each trace account for antenna effect of the distributed solenoid coil and parasitic coupling between coils and the ground plane of the test board. The magnetic coupling between adjacent differential traces is represented by the coupling coefficient K. With equal vertical spacing (i.e., layer thickness) D of each differential pair, the coupling coefficient K is assumed to be equal for all sections. The equivalent lumped inductance and resistance L_S and R_S are directly proportional to the length of the coil on each substrate. At higher frequencies, equivalent lumped-circuit representation of a distributed transmission line dictates the use of more than one section per layer. This can be done in a straightforward manner, details of which are therefore skipped here.

The typical single-ended scattering parameters (*S* parameters) are not sufficient to accurately characterize a differential component operating in differential mode. To have a solid analysis on a differential device, mixed-mode *S* parameters are introduced [10]. The generalized mixed-mode *S* parameters can be given as

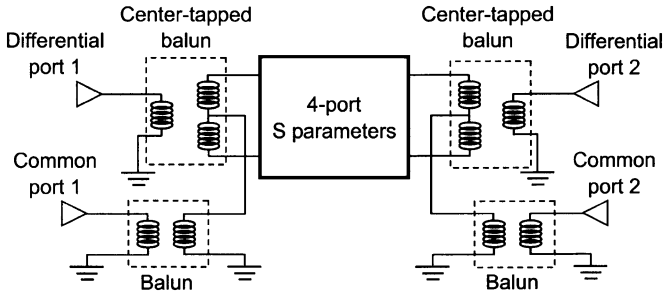

Fig. 3. Circuit used to obtain mixed-mode *S* parameters of differential device.

$$
\begin{aligned}
b_{\mathrm{dm1}} &= s_{\mathrm{dd11}}a_{\mathrm{dm1}} + s_{\mathrm{dd12}}a_{\mathrm{dm2}} + s_{\mathrm{dc11}}a_{\mathrm{cm1}} + s_{\mathrm{dc12}}a_{\mathrm{cm2}} \\
b_{\mathrm{dm2}} &= s_{\mathrm{dd21}}a_{\mathrm{dm1}} + s_{\mathrm{dd22}}a_{\mathrm{dm2}} + s_{\mathrm{dc21}}a_{\mathrm{cm1}} + s_{\mathrm{dc22}}a_{\mathrm{cm2}} \\
b_{\mathrm{cm1}} &= s_{\mathrm{cd11}}a_{\mathrm{dm1}} + s_{\mathrm{cd12}}a_{\mathrm{dm2}} + s_{\mathrm{cc11}}a_{\mathrm{cm1}} + s_{\mathrm{cc12}}a_{\mathrm{cm2}} \\
b_{\mathrm{cm2}} &= s_{\mathrm{cd21}}a_{\mathrm{dm1}} + s_{\mathrm{cd22}}a_{\mathrm{dm2}} + s_{\mathrm{cc21}}a_{\mathrm{cm1}} + s_{\mathrm{cc22}}a_{\mathrm{cm2}}
\end{aligned} \tag{1}
$$

where a_{dmn} and a_{cmn} are the normalized differential- and common-mode incident waves from port n, b_{dmn} and b_{cmn} are the corresponding normalized differential- and common-mode reflected waves. With mixed-mode *S* parameters, a complete characterization of the multilayer common-mode filter, including the differential mode, common mode, and any mode conversion responses, are revealed.

The general 4-port single-ended *S* parameters can be converted to 2-port mixed-mode *S* parameters by using the circuit shown in Fig. 3 [11]. To perform the differential-mode conversion and provide the mechanism for the common-mode terms, a center-tapped balun is used. The common-mode conversion occurs at the center tap of the balun where only common-mode

signals will appear because of the characteristics of the balun. These common-mode signals are then terminated through a balun into common-mode port. By applying this configuration, differential device represented by general 4-port single-ended *S* parameters are converted to 2-port mixed-mode parameters first. Subsequently, the parameters associated with the equivalent circuit of Fig. 2 are extracted and used to fine-tune the structural parameters for the optimization of differential- and common-mode performances and the minimization of component size.

B. Design of Multilayer Common-Mode Filter

Exploring the significant recent advances in the LTCC process techniques for high-frequency application, a multilayer structure using ceramic substrate with relative permeability 1, relative permittivity 4.8, and dielectric loss tangent 0.0016, is designed by employing symmetric structure similar to, but without the drawbacks of, wire-wound common-mode choke. By using longer coupling traces, the lower permeability and the resulting smaller inductance as compared to ferrite material can be compensated. To have long coupling traces, a 3-D multilayer structure with multiturn square spiral on each layer is formed. Each substrate is printed with conductive silver coil pattern and via holes. Positive coils and negative coils are formed on alternate substrates. After all the substrates are stacked, each positive coil is then connected in a sequence through the first plurality of via holes. Similarly, the negative coils are connected as a sequence through the second plurality of via holes.

In such designs, the dielectric and conductor losses are minimized, so any functional signal deterioration can occur mainly from signal reflection [8]. To achieve negligible effect on the transition edges (i.e., the high-frequency components) of differential digital signal, optimized characteristic impedance matching is needed. With good differential signal matching, the insertion loss incurred on the functional signal, evaluated by S_{dd21} of the mixed-mode *S* parameters, will be minimal over its intended operating bandwidth such that differential signal passes through the component undisturbed.

To design such optimum differential mode impedance, a full-wave, 3-D finite-element method-based simulator HFSS (Ansoft, Pittsburgh, PA) was utilized. As a first example, the spiral patterns in all layers are perfectly aligned. The line width W, horizontal trace spacing S, vertical spacing between positive and negative coil in each differential pair D, and vertical spacing H between adjacent differential pairs, as shown in Fig. 1, are parameters used to design an optimized matching. In principle, for the given W and S, different D and H combinations can be used to design different characteristic impedances by varying K and C_P. For simplicity, D and H will apply equal value. Using USB 2.0 as an example, the 90 Ω differential characteristic impedance can be obtained with $W = S = 75$ μm and $D = H = 140$ μm. Fig. 4 depicts the designed filter composed of 4 sets of differential pair and the input/output terminations. To compensate the difference in electrical length of the two differential traces so as to maintain phase balance, one additional layer (i.e., layer M9) for trace length compensation is added.

The simulated results of the designed multilayer common-mode filter with mixed-mode *S* parameters, are shown in Fig. 5.

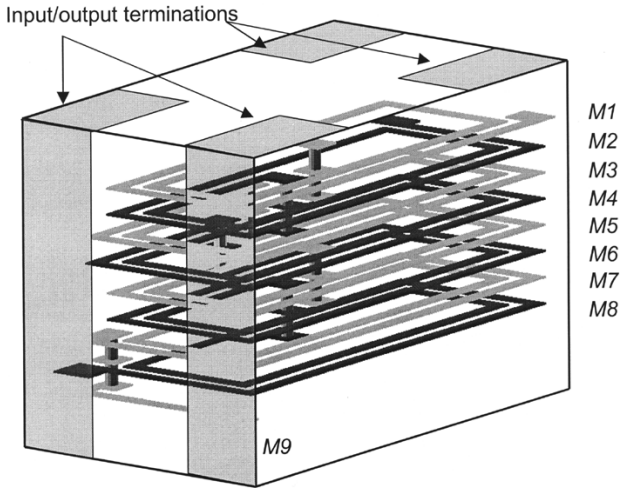

Fig. 4. Structure of the designed filter having four sets of differential pairs and one added layer for trace-length compensation.

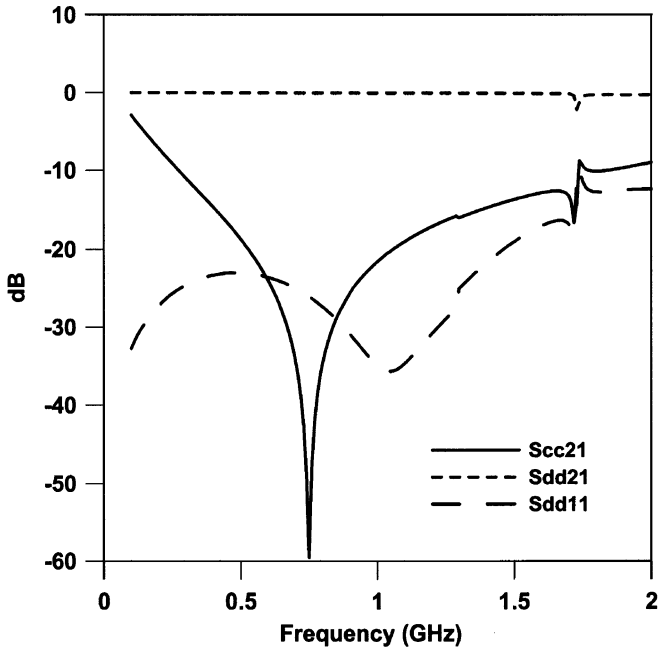

Fig. 5. Simulated result of the designed multilayer common-mode filter.

The S_{dd21} curve represents the insertion loss of differential signal, S_{dd11} curve denotes the reflection coefficient of differential signal, and S_{cc21} is the attenuation of common-mode signal. With both conductor and dielectric losses considered in the simulation, this designed filter provides better than 10-dB common-mode attenuation over the frequency range from 0.273 to 1.74 GHz, very low differential-mode insertion loss of $S_{\mathrm{dd21}} > -0.2$ dB up to 1.7 GHz, and good differential-mode matching with $S_{\mathrm{dd11}} < -10$ dB up to 2 GHz. To confirm the symmetric property of the multilayer design, mode conversion *S* parameters S_{cd21} and S_{dc21} are simulated and shown in Fig. 6. The small value, less than -20 dB, in the entire frequency band ensures the negligible mode conversion is achieved in the designed filter. So only little input energy is converted from differential signal to common-mode noise (i.e., evaluated by S_{cd21}) and only insignificant fraction of input

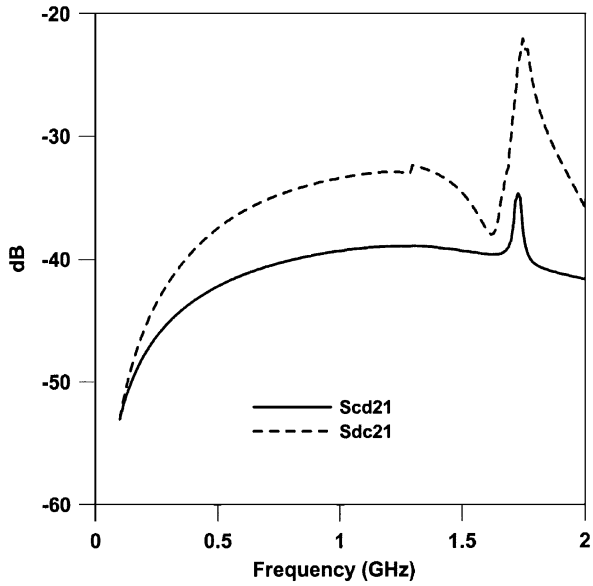

Fig. 6. Mode conversion of multilayer design.

power is transferred from common-mode noise to differential signal (i.e., analyzed by S_{dc21}) at the output of the component. Given such performances, the designed common-mode filter appears capable of supporting broadband differential signaling while simultaneously suppressing the unwanted common-mode noise.

The designed filter is fitted in an Electronic Industries Association (EIA) 1206 form factor (i.e., surface dimension 3.2 mm $\times$ 1.6 mm). The total occupied component thickness with 12-μm conductor thickness and the 10 foil substrates is 1.508 mm. It becomes an unusually thick component and a serious problem, with the width and thickness being almost equal, it is not convenient to differentiate the orientation of component and therefore not suitable for surface mount technology (SMT) assembly. A novel design to shrink the component thickness is thus required.

C. Miniaturization of Multilayer Common-Mode Filter

In the previous design, the positive traces and negative traces in alternate layers are completely overlapped in vertical direction as depicted in Fig. 7(a). The differential-mode characteristic impedance of the transmission pair is determined mainly by the stray inductance and capacitance of traces. Equation for differential-mode characteristic impedance Z_{0d} can be expressed as follows:

$$Z_{0d} = 2 \times \sqrt{\frac{r_s + jwl_s(1-K)}{\frac{1}{r_p} + jwc_p}} \tag{2}$$

where K represents the magnetic coupling coefficient between the two differential traces and r_s, r_p, l_s, and c_p are the per unit length series resistance, parallel resistance, stray inductance, and stray capacitance of the transmission lines, respectively.

To shrink the thickness of component, a thinner substrate is needed. The thinner the substrate, however, the larger the parasitic capacitance c_p is introduced and lowered Z_{0d} would result

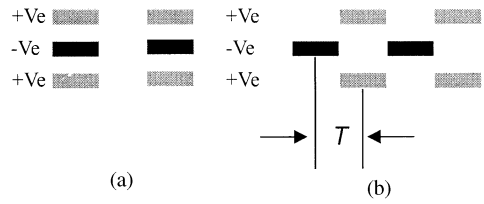

Fig. 7. Differential pair. (a) Completely overlapped. (b) Horizontally offset traces.

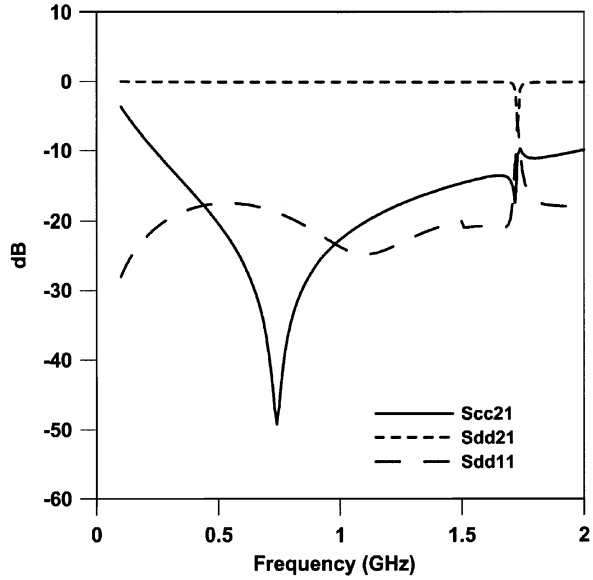

Fig. 8. Simulated mixed-mode *S* parameters result with offset design.

if unattended. Solutions used to overcome the large parasitic capacitance include narrowing the overlapping traces and/or using lower dielectric constant material. However, with the general LTCC process capability nowadays, forming the narrower traces is difficult to perform. In the other solution, even with the lower dielectric constant material (i.e., $\varepsilon_r = 4.3$ is the dielectric constant available for the state-of-the-art of LTCC process) applied, it was not found to result in significant decrease in the component thickness.

Alternatively, the capacitance associated with thin substrate can be lowered by horizontally displacing the originally overlapping traces, that is, an offset design is applied. As shown in Fig. 7(b), for a given layer thickness D, when the horizontal offset (T) between traces in adjacent layers increases the capacitance between traces decreases. For a given capacitance, the larger the offset distance, the thinner the substrate foil can be used, which should result in a reduction in the overall thickness of the component.

Fig. 8 demonstrates the simulated result for the offset structure. A 90-μm foil substrate with offset distance 75 μm is employed in this design. As can be seen in the figure, S_{dd11} remains lower than -10 dB from DC to 2 GHz. Also, S_{dd21} is better than -0.2 dB at the operation frequency (i.e., 240 MHz) and its higher harmonics. For noise elimination, S_{cc21} is better than 10 dB from 0.239 to 2 GHz. From 0.49 to 1.11 GHz, the attenuation on common-mode noise is even larger than 20 dB. To check its mode conversion performance, S_{cd21} and S_{dc21} are simulated and displayed in Fig. 9. Comparing Figs. 6 and 9, one

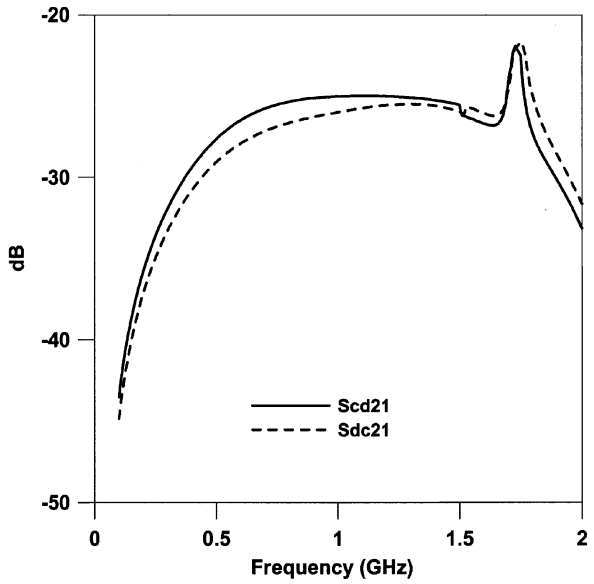

Fig. 9. Mode conversion performance of offset multilayer design.

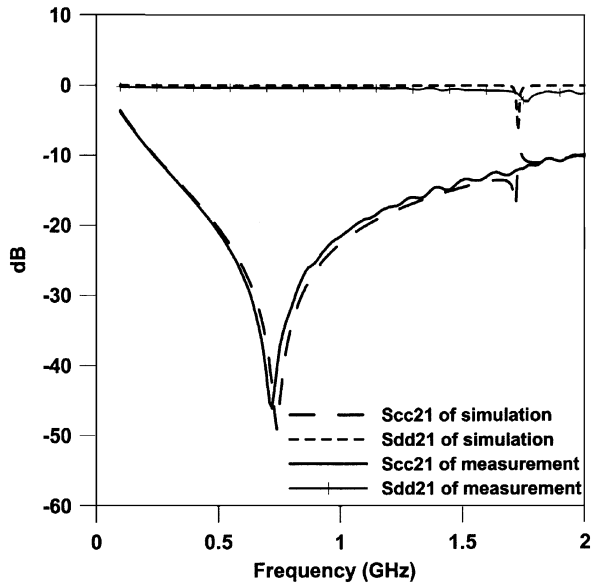

Fig. 10. Mixed-mode S parameters comparisons between simulated and measured results with offset design.

can see that asymmetry between the displaced traces results in poorer, but yet acceptable (i.e., better than -20 dB), mode conversion performance. Comparing Figs. 5 and 8, it is concluded that, while offering comparable or even better performance, the filter designed with offset concept has an overall thickness of 1.008 mm, which is 33% less than the original design using completely overlapping traces.

III. Results and Discussion

A. S-Parameter Measurements and Extractions of Equivalent Circuit Parameters

According to the two different multilayer designs mentioned above, samples are fabricated by LTCC process and measured by using an Agilent E5071B ENA series 4-port vector network analyzer. An short-open-load-through (SOLT) calibration is performed first to de-embed the measurement system and to shift the reference plane to the input/output connectors. To measure the fabricated components, a test board made of FR4 with four feeding traces is applied. By the identical simulated 2-port S parameters of the four feeding traces, the effect of the test board is de-embedded. Fig. 10 demonstrates the good agreement between the simulated and measured results of the offset design.

Due to the long trace length (about 15 mm) on each layer, a multiple sections equivalent circuit is required to obtain a representative equivalent circuit model at high frequency. To extract the parameters of elements used in the equivalent circuit model, the individual inductor is simulated and characterized first [12]. As depicted in Fig. 4, the input pair arranged on the top pair of foils (i.e., M1-M2) has shorter length than the internal pairs (i.e., M3-M4 and M5-M6); this is also the case for the bottom output pair (i.e., M7-M8). For simplicity, the circuit parameters associated with the compensated length on the bottom layer M9 is combined into that of the last pair. With these extracted parameters, L_S and R_S of each inductor, the coupling coefficient K, and parasitic capacitances C_S and C_P are then derived by curve fitting. The simulated mixed-mode S parameters S_{dd21} and S_{cc21} are simultaneously fitted with the equivalent circuit.

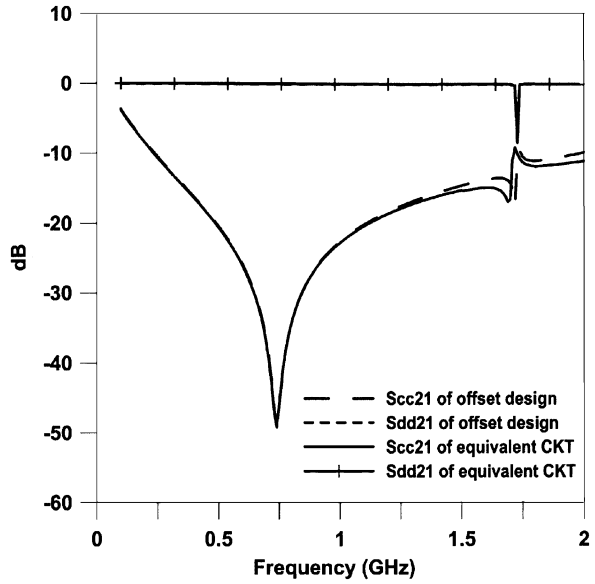

Fig. 11. Comparison between simulated and equivalent circuit model results with offset design.

Finally, the value of insulation resistance R_P is used to adjust the attenuation depth on the resonance frequency of S_{cc21}.

As displayed in all simulated and measured figures, at 1.74 GHz an abrupt change occurs both on S_{dd21} and S_{cc21}. By checking the power conservation, it is found to result from an inefficient antenna effect of the long distributed solenoid coil and parasitic coupling between coils and the ground plane of the test board [13]. The grounded R and shunt L-C resonator, as shown in Fig. 2, is applied to signify these phenomenons, respectively. With 3300 Ω radiation resistance and resonator composed of 820 nH inductance and 0.01 pF capacitance, Fig. 11 demonstrates the good agreements of S_{dd21} and S_{cc21} between the equivalent circuit model and the simulated results. By means of 4 cell sections of the equivalent circuit as shown in Fig. 2, it can accurately model the electrical behavior of the filter to 2 GHz.

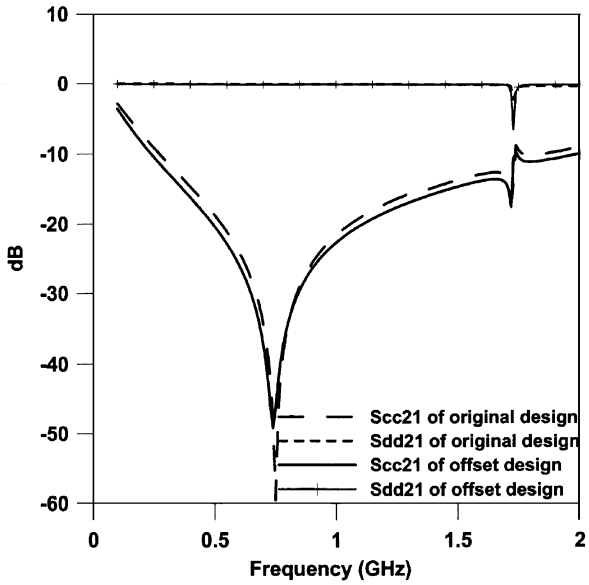

Fig. 12. Simulated results of original thick substrates and offset thin substrates design.

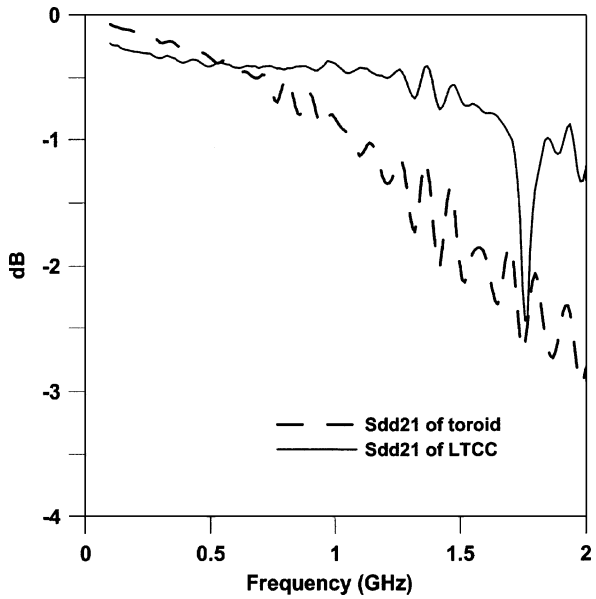

Fig. 13. Comparison of S_{dd21} between a commercially-available toroid and the proposed LTCC design.

TABLE I
SUMMARY OF THE EXTRACTED PARAMETERS FOR THE COMMON-MODE FILTER WITH AND WITHOUT OFFSET DESIGN

Parameters	With offset	Without offset
K	0.94	0.92
L_{S1} (nH)	20.29	17
R_{S1} (Ω)	0.024	0.024
C_{P1} (pF)	0.58	0.59
L_{S2} (nH)	21.71	18.42
R_{S2} (Ω)	0.026	0.026
C_{P2} (pF)	0.46	0.45
L_{S3} (nH)	21.71	18.42
R_{S3} (Ω)	0.026	0.026
C_{P3} (pF)	0.46	0.45
L_{S4} (nH)	20.29	17
R_{S4} (Ω)	0.024	0.024
C_{P4} (pF)	0.4	0.38
R_P (Ω)	6580	3790
C_S (pF)	0.283	0.335
R (Ω)	3300	3300
L (nH)	820	815
C (pF)	0.01	0.01

Fig. 12 compares the simulated results of filters designed with original thick substrates and new offset design with thin substrates. Clearly, very comparable electrical characteristics on common- and differential-mode signals are observed for the two different designs. Table I summarizes the extracted parameters of the equivalent circuit model with and without offset design. As depicted in the table, while C_p's remain nearly unchanged when offset design is applied, the use of the thinner substrate results in larger self-inductance L_S's and magnetic coupling coefficient K. Also, as a result of the overlapping between input/output pads and internal traces, as can be seen in Fig. 4, the parasitic capacitance C_{p1} are larger than C_{p2} and C_{p3}. As for C_{p4}, the shorter overlapped traces and larger distance to input/output pads make it smaller than other C_p's. In view of the common-mode signal path shown in Fig. 2, the frequency of the first null of $S_{\rm cc21}$ that appeared in the simulated and measured results can be approximated by the following equation, in which results calculated from parameters shown in Table I are also given

$$f_{\rm cm} = \frac{1}{2\pi\sqrt{(\sum L_{Sn}) \times (1+k) \times C_S}} = \begin{cases} 745.6\ \text{MHz} & \text{(without offset)} \\ 741.1\ \text{MHz} & \text{(with offset).} \end{cases} \tag{3}$$

Overall, the agreements found among the theoretically predicted and experimentally measured frequency responses confirm the offset design concept proposed here and the validity of the equivalent circuit model.

Fig. 13 compares the $S_{\rm dd21}$ measured for a commercially available toroid (TDK ACM2012-900) and LTCC designs with offset. Clearly, the multilayer design proposed here with ceramic material achieve much better high-frequency performance, which is a combined result of a high degree of magnetic coupling, small parasitic capacitances, excellent differential-mode impedance matching, and very low conduction and dielectric loss.

B. Eye Diagram and Radiated Emission Measurements

To verify the influence on differential signal of the designed common-mode filter, the eye diagram defined in USB 2.0 specifications is measured in system application. Fig. 14 shows the eye diagram measurement setup and the test plane to examine the influence of common mode filter. Using Tektronix TDS7404 oscilloscope and the TDSUSB2 Universal Serial Bus measurement package, Fig. 15(a) and (b) show the measured eye diagram without and with the common-mode filter designed above using offset traces. Due to the small differential-mode insertion loss $S_{\rm dd21}$, there is no significant effect on signal quality when the common-mode filter is added.

By using an ESCO 94 111-1 current probe and a 25-dB amplifier, the spectrum of common-mode current, which is

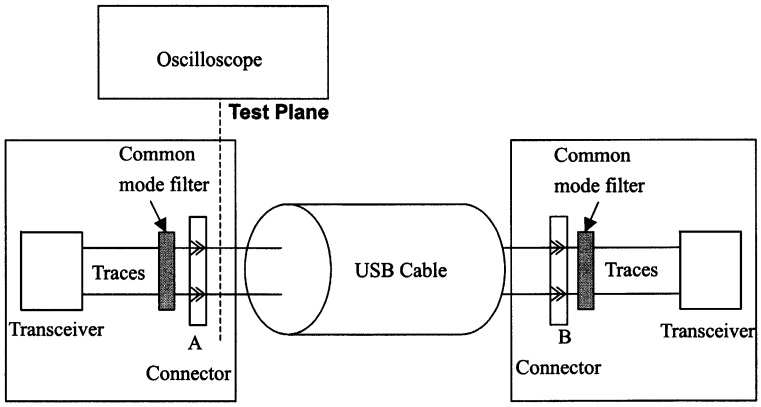

Fig. 14. Configuration of eye diagram measurement.

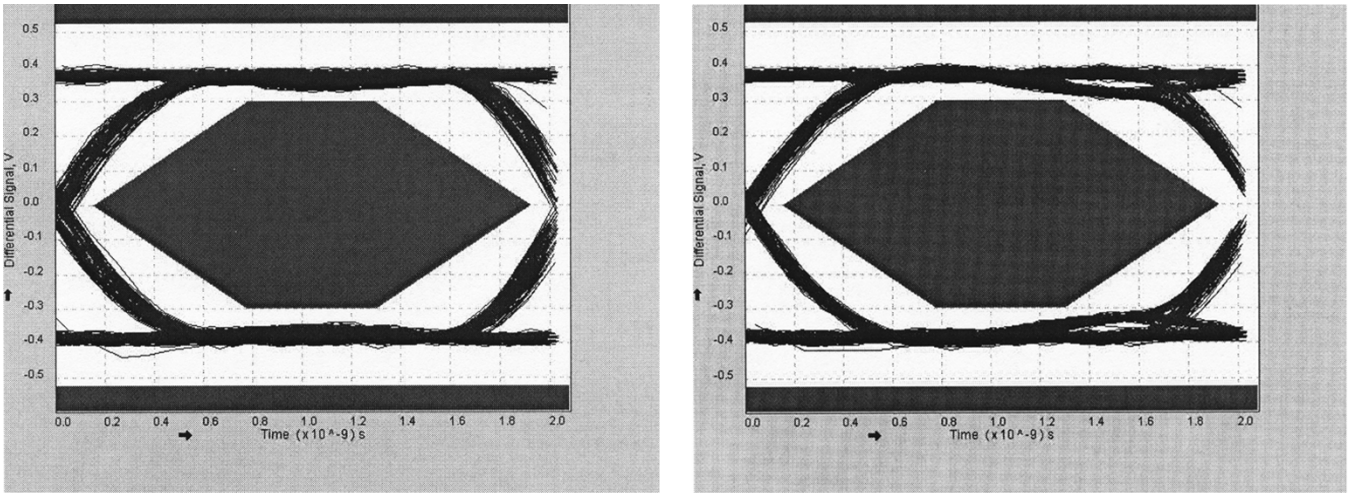

Fig. 15. Eye diagram measurement results. (a) No filter added. (b) Filter added.

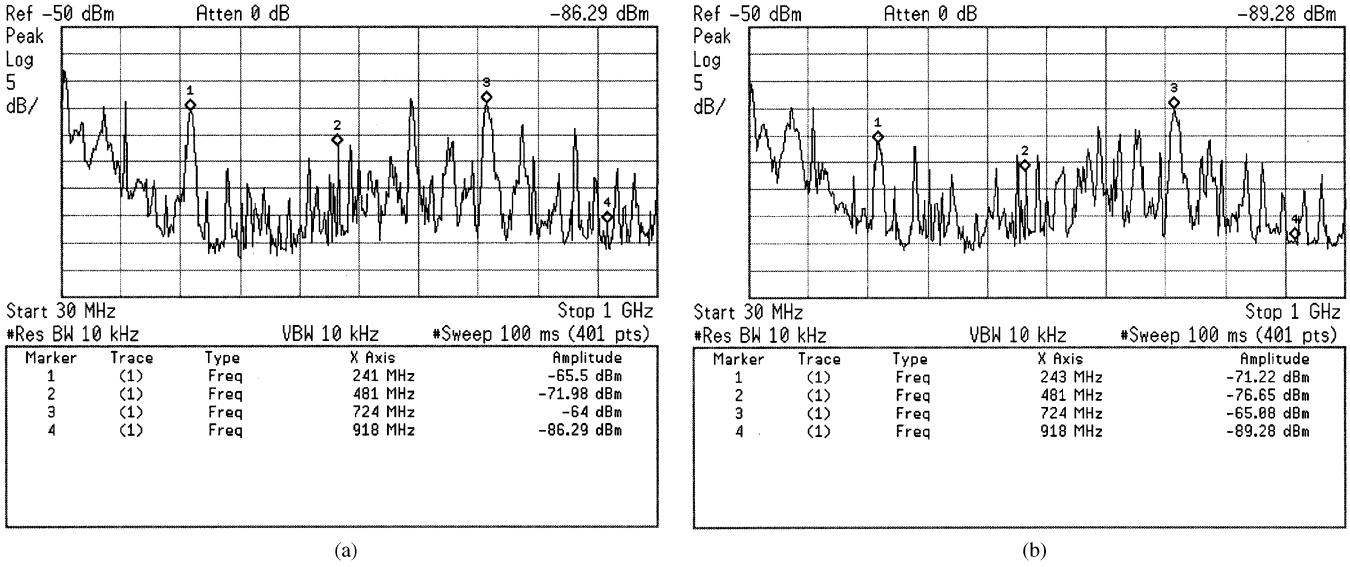

Fig. 16. Spectrum of common-mode current measured. (a) No filter added. (b) Filter added.

resulted from imbalanced differential signal in the absence of the common-mode filter, is measured and depicted in Fig. 16(a). With the balancing effect provided by the common-mode filter, the improved spectrum is shown in Fig. 16(b). When comparing these two figures, the fundamental frequency component (i.e., 240 MHz) is effectively suppressed by 5.7 dB and similar noise suppression performance can also be found around the higher harmonics.

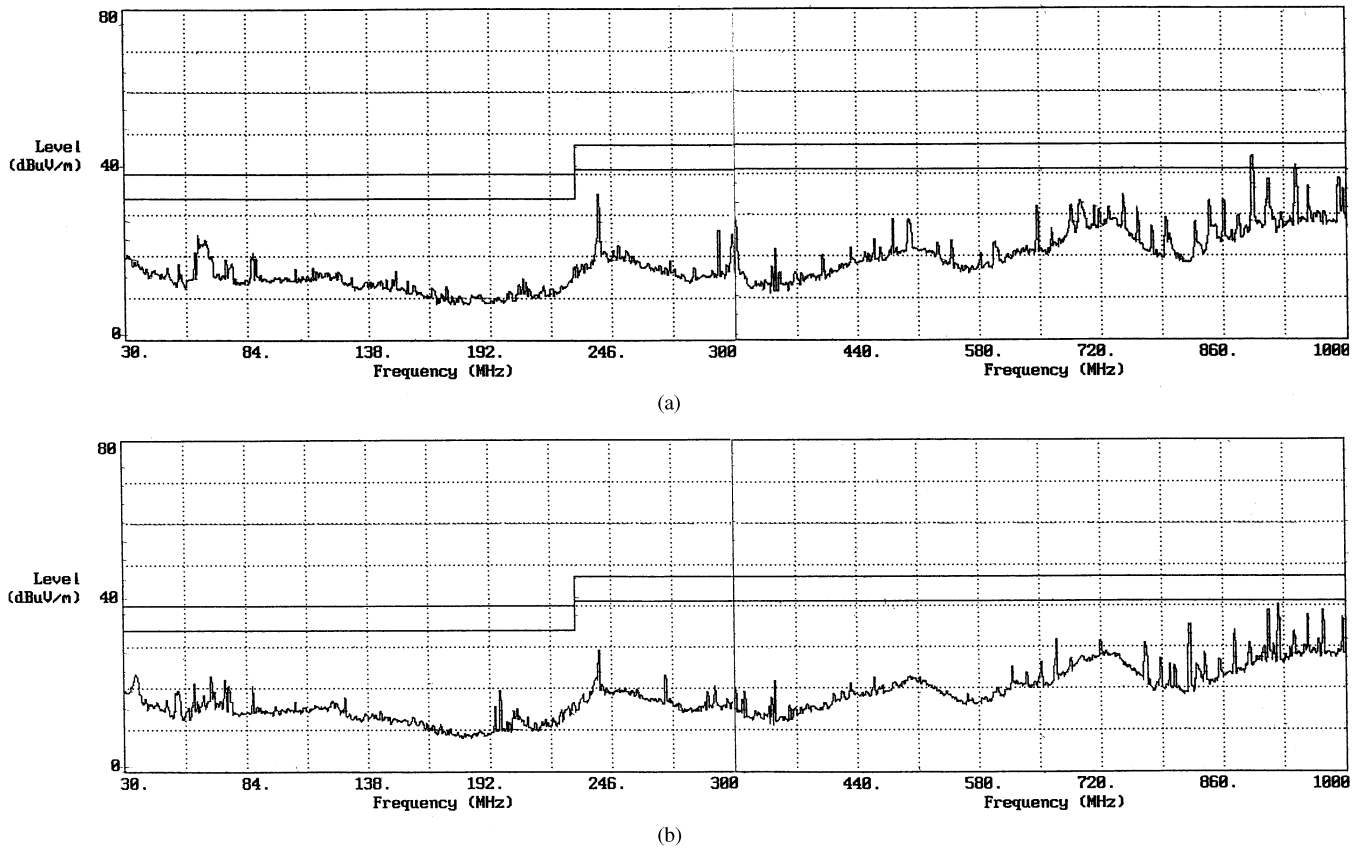

Fig. 17. Spectrum of radiated emission measured in a semi-anechoic chamber. (a) No filter added. (b) Filter added.

As a final check, the radiated emission test conducted in a semi-anechoic chamber for verifying compliance with the CISPR 22 requirements are illustrated in Fig. 17(a) and (b). When comparing these two figures, obtained with and without the designed common-mode filter, the fundamental frequency component (i.e., 240 MHz) is suppressed by 7.6 dB and similar performance can also be observed at higher harmonics especially around 900 MHz.

IV. Conclusion

Common-mode noise, which is often the predominant contributor to the overall noise radiated from circuit boards and electronic instrument, must be eliminated or reduced to an acceptable level to comply with the EMC regulations. Components used to solve such problem are not only asked for providing good noise attenuation and negligibly signal loss but also further dimension shrinkage. In this paper, a miniaturized common-mode filter with offset traces has been proposed. The procedures for the extraction of equivalent circuit parameters, which are needed for fine-tuning the structural parameters to optimize the electrical performance and to minimize the size of the filter, are described. It is shown that while essentially the same electrical characteristics are retained, a 33% reduction of thickness is achieved with an offset design.

In designing a common-mode filter, the 3-D LTCC is advantageous in offering a larger set of structural parameters and a more accurate process than the wire wound structure. The designed multilayer common-mode filter made of LTCC with a high Q-factor ceramic material and a silver conductor produces a lower insertion loss on differential-mode signal than the conventional ferrite-based common-mode filter. This distinguishing feature makes this filter especially suitable for high-speed data communication applications.

As the volume of information transfer grows, data transmission speed in electronic sets will continue to increase. In anticipation of this trend, the noise suppression components need to pursue an even higher operational frequency by using high-frequency material. In a high-frequency band, the ceramic material has lower loss than the conventional ferrite material, so the common-mode filter made of ceramic substrate has better performance than the wire-wound choke using ferrite material for future application.

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