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Nanoflash device with self-aligned double floating gates using scanning probe lithography and tetramethylammonium hydroxide wet etching

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We report a self-aligned technology for nanoflash devices with double floating gates using scanning probe lithography (SPL) technology and anisotropic wet etching. On a (110) SOI silicon wafer, along [001] and [111] directions, a silicon nanowire was generated through local oxidation with SPL followed by wet etching with tetramethylammonium hydroxide solution. Silicon nanowires (SiNW) with profiles of sidewall either sloped or vertical were formed after anisotropic etching in the [001] or [111] direction respectively. After deposition of a polysilicon film on the SiNW with low pressure chemical vapor deposition, nanostructures of a nanoflash device with polysilicon double-floating side gates were obtained along the [111] part of SiNW after reactive ion etching spacer etching. The silicon nanowire channel has a width of 20 nm and a height of 200 nm; the width of the self-aligned floating gate is approximately 40 nm. Silicon nitride was deposited to serve as gate dielectric. The top gate and source-drain aluminum pads were defined by photolithography. Electrical properties of such a nanoflash device with double-floating side gates are discussed. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1826060]

I. INTRODUCTION

Flash memories have enhanced flexibility relative to read-only memories (EPROM) that are electrically programmable but erasable via ultraviolet exposure. Because of larger chip area and power consumption, electrically erasable and programmable read-only memories (EEPROM) are adopted for specific applications only. There has been much research on nanoflash devices with high density, small power consumption, and high access speed, but with the dimensions of the floating gate reaching the sub-100 nm range the fabrication process becomes difficult to control. Several fabrication technologies have been developed for floating-gate flash memories. The nanoparticle dots that are embedded in the oxide layer between a control gate and a channel act as floating memory nodes. It is easy to obtain a small floating gate, but the nanoparticles are invariably randomly deposited.[1] To generate floating dots for a SOI flash memory device, Tang *et al.*[2] made use of a rate of oxidation on silicon that varies with concentration of doping. Choi *et al.* utilized atomic layer doping to fabricate a flash memory with a side channel and a side floating gate.[3] Futatsugi *et al.* developed a Si single-electron memory having an ultra-small floating gate, called a floating dot, stacked on a channel with a self-aligned process; to obtain a narrow channel field-emission microscopy (FET), a line pattern of chloromethyl polystyrene resist was formed with a width of 70 nm and a length of about 200 nm using electron-beam lithography.[4]

Traditional flash memories use one floating gate for each memory cell. The floating gate is generally located near the transistor channel so that the floating gate can be charged via a tunneling current from the channel. Here we describe the fabrication of a nanoflash device with self-aligned double floating gates based on a scanning probe lithography (SPL) technique and anisotropic tetramethylammonium hydroxide (TMAH) wet etching, and demonstrate the electrical properties of nanoflash devices with double-floating side gates.

II. EXPERIMENTS

The devices are fabricated on a *p*-type separation by implantation of oxygen wafer with silicon 75 nm thick and buried silicon dioxide 350 nm thick. After wafer cleaning, a thermally oxidized SiO_2 layer 30 nm thick was formed on the sample surface. The first optical mask was then used to remove thermal oxide to define the active area of a device. Local oxidation was performed by SPL in ambient condi-

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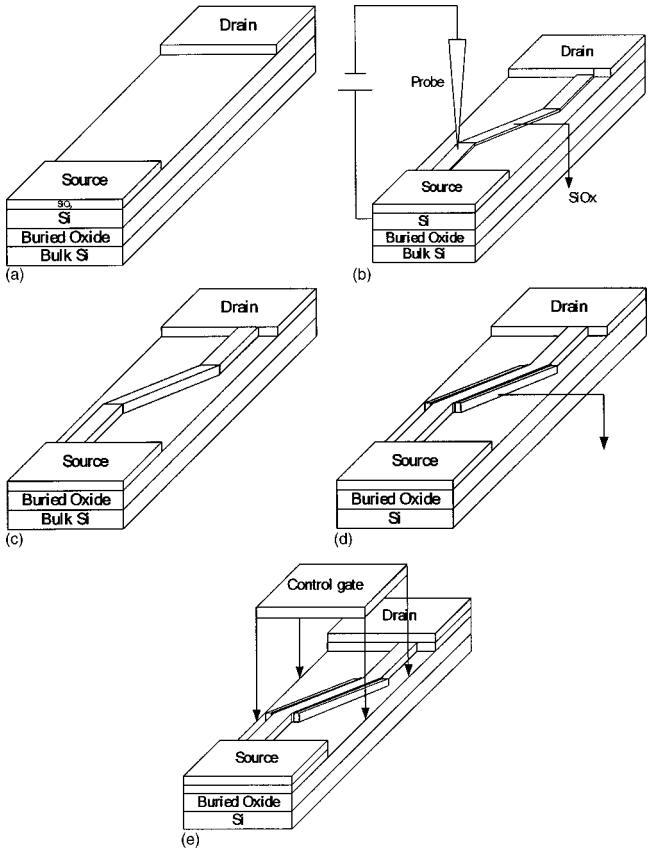

FIG. 1. Schematic diagram of major process steps of a nanoflash device with self-aligned double floating gates. (a) A Si (110) *p*-type SOI wafer was oxidized, and an active region was then patterned. (b) The nano-oxide pattern of a nanoflash was defined using scanning probe lithography. (c) The nano-oxide pattern of a nanoflash was transferred to silicon with TMAH wet etching. (d) The tunneling oxide was grown in a furnace; polysilicon was deposited by LPCVD, followed by RIE spacer etching. (d) The gate dielectric was deposited by plasma enhanced chemical-vapo deposition. After the Al layer was deposited, top gate and source/drain contact pads were defined.

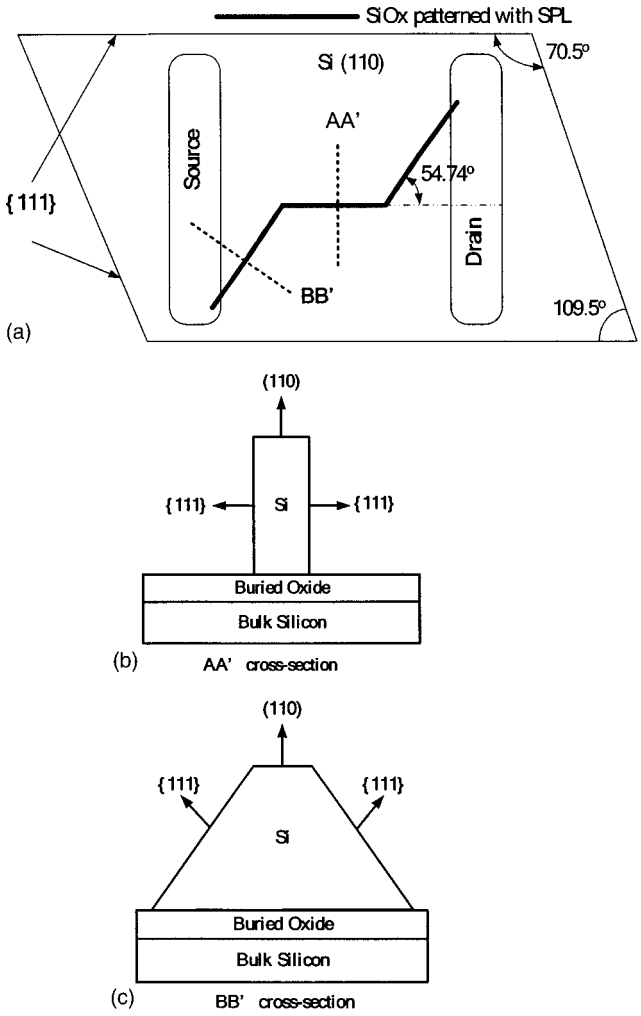

FIG. 2. (a) A Si (110) SOI sample aligned with crystal direction to obtain a SiNW with varied profiles of sidewall. Oxide patterns were generated by scanning probe lithography. The SiNW channel of a nanoflash device was transferred from the oxide pattern into silicon using TMAH wet anisotropic etching. (b) Vertical sidewall of a SiNW channel along [111] (AA′ cross section). (c) Slanted sidewall of a SiNW channel in BB′ cross section.

tions using a PtIr tip to generate nano-oxide patterns along the [001] and [111] directions. SiNW were generated with tetramethylammonium hydroxide (TMAH) wet etching solution. A layer of tunneling oxide of a thickness of 8 nm was also deposited on the SiNW. Subsequently, a polysilicon film of a thickness of 100 nm was deposited on the SiNW with low-pressure chemical vapor deposition (LPCVD). Nanostructures of a nanoflash device with polysilicon double-floating side gates were obtained in the [111] part of a SiNW after reactive ion etching (RIE) etching. Because sidewalls were slanted, polysilicon on the SiNW was all etched away along the [001] direction. After deposition of nitride with LPCVD as gate dielectric and an aluminum layer, both top gate and source-drain pads were defined by photolithography. The process flow is depicted in Fig. 1.

III. RESULTS AND DISCUSSION

Anisotropic wet etching can also make a hexagonal pit array by patterning an oxide grid in a silicon wafer with (110) orientation; this pit is surrounded by four vertical and two slanted {111} planes, but alignment along the right crystal direction is crucial to obtain a vertical sidewall nanostructure. In this work, when oxide patterns generated by SPL were not aligned along vertical {111} planes, the etched hexagonal pit was distorted such that SiNW with slanted sidewalls were obtained. SiNW with vertical and slanted sidewalls were obtained using anisotropic wet etching features. Figure 2(a) shows that a Si (110) SOI sample alignment with crystal direction and oxide patterns was fabricated by scanning probe lithography. The SiNW channel of a nanoflash device was transferred from the oxide pattern using TMAH wet anisotropic etching. The sidewall profiles of a SiNW differ with crystal directions; Fig. 2(b) shows that vertical SiNW channel sidewalls occur along [111] (AA′ cross section) whereas Fig. 2(c) shows slanted sidewalls of a SiNW channel in the BB′ cross section.

Although alkaline chemical solutions such as potassium hydroxide (KOH) are popular for anisotropic wet etching of silicon, the contamination of the mobile ions (K^+) by the KOH solution is unfavorable for processes in the semicon-

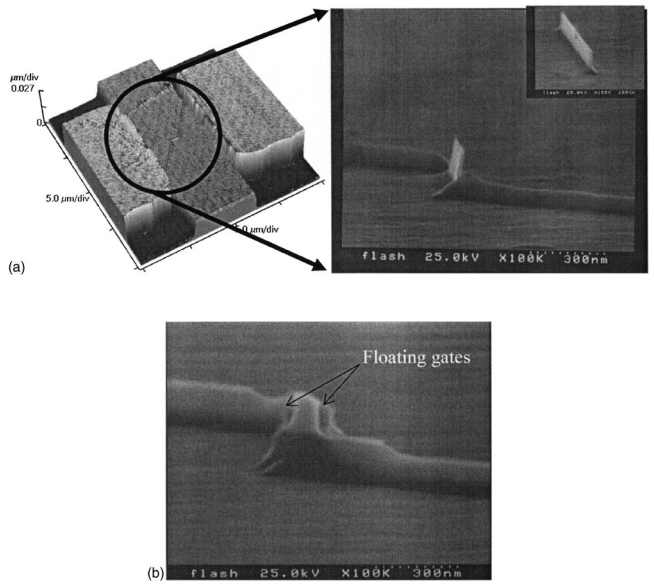

FIG. 3. (a) AFM and SEM images of a SiNW channel of a nanoflash device after TMAH wet etching. The inset shows a SiNW of width 20 nm and length 200 nm obtained along the [111] crystal direction after TMAH wet etching. (b) SEM image of a nanoflash device with double-floating side gates with width about 40 nm and length 500 nm.

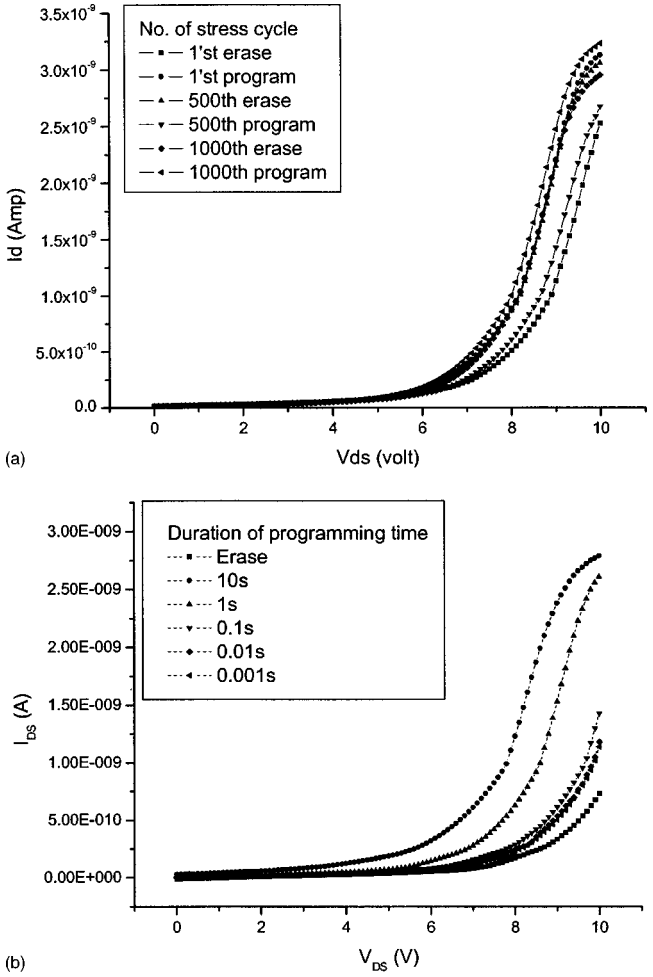

FIG. 4. (a) Operation window narrowing was observed in *I–V* characteristics of a nanoflash device after the device was programmed and erased up to 1000 times; the duration of programming was 10 s. (b) *I–V* characteristics of a nanoflash device programmed using pulses of varied duration.

ductor industry.[5] Moreover, the etching rate and the surface roughness on silicon with KOH solution are difficult to control in nanofabrication. In contrast, although TMAH wet etching produces slower etching than that with KOH solution, its etching selectivity between silicon and SiO_2 is superior. TMAH wet etching also demonstrated superior surface roughness than after KOH wet etching. Both selectivity and surface roughness are important factors for nanofabrication, especially when a thin oxide is used as the etching mask.[6] We adopted TMAH to serve as wet anisotropic etching solution to obtain silicon nanostructures.

Oxide patterns formed on the silicon surface by SPL served as a mask for wet etching with TMAH solution. Figure 3(a) shows antiferromagnetic (AFM) and scanning electron microscopy (SEM) images of a SiNW channel of a nanoflash device. The inset shows a SiNW of a width of 20 nm and a height of 200 nm obtained along the [111] crystal direction after TMAH wet etching. Figure 3(b) shows a SEM image of a SiNW channel with double floating side gates fabricated after RIE polysilicon spacer etching. The tetramethylamonium ions (TMA^+) from the dissociation of TMAH apparently decrease rates of etching of high index crystallographic planes. TMA^+ adsorbed on these high-index crystallographic planes and hindered access of the etching agent (OH^- ions) to the surface.[7,8] As shown in the inset of Fig. 3(a), slant planes invariably form at the bottom of a vertical channel sidewall. As shown in Fig. 3(b), floating gates formed only at the region of a vertical sidewall of a SiNW. Polysilicon coated along [001] was all etched away after RIE etching. The floating gates formed at sidewalls of a SiNW along [111] have a width of 40 nm and a length of 500 nm. With a structure of double floating side gates, they are electrically coupled with the channel of a SiNW. Changes in the source or drain current due to charging/discharging (programming/erase) of floating gates are to be expected.

When electrons tunnel into floating gates (programming), the sidewalls of *p*-type SiNW accumulate such that the conductivity of the SiNW increases, whereas when electrons are pumped out from the floating gates (erasure), the conductivity of SiNW decreases. Figure 4(a) shows the $I_{ds}-V_{ds}$ characteristics of nanoflash memory devices when V_{ds} was swept from 0 to 8 V. During programming, a bias of +20 V was applied to the control gate and a bias of −10 V to the drain. Programming results in electrons tunneling from the channel to floating gates according to the Fowler–Nordheim mechanism. For erasing, a bias of −20 V was applied to the control gate and a bias of +10 V to the drain to pump electrons from the floating gates. As depicted in Fig. 4(a), operation window narrowing was observed in the *I–V* characteristics of a nanoflash device after that device was programmed and erased up to 1000 times. The duration of each program is 10 s. The operation window narrowing is expected to be reduced if silicon nitride was replaced by the silicon oxide in the process.

When V_{ds} was operated at 8 V, the drain current on/off ratio is approximately 7. Figure 4(b) shows characteristics of the nanoflash with respect to the variation of duration of the program. A decreased duration of the program resulted in a decrease of tunneling electrons into the floating gate such that a smaller conductance was observed, but a difference between on/off currents is still clearly identified even with the duration of programming down to 0.001 s.

IV. CONCLUSIONS

A self-aligned technology for nanoflash devices with double floating gates is reported using scanning probe lithography and anisotropic wet etching. On a (110) SOI silicon wafer, along [001] and [111] directions, a silicon nanowire was generated with local oxidation by SPL followed by wet etching with tetramethylammonium hydroxide (TMAH) solution. Polysilicon self-aligned floating gates of a width of approximately 40 nm and a length of 500 nm were fabricated. Programming and erasing of the nanoflash device were performed, and an on/off current ratio up to 7 was obtained. The fabricated nanoflash device with duration of programming down to 0.001 s still demonstrated the electrical features of memory.

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[1]Winkler, F. Merget, M. Heuser, B. Hadam, M. Baus, B. Spangenberg, and H. Kurz, Microelectron. Eng. **61-62**, 497 (2002).
[2]X. Tang, X. Baie, J. P. Colinge, A. Crahaya, and B. Katschmarsyj, Solid-State Electron. **44**, 2259 (2000).
[3]H. Choi, T. Tanabei, N. Kotaki, K. W. Koh, and J. C. Shim, Jpn. J. Appl. Phys., Part 1 **42**, 3361 (2003).
[4]T. Futatsugi, A. Nakajima, and H. Nakao, Fujitsu Sci. Tech. J. **34**, 142 (1998).
[5]M. Madou, *Fundamentals of Microfabrication* (CRC, New York, 2002), p. 215.
[6]W. L. Hung, C. C. Chen, and J. T. Sheu, SNDT 2004, 11–13 May 2004.
[7]I. Zubel and M. Kramkowska, Sens. Actuators, A **93**, 138 (2001).
[8]A. Chimenton, P. Pellati, and P. Olivo, Proc. IEEE **91**, 617 (2003).