Guest Editorial

THE convergence of nanoscience and nanotechnology, biotechnology, information technology, and cognitive based systems creates tremendous opportunities for the improvement of industrial productivity and the quality of human life. Nanoelectronics and its nanotechnology and nanoscience foundations offer such prospects and promises of creative new products for transforming and redefining many industries. This is a multidisciplinary research field which offers great opportunities and challenges for scientists, researchers, and engineers to explore the new frontiers and applications. The achievement and contributions will produce profound and long-lasting impacts in many aspects of our lives, in industry, medicine, scientific research, and aerospace applications, etc.

In the nanoelectronics era, the semiconductor technology continues its rapid progress into the nanometer regime toward the near-10-nnm technology node. Meanwhile, new nanostructures or nanodevices in the scale of 0.1–10 nm are under intensive development through innovative fabrication technologies with new material. With the fast development in silicon nano-CMOS devices and other new nanodevices and nanostructures, significant advanced research activities have been undergoing innovative circuit design with nanoelectronic devices as well as the integration of billions of these nanodevices to form low-power high-frequency intelligent and cognitive gigascale systems. There are new challenges and opportunities in many frontiers, like the design of nanoelectronic processors and computer systems, the design of cognitive and intelligent systems using nanobioelectronic devices, design methodology, and computer-aided design for nanoelectronics systems, etc. The researchers, scientists, and engineers in different fields of circuits and systems, computer, biotechnology, neural science, atomic/molecular physics, and material science, etc., will work closely together to advance future research excellence.

Power Consumption (contributed by Dr. Enrico Macii, Politecnico di Torino, Dip. di Automatica e Informatica, Torino, Italy).

Technology scaling involves important changes in the way circuits and systems are designed. More specifically, the entire design chain requires radical modifications, starting with the system specification step all the way down to the physical implementation phase.

At the low level of abstraction, one of the issues to be faced is represented by the growing importance of leakage power. Recent experiments have shown that in many applications, leakage currents are comparable to dynamic currents in nanometric CMOS gates. Traditionally, leakage control has been considered as a problem to be addressed at the process level. But the advent of the new, nanometric device proves that technological improvements no longer suffice and that better processes must be urgently paired with design solutions, possibly suitable for automated approaches, that will enable to reduce subthreshold and gate-leakage currents.

An equally important opportunity for controlling the power demand of nanometric circuits is provided by the design of the interconnect network, including the clock-distribution tree. Interconnect power optimization entails the capability of accurately modeling self and coupling capacitances, including parasitic elements, and to exploit such models in environments that tackle the optimization problem from a higher point of view. Crosstalk power minimization, congestion control, regularity exploitation and design for manufacturability are further issues that need to be considered while developing low-power design techniques, methodologies, and tools for the nanoelectronics.

From a higher level of abstraction, research will focus on new power modeling capabilities that are able to deal with the size and the complexity of nanometric systems. High accuracy and reduced cost/time for model characterization are some of the parameters the new models will have to exhibit in order to allow their seamless integration into design environments that are able to handle and simulate flexible platforms containing heterogeneous components. In such kinds of platforms, communication will play a fundamental role, due to the high number of processing elements (e.g., cores, digital signal processing, and custom processors) that need to exchange data among each others. In this scenario, conventional bus-based communication by energy aware, nondeterministic communication channels implementing protocols reminiscent of some of the basic concepts used so far in the telecom domain.

New architectures for the memory subsystems will also require particular attention, as chip area tends to be strongly determined by storage devices over the computation logic. Thus, minimization of the energy cost of memory accesses and transfers will result in large power savings on a global basis.

Finally, energy efficiency will be achieved from a system perspective by properly managing (i.e., at run time) the resources involved in computation, communication, and storage, thus implying the need of more sophisticated dynamic power management mechanisms and policies than those currently in use. Low intrusion, low-power demand, and high-workload prediction capabilities are the characteristics the new policies will need to feature in order to become appealing and usable in practice.

Fundamental for bridging the gap between high-level design and the layout and mask generation phases will be the availability of electronic design automation (EDA) technologies, ranging from front-end/back-end interfaces to hybrid simulation environments and synthesizers, in which the power cost function will have the priority. Integration of the two worlds (i.e., high and low levels) is still an open issue, calling for the solution of numerous research and practical problems. Among others, it is worth mentioning resource floorplanning, synthesis of communication interfaces, automatic generation of design wrappers for plug-and-play use of IP components,

Digital Object Identifier 10.1109/TVLSI.2004.836278

and synthesis of flexible and software-programmable power management units.

The list of research challenges to be targeted in the near future in order to allow nanoelectronic devices finding their way into mass-production systems is certainly longer than what we can discuss here. Sure enough, the solution to some of the problems highlighted here will contribute in a decisive way to make nanoelectronics become part of everyone's life.

A. One Highlight Paper and Nine Focused Papers

There have been numerous new developments and achievements in recent years in nanotubes, nanoelectronics, nanoelectro-mechanical systems (NEMS), and the associated circuits and signal/data processing systems. Thus, it is timely to organize a special issue on nanoelectronic circuits and systems to share the vast amount of knowledge accumulated in this fast-growing field.

The research activities in nanoelectronic circuits and systems span many specialty areas and are multidisciplinary. They have attracted very high interest from researchers, scientists, and engineers in governmental laboratories, universities, and leading industrial institutions from all over the world. One highlight paper and nine focused papers have been selected that cover key issues of nanoelectronics, from nanodevice and circuit modeling, CAD, and robust circuits and systems design methodologies, to the analysis and design of interconnect, circuits, and architectures of nanoscale large-array systems.

B. Special Thanks

Successful publication of this Special Issue would not have been possible without the enthusiastic support from the many volunteers and IEEE professionals. Great thanks go to B. Sheu and E. Friedman for their strongest support and assistance in making this Special Issue happen. The Guest Editors would like to express their deep appreciation to E. Kuh, D. Bouldin, E. Macii, the VLSI Steering Committee, N. Ranganathan, Editor-in-Chief, IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATION (VLSI) SYSTEMS, and M. Pham, VLSI Editorial Assistant, and the many tireless reviewers and supporters.

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