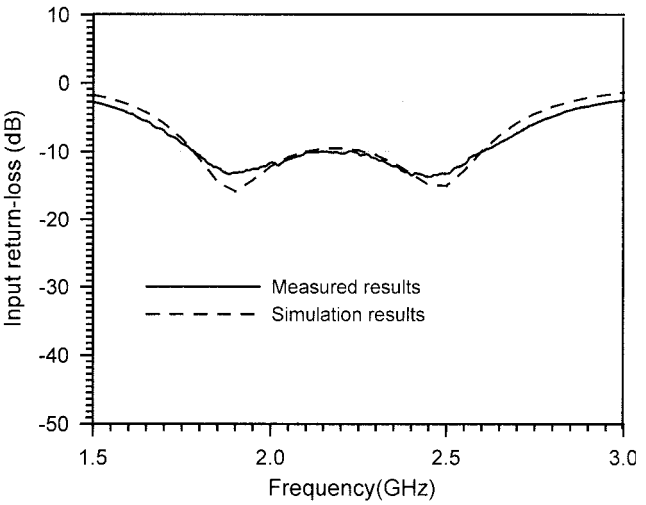

Figure 2 Measured and simulated input-return losses of the nonuniform-width folded-slot antenna fed by CPW

GHz, and a broader bandwidth of 37.4% (1.78–2.60 GHz) for VSWR < 2, which agrees well with the simulation results.

Figure 3 shows the normalized radiation patterns of the folded-slot antenna for the E- and H-planes, operating at the ISM band. These patterns were measured in the anechoic chamber of the Electrical Engineering Department of National Taiwan University. Because of the antenna's balanced feeding port, the radiation patterns appear to be rather symmetric. Comparing the measured data of the electric field at different frequencies, we find that the gain is about 4 dBi and the variation less than 1 dB over the desired frequency range. The gain variation is always obvious over the wide bandwidth on the slot antenna [6].

6. CONCLUSION

Using a nonuniform-width slot, we have presented a folded-slot antenna fed by CPW with tuning slits. The measured results show that the device's bandwidth is broader than that of a conventional folded-slot antenna. In addition, it is applicable on an MMIC device because it does not occupy an unacceptably large space.

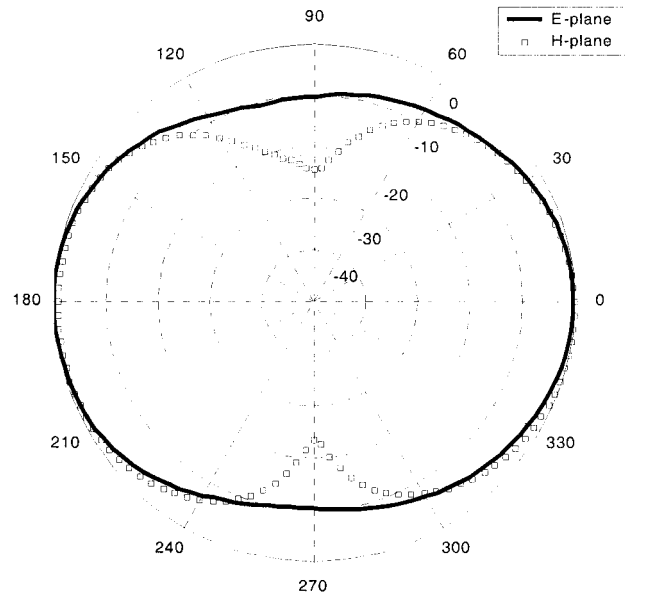

Figure 3 Measured radiation patterns for the CPW-fed nonuniform-width slot antenna for the E-plane (solid line —) and H-plane (□ □ □ □ □ □) at the ISM band

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HIGH-PERFORMANCE BULK AND THIN-FILM MICROSTRIP TRANSMISSION LINES ON VLSI-STANDARD Si SUBSTRATES

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ABSTRACT: *Microstrip transmission lines with very low power loss of 0.4 dB/mm at 50 GHz have been fabricated on Si substrates using an optimized ion-implantation process. These devices have the inherent advantages of smaller chip size and better power performance than CPW lines. Using the same approach, high-performance thin-film microstrip lines are also developed, showing a loss of 0.9 dB/mm at 20 GHz. This approach is compatible with existing VLSI backend layout technology.* © 2004 Wiley Periodicals, Inc.
Microwave Opt Technol Lett 43: 148–151, 2004; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.20404

Key words: *microstrip lines; Si; ion implantation; CPW; thin-film; VLSI*

1. INTRODUCTION

Scaling of Si device technology into the nm-scale regime yields Si transistors with performance reaching into the sub-THz range [1]. However, the performance of MMICs on Si substrates is inferior to those on semi-insulating GaAs ($\sim 10^7$ Ω-cm) due to the large loss of passive devices on low-resistivity Si (10 Ω-cm) substrates [2, 3]. To overcome this problem, we have previously proposed and demonstrated a method to reduce the large RF loss in standard Si substrates using ion implantation, which can selectively form high-resistivity (10^6 Ω-cm) regions in VLSI-standard Si substrates (10 Ω-cm) [4–7]. Excellent coplanar waveguide (CPW) transmission lines with only 0.6-dB loss at 110 GHz [8], as well as

CPW-based broadband filters with small insertion loss (1.6 dB) and 10 GHz bandwidth at 91 GHz [9], have been demonstrated using this technique. In this paper, we successfully demonstrate high-performance microstrip lines on Si substrates. Using proton-ion implantation, the power loss of the microstrip transmission line is reduced significantly from 6.7 dB/mm to only 0.4 dB/mm at 50 GHz. In addition, we also fabricate thin-film microstrip transmission lines using current VLSI backend interconnect processes with a loss of ~0.9 dB/mm at 20 GHz. This approach has the inherent merit of being fully compatible with current VLSI technology without requiring additional masks or process steps.

2. DESIGN PROCESS

Standard 10 Ω-cm resistivity Si wafers of 200-μm thickness were used in this study. Bulk microstrip transmission lines were fabricated on 1.5-μm-SiO_2/Si substrates using 4-μm-thick A1 of 3-mm length and 60-μm width. Thick A1 was deposited on the backside of the wafer to form the bulk microstrip transmission line. For thin-film microstrip transmission lines, a 0.75-mm-length and 20-μm-width strip was formed using the top metal layer (metal-6) of a conventional VLSI backend process, with the first metal layer used as the ground plane. Two-port *S*-parameters were measured up to 50 GHz using an HP8510C network analyzer.

3. EXPERIMENTAL RESULTS AND DISCUSSION

3.1. Bulk Microstrip Lines on Si

Figure 1 shows the power loss for a 3-mm-long microstrip line on 1.5-μm SiO_2-isolated Si, where the loss increases from 2.8 dB/mm to 6.7 dB/mm as the frequency increases to 50 GHz. This loss is greater than that of the CPW transmission line, as shown in Figure 1, over the same frequency range. The larger loss in the microstrip transmission line than in the CPW line is due to the vertical EM field being fully inside the lossy Si substrate, whereas the horizontal EM field in CPW line is only partially within the Si substrate.

The increasing power loss at high frequency is an issue for Si RF IC technology, since future wireless communications require higher frequencies and bandwidths. As shown in Figure 1, our microstrip transmission lines with proton implantation show an improved power loss of ≤0.4 dB/mm at 50 GHz. This value is similar to that of CPW transmission lines with the same ion implantation [6, 8] and comparable to the loss in semi-insulating GaAs obtained from EM simulation using IE3D.

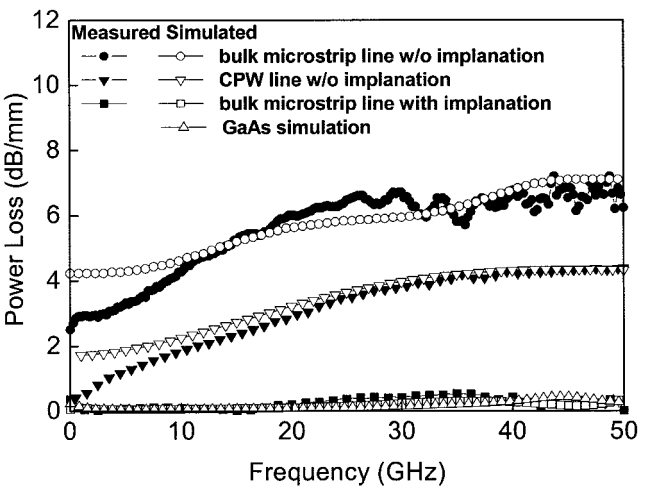

Figure 1 Measured and EM-simulated power loss of 3-mm-long bulk microstrip transmission lines. For comparison, results for a 1-mm-long CPW line are included. Implantation produces a large loss reduction, from 6.7 dB/mm to 0.4 dB/mm at 50 GHz

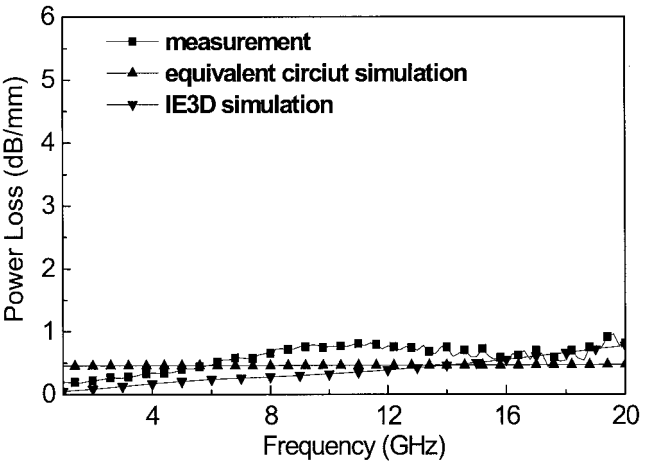

Figure 2 Measured and EM-simulated power loss of 0.75-mm-long thin-film microstrip transmission lines. The measured loss at 20 GHz is <1 dB/mm, that is much lower than the bulk CPW (3 dB/mm) and microstrip lines (6 dB/mm) in Fig. 1 without implantation

3.2. Thin-film Microstrip Lines on Si

Using the same approach of forming a high-resistivity layer by proton implantation, we have also designed and fabricated thin-film microstrip transmission lines. The isolation layer is from the multiple layers of SiO_2 used in the VLSI backend process. Figure 2 shows the measured and EM-simulated power loss. As can be seen, the power loss is ~0.9 dB/mm at 20 GHz, which is much lower than that of the unimplanted bulk CPW and microstrip lines shown in Figure 1. Although the loss of the thin-film microstrip line at 20 GHz is larger than the 0.25 dB/mm in ion-implanted bulk microstrip lines, this process uses simple layout technology without adding additional mask and process.

Because the transmission line is a passive device, the RF loss L is equivalent to the generated noise [8] with equivalent noise temperature of $(L - 1)T_0$. The noise from advanced 0.18-μm and 0.13-μm MOSFETs is ~2.5 dB at 20 GHz [10], whereas the unimplanted CPW and microstrip transmission lines typically

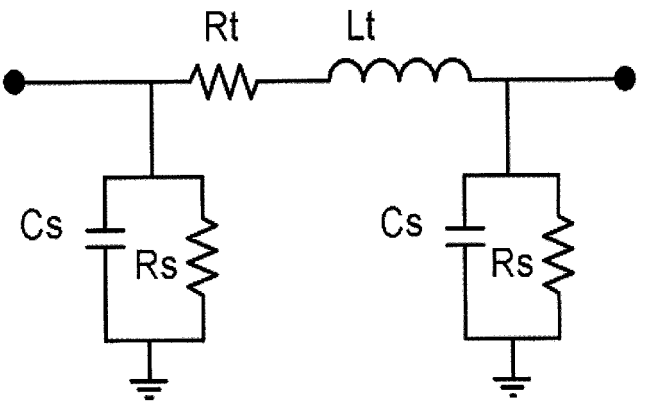

Figure 3 Physically based equivalent circuit for the microstrip transmission lines (*Lt* is the line inductor, *Rt* is the parasitic resistor of the transmission line). The substrate loss is modeled by the shunt *Rs* and *Cs* to ground

10show larger noise and would dominate the overall noise floor of an RF system. However, the noise floor can be significantly reduced by using the thin-film microstrip line, even for a length as long as 1 mm. Further improvement may be possible by improving the dielectric loss of the low-temperature-formed SiO_2 or by increasing the thickness of the dielectric layer. This will be possible using the advanced 1-poly-9-metal layer (1P-9M) process of the 90-nm technology node and beyond. This will further reduce the performance gap with the bulk microstrip transmission line using proton implantation or that on GaAs, with the inherent merit of only changing the layout of current VLSI.

3.3. Modeling and Analysis

We use the physically based equivalent-circuit model shown in Figure 3 to simulate the *S*-parameters. *Lt* and *Rt* are the series inductor and parasitic resistor from the long microstrip transmission-line body, respectively. The symmetrical *Rs* and *Cs* at the respective input and output ports represent the RF signal losses to the ground plane, which should be large for the bulk microstrip line formed on VLSI-standard low resistivity Si substrate (10 Ω-cm) without ion implantation.

The measured and simulated *S*-parameters of the bulk and thin-film microstrip transmission lines, with or without implantation, are shown in Figures 4(a) and 4(b). Good agreement is obtained between the measured and modeled *S*-parameters, suggesting that the equivalent-circuit model in Figure 3 is appropriate.

The extracted substrate impedances, deduced from the *Rs*-*Cs* subcircuits for both bulk and thin-film microstrip transmission lines, are shown in Figure 5. For the bulk microstrip lines on standard Si, the proton implantation can increase the substrate impedance by more than one order of magnitude. For the thin-film microstrip lines, the relatively high substrate impedance arises from the high-resistivity SiO_2 dielectric inside the microstrip-line body.

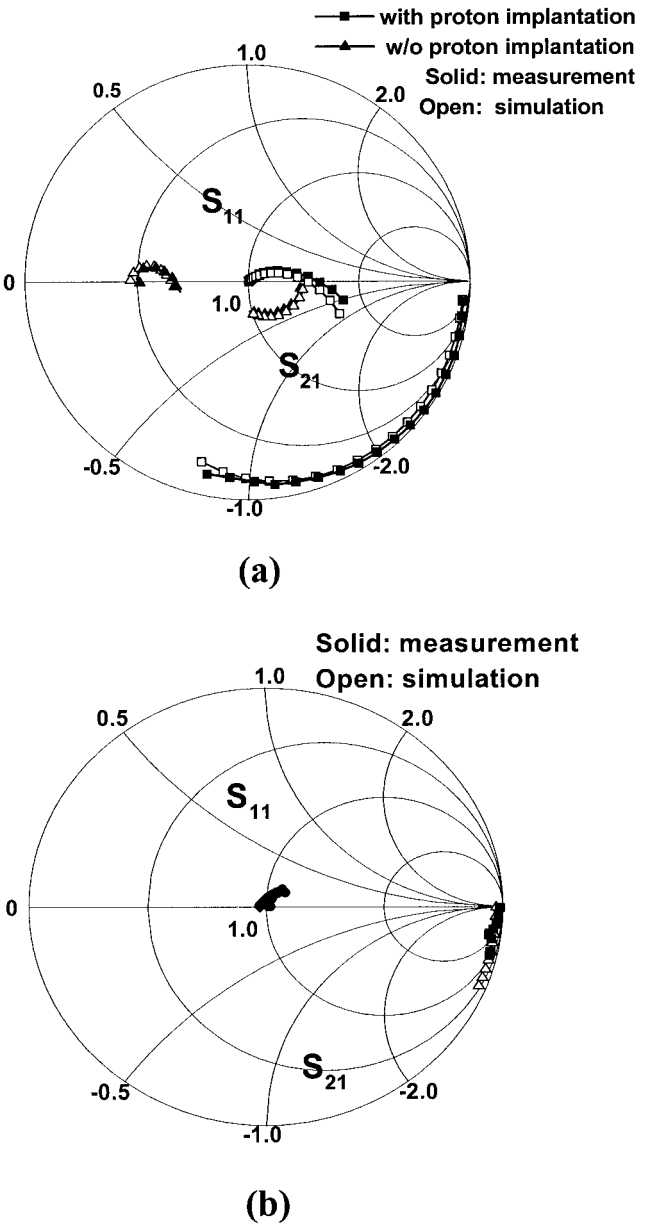

Figure 4 Measured and equivalent-circuit modeled *S*-parameters of (a) bulk and (b) thin-film microstrip transmission lines on Si substrates. The effect of proton implantation is shown in (a). The different curve lengths are due to different frequency ranges: 50 GHz in (a) and 20 GHz in (b)

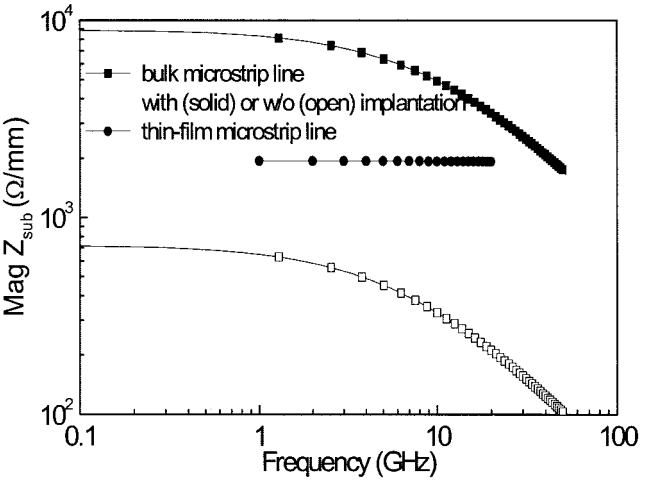

Figure 5 Extracted magnitude of the substrate impedance/mm derived from the bulk and thin-film microstrip transmission lines. The effect of proton implantation is to increase the substrate impedance and thus reduce the loss of the bulk microstrip transmission line

4. CONCLUSION

We have achieved extremely low power loss for both bulk (0.4 dB/mm at 50 GHz) and thin-film (0.9 dB/mm at 20 GHz) microstrip transmission lines on VLSI-standard Si substrates. Proton implantation has selectively transformed the low-resistivity Si substrates of the bulk microstrip transmission line into a high-resistivity state. The high performance of thin-film microstrip line results from the high-resistivity SiO_2-dielectric being inside the microstrip-line body. Both transmission lines can be integrated into RF circuits and distributed devices at a reduced size, as compared with the use of CPW lines.

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CHARACTERIZATION OF RESISTIVE-LOADED WIRE LOOP IN UWB (IMPULSE) RADIO

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ABSTRACT: *This paper discusses the applicability of loaded circular-loop antennas for impulse radio systems using a time-domain integral-equation (TDIE) method. The circular loops loaded with lumped and distributed resistances are characterized for pulse radiation and reception. The effects of the loads on the current distributions are investigated. The performance of the system comprising two identical loop antennas is examined and validated by measurement for ultra-wideband applications.* © 2004 Wiley Periodicals, Inc. Microwave Opt Technol Lett 43: 151–156, 2004; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.20405

Key words: *time-domain integral equations; loaded loop antennas; transient response; ultra-wide band*

1. INTRODUCTION

Recently, the applications of ultra-wideband (UWB) technology to commercial radio systems have gained increasing interest from both academia and industry. UWB systems usually require antennas to be broadband, small in size, and omnidirectional. There are many proposed antennas for UWB systems, such as thin wire monopoles, planar monopoles, loop antennas, and so forth. Among them, the loop antenna in a simple form has the advantages of small size and omnidirectional features, but its impedance bandwidth is narrow. Similar to straight dipoles and monopoles, loading techniques can be used to broaden the bandwidth of a loop antenna. This paper investigates the effects of the applied load on the performance of the loop antenna for UWB impulse radio.

A lot of work has been done on the transient response of loop antennas [1–4]. For example, the singularity expansion method (SEM) was successfully applied to the broadband equivalent circuit synthesis of circular-loop antennas for the perfectly conducting loop and uniformly loaded loop. However, the SEM cannot easily analyze a loop with a nonuniform load. Therefore, the time-domain integral-equation (TDIE) method, which is capable of modeling various load schemes, is selected for the analysis of loaded-loop antennas.

In this paper, circular loops loaded with lumped and distributed resistances are investigated. The effects of the load are discussed with the aid of snapshots of the currents on the loops. The efficiency of the loop antennas with different load schemes is compared and discussed. The radiation patterns over a wide frequency range are examined. To evaluate the reception ability, the normalized sensitivity is calculated. The voltage-transfer functions and received pulses for antenna systems built with such loops are compared and validated by measurements.

2. ANTENNA GEOMETRY AND LOAD SCHEMES

Figure 1 shows the geometry of the circular-loop antenna under study. The loop radius is $b = 13$ mm and the wire radius is $a = 0.5$ mm. Therefore, the shape factor of the loop is $\Omega = 2\ln(2\pi b/a) = 10.2$. The internal impedance at the feed point is 100Ω. The angle ϕ represents the position on the loop. To investigate the characteristics of the loaded loops, four load schemes are considered.

2.1 Perfectly Conducting Loop

This is a closed and perfectly conducting wire-loop antenna.

2.2 Lumped Absorbing Load

The lumped resistive load at the position $\phi = \pi$ is 240Ω, which is called the absorbing load in this paper. The optimized absorbing load results in very little or no ringing in the late time of the

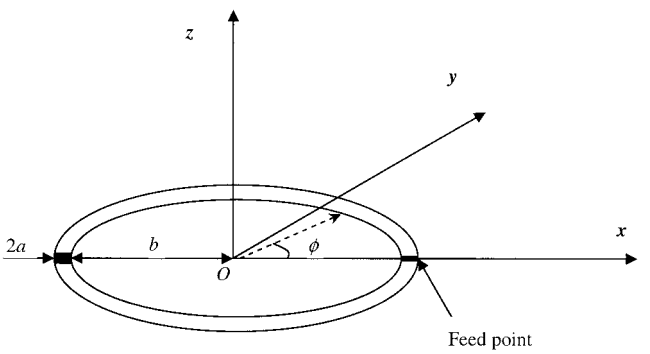

Figure 1 Geometry of the loop antenna