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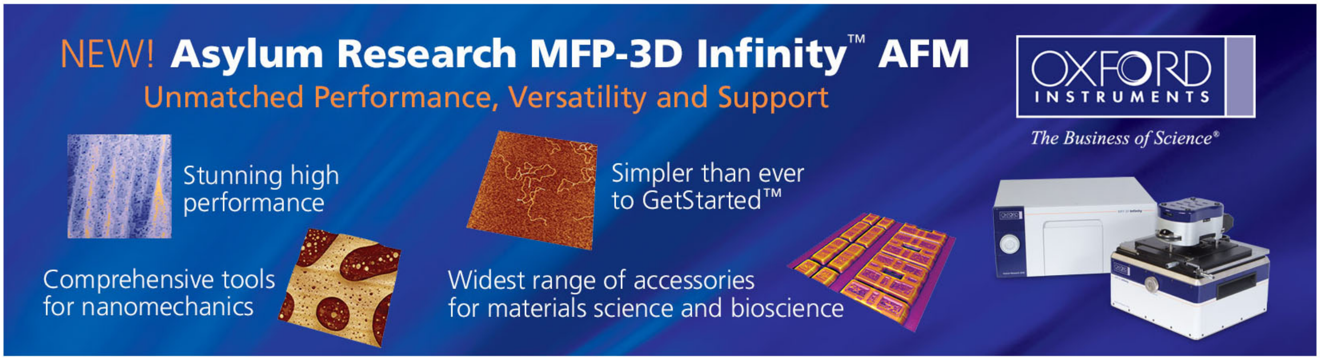
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The characteristics of hole trapping in HfO_2/SiO_2 gate dielectrics with TiN gate electrode

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The characteristics of charge trapping during constant voltage stress in an *n*-type metal–oxide–semiconductor capacitor with HfO_2/SiO_2 gate stack and TiN gate electrode were studied. We found that the dominant charge trapping mechanism in the high-*k* gate stack is hole trapping rather than electron trapping. This behavior can be well described by the distributed capture cross-section model. In particular, the flatband voltage shift (ΔV_{fb}) is mainly caused by the trap filling instead of the trap creation [Zafar *et al.*, J. Appl. Phys. **93**, 9298 (2003)]. The dominant hole trapping can be ascribed to a higher probability for hole tunneling from the substrate, compared to electron tunneling from the gate, due to a shorter tunneling path over the barrier for holes due to the work function of the TiN gate electrode. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1808228]

As devices are scaled aggressively into nanometer regime, SiO_2 gate dielectric is approaching its physical and electrical limits. The primary issue is the intolerably huge leakage current caused by the direct tunneling of carriers through the ultrathin oxide. To substantially suppress the leakage current, high-*k* materials are recently employed by exploiting the increased physical thickness at the same equivalent oxide thickness (EOT). Among them, HfO_2 has been demonstrated to be highly attractive because of its relatively high dielectric constant (~25), sufficiently large band gap (~5.9 eV), suitable tunneling barrier height for both electrons and holes (>1 eV), and thermal compatibility with contemporary device processes.

Even though HfO_2 films have been shown to be scalable to below 1 nm,[1] there still exist several issues that need to be tackled before they can eventually replace SiO_2 dielectric in production. One of the most important issues for HfO_2 is the charge trapping, which leads to threshold voltage instability.[2–6] In this work, we investigate the characteristics of charge trapping in the HfO_2/SiO_2 gate stack with TiN gate electrode. Contrary to most previous reports,[2–6] it is found that hole trapping, rather than electron trapping, prevails in the HfO_2/SiO_2 gate stack during constant voltage stressing (CVS). By employing the distributed capture cross-section model,[2,3] the behavior of hole trapping can be well predicted over several decades of stress time; that is, charge trapping is caused by the hole filling of as-fabricated traps with distributed capture cross section.

The capacitors were fabricated on *p*-type (100) silicon wafers with local oxidation of silicon isolation. After HF-last dipping, a 1.1-nm-thick ultrathin oxide layer was grown at 800 °C by rapid thermal annealing (RTA) in O_2. Subsequently, an approximately 5 nm HfO_2 film was deposited by atomic vapor deposition (AVD™) in an AIXTRON Tricent® system at a substrate temperature of 500 °C, followed by N_2 RTA at 500 °C for 30 s. A 5000 Å TiN electrode was sputtered and patterned to form gate electrodes. Then, wafers were sputtered with aluminum on the back side, and received a forming gas anneal at 400 °C for 30 min. The EOT and initial flatband voltage of the stack before stressing are estimated to be 24 Å and 0.005 V from the high-frequency (100 kHz) capacitance–voltage ($C-V$) curves using UCLA CVC method without considering quantum effect.[7]

Figure 1(a) shows the $C-V$ curves of a metal–oxide–semiconductor (MOS) capacitor measured after different

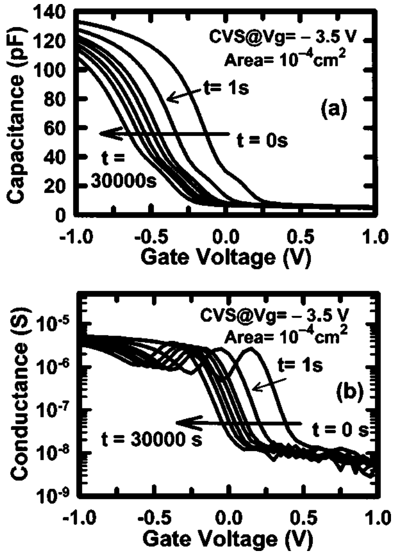

FIG. 1. (a) Capacitance–voltage curves and (b) conductance–voltage curves measured at 100 kHz with stress time as a parameter. The stress voltage (V_g) was −3.5 V. The curve labeled $t=0$ s corresponds to the data before stressing.

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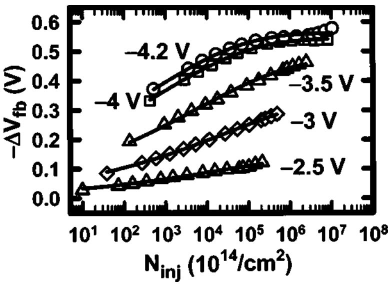

FIG. 2. Dependence of flatband voltage on injected charge density at various stress voltages; symbols are measured data; solid curves are fitting curves.

CVS times. The stress voltage was −3.5 V. One observes that the $C-V$ curve gradually shifts toward negative voltage with stress time. This tendency indicates that hole trapping is the predominant process in the gate stack during stressing. However, the negative flatband voltage shift (ΔV_{fb}) may arise from the emergence of positive bulk trapped charges and/or interface charges. To clarify the mechanism responsible for the hole trapping, the conductance of the capacitor is plotted against measuring voltage over several decades of stress time, as shown in Fig. 1(b). It is found that the conductance peak value and shape only change slightly with stress time. This suggests that charge trapping at the interface states does not play any significant role in ΔV_{fb} for the HfO_2/SiO_2 gate stack during CVS.[8] Thus, we conclude that the ΔV_{fb} is mainly caused by hole trappings in the bulk of HfO_2 layer. This result seems to contradict with most previous works, in which electron trappings in the high-k stacks were shown to be the dominant mechanism responsible for the threshold and flatband voltage shifts.[3–6]

To gain further insight into the trapping mechanism, we employ the so-called distributed capture cross-section model or stretched exponential model[2,3] to describe the trapping behavior. The stretched exponential equation is given by $|\Delta V_{fb}|=|\Delta V_{max}|(1-\exp(-N_{inj}\sigma_0)^{\beta})$, where $|\Delta V_{max}|$, σ_0, β are fitting parameters which are related to the total trap density. Here, σ_0 represents the characteristic capture cross section, $|\Delta V_{max}|$ denotes the maximum shift in $|\Delta V_{fb}|$ that occurs after prolonged stressing, and N_{inj} denotes the injected charge density. Figure 2 shows the dependence of ΔV_{fb} on N_{inj}. It can be clearly seen that the fitting curves (i.e., solid curves) match very well with experimental data (i.e., symbols) over several decades of N_{inj}. In addition, $|\Delta V_{fb}|$ saturates at larger N_{inj} when the magnitude of the stress voltage is higher than $|-3.5\ \mathrm{V}|$. These features imply filling existing hole traps in the high-k gate stacks. The β value is around 0.184 for all stressing conditions indicating that hole traps in the high-k gate stacks possess larger distributed capture cross section than that of electron traps (cf., $\beta\sim 0.32$);[1] while σ_0 is nearly independent of voltage and its value is about 1.5×10^{-14} cm^2. Moreover, it is worthy to note that $|\Delta V_{fb}|$ increases again as the N_{inj} is larger than 2×10^{20} cm^{-2} s at $V_g=-4.2$ V. This phenomenon is thought to be due to additional traps creation.

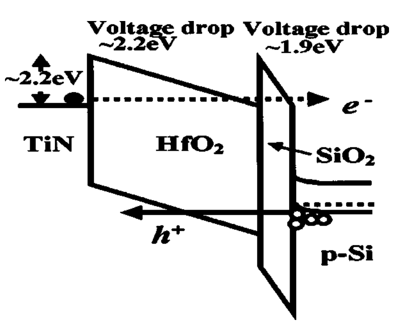

FIG. 3. Energy diagram of HfO_2/SiO_2 gate stack capacitor with midgap TiN metal gate electrode under constant voltage stress ($V_g=-4.2$ V).

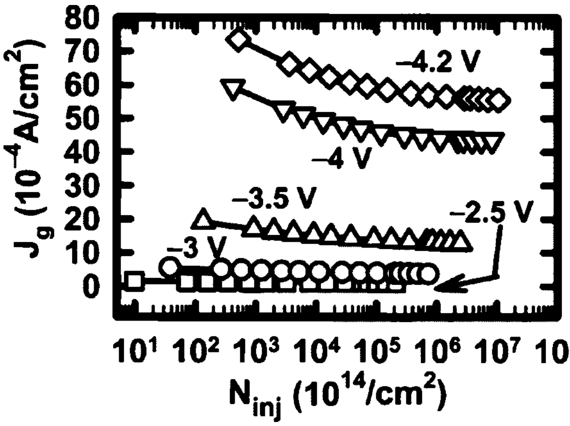

FIG. 4. Gate current density as a function of injection charge density for various stress voltages.

Not disregarding the success of the distributed capture cross-section model in describing the ΔV_{fb} during CVS, it is still necessary to explain why the hole trapping is more likely to occur in our high-k gate stacks. We believe this can be explained by the resultant band diagram of the gate stack under $V_g=-4.2$ V stress, as illustrated in Fig. 3. The parameters, including physical thicknesses, band offsets and the voltage drops across the individual insulators were determined based on our TEM analyses (not shown) and the work function of TiN (~4.8 eV) presented in previous researches.[9,10] It can be seen that the probability of hole tunneling from the substrate is much higher than that of electron tunneling from the gate because of the shorter tunnel distance. Therefore, the leakage current is dominated by hole injection. To reinforce this argument, the characteristics of the gate current density (J_g) as a function of N_{inj} under various CVS conditions (Fig. 4) show that the leakage current decreases with N_{inj} for all stress voltages. This is consistent with hole dominance in the gate stack because only the trapped holes can cause leakage increase if the electron current is dominant component.

In conclusion, hole trappings are firmly observed in the HfO_2/SiO_2 gate stack with TiN metal gate electrode. The δV_{fb} caused by the trapped holes can be well described by adopting distributed capture cross-section model over several decades of stress time during CVS. This phenomenon is attributed to the resultant asymmetric band structure, which favors hole tunneling from the substrate and, in turn, makes the gate stack more susceptible to the hole trapping.

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[1] B. H. Lee, R. Choi, L. Kang, S. Gopalan, R. Nieh, K. Onishi, Y. Jeon, W.-J. Qi, C. S. Kang, and J. C. Lee, Tech. Dig. - Int. Electron Devices Meet. **2000**, 39.
[2] S. Zafar, A. Callegari, E. Gusev, and M. Fischetti, J. Appl. Phys. **93**, 9298

(2003).

[3] M. Krishnan and V. Kol'dyaev, IEEE Reliability Physics Symposium Proceedings, 2002.

[4] W. J. Zhu, T. P. Ma, S. Zafar, and T. Tamagawa, IEEE Electron Device Lett. **23**, 597 (2002).

[5] E. P. Gusev and C. P. D'Emic, Appl. Phys. Lett. **83**, 5223 (2003).

[6] A. Kerber, E. Carter, L. Pantisano, M. Rosmeulen, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, IEEE Reliability Physics Symposium Proceddings, 2003, p. 41.

[7] J. R. Hauser and K. Ahmed, AIP Conf. Proc. **449**, 235 (1998).

[8] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 1982).

[9] J. Westlinder, T. Schram, L. Pantisano, E. Cartier, A. Kerber, G. S. Lujan, J. Olsson, and G. Groeseneken, IEEE Electron Device Lett. **24**, 550 (2003).

[10] G. S. Lujian, T. Schram, L. Pantisano, J. C. Hooker, S. Kubicek, E. Rohr, J. Schuhmacher, O. Kilpela, H. Sprey, S. D. Gendt, and K. D. Meyer, Proceedings ESSDERC. 2002.