

Electromigration failure mechanisms for SnAg 3.5 solder bumps on Ti Cr - Cu Cu and Ni (P) Au metallization pads

T. L. Shao, Y. H. Chen, S. H. Chiu, and Chih Chen

Citation: Journal of Applied Physics 96, 4518 (2004); doi: 10.1063/1.1788837

View online: http://dx.doi.org/10.1063/1.1788837

View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/96/8?ver=pdfcov

Published by the AIP Publishing

Articles you may be interested in

Study of electromigration-induced Cu consumption in the flip-chip Sn Cu solder bumps J. Appl. Phys. **100**, 083702 (2006); 10.1063/1.2357860

Interaction of single pentacene molecules with monatomic Cu Cu (111) quantum wires

J. Vac. Sci. Technol. B 23, 1726 (2005); 10.1116/1.1942508

Increase of the thermoelectric power factor in Cu Bi Cu, Ni Bi Ni, and Cu Bi Ni composite materials J. Appl. Phys. **97**, 103722 (2005); 10.1063/1.1895468

Transmission electron microscopy based study of epitaxy in Nb (100) Cu bilayer and Cu Nb (100) Cu trilayer nanoscale films

Appl. Phys. Lett. 86, 051904 (2005); 10.1063/1.1850195

Electromigration of eutectic SnPb and SnAg 3.8 Cu 0.7 flip chip solder bumps and under-bump metallization J. Appl. Phys. **90**, 4502 (2001); 10.1063/1.1400096



Re-register for Table of Content Alerts

Create a profile.



Sign up today!



Electromigration failure mechanisms for SnAg3.5 solder bumps on Ti/Cr-Cu/Cu and Ni(P)/Au metallization pads

T. L. Shao, Y. H. Chen, S. H. Chiu, and Chih Chen^{a)}
Department of Material Science & Engineering, National Chiao Tung University, Hsin-chu 300, Taiwan, Republic of China

(Received 19 March 2004; accepted 9 July 2004)

The electromigration behavior of SnAg3.5 solder bumps is investigated under the current densities of 1×10^4 A/cm² and 5×10^3 A/cm² at 150° C. Different failure modes were observed for the two stressing conditions. When stressed at 1×10^4 A/cm², damage occurred in both the anode/chip side and the cathode/chip side. However, failure happened only in the cathode/chip side under the stressing of 5×10^3 A/cm². A three-dimensional simulation of the current-density distribution was performed to provide a better understanding of the current-crowding behavior in the solder bump. The current-crowding effect was found to account for the failure in the cathode/chip side. In addition, both the temperature increase and the thermal gradients were measured during the two stressing conditions. The measured temperature increase due to Joule heating was as high as 54.5° C, and the thermal gradient reached 365° C/cm when stressed by 1×10^4 A/cm². This induced thermal gradient may cause atoms to migrate from the chip side to the substrate side, contributing to the failure in the anode/chip side. Moreover, the formation of intermetallic compounds in the anode/chip side may also be responsible for the failure in the anode/chip side. © 2004 American Institute of Physics. [DOI: 10.1063/1.1788837]

I. INTRODUCTION

With the increasing environmental concerns, the micro-electronics industry is paying greater attention to lead-free solder alternatives. One of the most promising alternatives is the SnAg3.5 solder for flip-chip packages, and manufactured SnAg3.5 solder bumps on a wafer by electrical plating or printing technology is now commercially available. Furthermore, the input/output pin count of flip-chip products has dramatically increased recently. In addition, bump pitch has decreased rapidly, so the contact area of the solder bumps and the diameter of the under bump metallization (UBM) continues to shrink. Therefore, electromigration of the Pb-free solder bumps has become an important issue, ^{1,2} and it needs urgently to be studied.

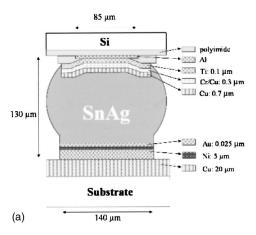
Previous studies on the electromigration of flip-chop solder bumps were mainly focused on eutectic SnPb solders.³⁻⁷ The current-crowding effect on the cathode/chip side was proposed to be responsible for the failure at the cathode/chip side of the SnPb bumps. ^{1,6} A two-dimensional simulation has been carried out to depict the current-density distribution in solder bumps. Recently, efforts have been made on the electromigration of Pb-free solder bumps. 8,9 The current crowding induced by electromigration still plays a crucial role in the failure of the bumps. In addition, thermomigration due to the thermal gradient in the flip-chip solder joints is considered to account for the void formation on the anode/chip side. However, concerning the SnAg3.5 flip-chip solder bump on Ti/Cr-Cu/Cu UBM and Ni(P)/Au pad, little research has been made on the failure mechanism due to electromigration. We found that three failure modes occurred in this system when the solder bumps were stressed by $5 \times 10^3 A/cm^2$ and by $1 \times 10^4~A/cm^2$. The goel of this paper is to investigate the electromigration mechanisms of SnAg3.5 flip-chip solder bumps. In addition, since electromigration is the result of a combination of the thermal and electrical effects on mass motion, a three-dimensional (3D) simulation on current-density distribution was performed to provide a better understanding of the current-crowding behavior in the solder joints. Furthermore, the temperature increase and the temperature gradients due to the current stressing in the solder bumps were measured to examine the thermal effect on the migration of atoms. Possible failure mechanisms responsible for the three failure modes are proposed.

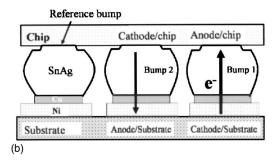
II. EXPERIMENT

The flip-chip packages of SnAg3.5 solder bumps were prepared as follows: The chip's size was 9.5×6.0 mm with a 105- μ m UBM diameter. The UBM consisted of $0.7~\mu$ m Cu, $0.3~\mu$ m Cr-Cu, and $0.1~\mu$ m Ti. A SnAg3.5 solder paste was printed and deposited on the UBM pad of the chip. The chip was reflowed in a nitrogen atmosphere oven at the 250°C peak temperature and remained above the liquid temperature for approximately 60 s. Then, the bumped die sample was prepared after sawing.

Afterward, the bumped die was mounted on a BT substrate, on which the SnAg3.5 solder paste was printed through a metal stencil printing on the metallization pads of the substrate. Then, the flip-chip sample was reflowed for the second time in a nitrogen atmosphere oven at the 250°C peak temperature for approximately 60 s. The flip-chip joints were formed after the second reflow. Afterward, the flip-chip package was under filled. The schematic diagram of the flip-chip sample is shown in Fig. 1(a). In this paper, we refer to

a) Author to whom correspondence should be addressed; electronic mail: chih@cc.nctu.edu.tw





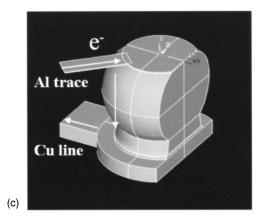
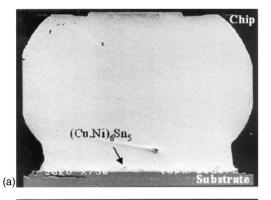


FIG. 1. Schematic diagrams of the bumps used in this study: (a) Crosssectional view showing the structure of a SnAg bump. (b) Schematic diagram of the bumps during current stressing. The directions of the electron flow are indicated by arrows in the figure. (c) Schematic diagram of the bump for temperature and thermal gradient measurement, in which 97% of the solder remains. An infrared microscope was used to measure the temperature increase and the thermal gradient on the polished surface.

the right bump as Bump 1, in which the electron flow goes from the board side to the chip side, whereas the middle bump is Bump 2, in which the electrons migrate from the chip side to the board side. The direction of the electron flow during the current stressing is indicated by the arrows in Fig. 1(b).

To measure the temperature increase in the solder joints due to the current stressing, a solder bump was polished laterally until the contact opening was visible, with approximately 97% of the mass of the bump remaining, as shown in Fig. 1(c). The current stressing of the specimen was performed on a hot plate in ambient air, which has a heating capacity of up to 120°C. The specimen was powered by



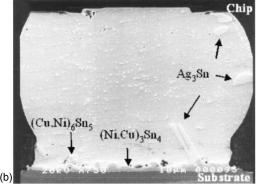


FIG. 2. (a) Cross-sectional SEM image of an as-prepared SnAg solder bump. (b) Cross-sectional SEM image of a SnAg bump aged at 150°C for 20 h.

various currents on a hot plate maintained at 70°C. Prior to the current stressing, the emissivity of the specimen was calibrated at 70°C. After the calibration, the bumps were powered by the desired currents. Then measurement was performed to record the temperature distribution after the temperature reached a stable state. The temperatures in the solder joints were detected by a QFI thermal infrared microscopy, which has a 0.1°C temperature resolution and a $2-\mu m$ spatial resolution.

To prepare the plan-view specimens for observation by the scanning electron microscope (SEM), the samples were grounded either from the substrate side or the chip side until there was about 10-µm-thick solder left. Then, an etching solution consisting of glycerin, nitric acid, and acetic acid at a ratio of 1:1:1 was used to selectively etch the tin. Thus, the morphology of intermetallic compound (IMC) and the whole contact opening could be observed clearly after the selective etching. Microstructure and composition were examined by a Joel 6500 field-emission SEM and energy dispersive spectroscopy (EDS), respectively.

III. RESULTS

Figure 2(a) shows the cross-sectional SEM image of a solder bump without thermal annealing and current stressing. IMCs of (Cu, Ni)₆Sn₅ were found on the interface of the solder and the metallization layer in the substrate side. However, there were no obvious IMCs observed in the vicinity of the UBM on the chip side. Figure 2(b) depicts the bump microstructure after thermal annealing at 150°C for 20 h. IMCs of (Ni, Cu)₃Sn₄ formed at the interface of the solder





FIG. 3. Plan-view SEM images showing the morphology of the contact openings on the chip side for (a) an as-prepared SnAg solder bump and (b) a SnAg bump aged at 150°C for 20 h. Ternary compound of Ni, Cu, and Sn were found after the aging.

and the Ni pad in the substrate side after the solid-state aging. Furthermore, several large Ag_3Sn particles were observed in the bulk solder, as seen in Fig. 2(b). A slight amount of $(Cu,Ni)_6Sn_5$ IMC in the solder bump near the substrate side was occasionally observed. Again, no large amount of Cu-Ni-Sn IMC was seen in the chip side.

To examine the microstructure evolution on the contact opening of the chip side after the current stressing, the SnAg solder was etched selectively to allow a plan-view observation of the contact, which can provide more information on the failure mechanism when the electromigration damage occurs in the UBM. In addition, the IMC formation on the contact opening can be clearly observed because the etchant does not etch the Cu-Ni-Sn IMCs and the UBM. Figure 3(a) depicts the plan-view SEM image of the contact opening on the chip side when the SnAg solder was etched away, and the whole contact opening can be clearly seen. The inner circle is the contact opening for the solder bump connecting to the Al trace on the chip side. No obvious IMCs were found to attach to the UBM. Figure 3(b) shows the plan view of the chip side that was only thermally annealed at 150°C for 20 h. Several IMCs were observed after the thermal annealing, as indicated by the arrow in Fig. 3(b). The EDS results indicated that they consisted of Sn, Ni, Cu, and Cr. The Ni atoms may migrate from the substrate side during the annealing process.

Surprisingly, both the anode/chip and the cathode/chip sides of the SnAg bumps may be damaged after the current



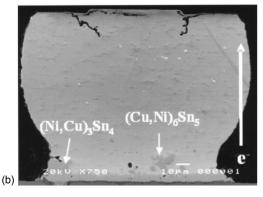


FIG. 4. Cross-sectional SEM image after the current stressing of $1 \times 10^4 \text{ A/cm}^2$ at $150\,^{\circ}\text{C}$ for 22 h (a) for Bump 2 and (b) for Bump 1. Voids formed on both the cathode/chip and anode/chip sides.

stressing by 1×10^4 A/cm² at 150°C. However, the damage may occur on both sides or only on one of them. The current density was calculated based on the area of contact opening on the chip side. In these packages, the contact opening was 85 μ m in diameter on the chip side, whereas it was 150 μ m in diameter for the pad opening on the substrate side. Thus, the current density on the chip side was about three times larger than that of the substrate side. Therefore, electromigration damage generally occurs on the chip side. Figure 4 shows the cross-sectional SEM images of the bump pairs after the current stressing by 1×10⁴ A/cm² at 150°C for 22 h. Open failure occurred after the current stressing, and voids formed near the chip sides of the bump pairs. On the anode/chip side, as shown in Fig. 4(a), voids/cracks can be observed near the UBM. In addition, IMCs of (Ni,Cu)₃Sn₄ can be detected below the UBM, as indicated by one of the arrows in the figure. On the cathode/substrate side, the IMCs also grew larger. Some IMCs inside the solder were determined to be (Cu, Ni)₆Sn₅. On the cathode/chip side, as shown in Fig. 4(b), voids are also found inside the solder below the UBM. Furthermore, the voids on the right side are bigger than those on the left side. The IMCs on the anode/ substrate side grew bigger. Elemental EDS mapping of Ti, Cr, Cu, and Ni were performed for the bump pairs, as shown in Fig. 5. The UBM layers for both bumps were damaged, and Ni and Cu atoms were detected accumulating in the solder near the center of the UBM on the anode/chip side. The Ni atoms had migrated from the substrate to the chip side in the same direction as the electron flow. Since the thermal gradient in the bump drove the atoms from the chip side to the substrate side, the electrical field could be the major

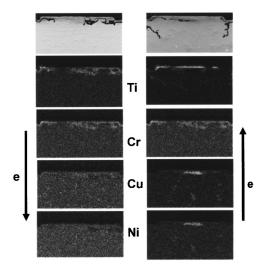


FIG. 5. Elemental EDS mappings of Ti, Cr, Cu, and Ni for the bump pairs in Fig. 5. Ni and Cu atoms accumulated on the anode/chip side.

driving force causing Ni atoms to migrate from the substrate side to the chip side. However, the Cu atoms may have come from the UBM either on the chip side or from the substrate side, since part of the Ni layer in the substrate side was damaged.

Plan views for the contact opening on the chip side were prepared to investigate the failure mechanism. Figure 6 shows the microstructures of the contact openings of another bump pair that failed after the current stressing of $1 \times 10^4 \, \text{A/cm}^2$ at $150\,^{\circ}\text{C}$ for 22 h. Both contact openings for

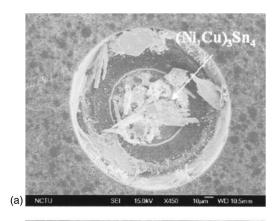
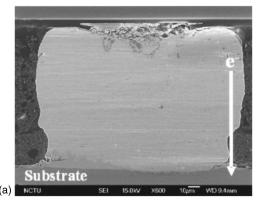




FIG. 6. Plan-view SEM images depicting the morphology of the contact openings after the stressing of $1\times10^4~{\rm A/cm^2}$ at $150\,{\rm ^{\circ}C}$ for 22 h (a) on the anode/chip and (b) on the cathode/chip side. IMCs formed on both sides.



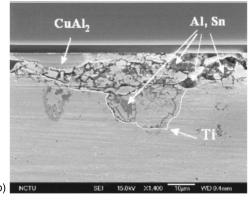


FIG. 7. Cross-sectional SEM images for the bumps after current stressing of $5 \times 10^3 \ A/cm^2$ at $150 \, ^{\circ}\text{C}$ for 218 h (a) for bump 2, in which electrons drifted downward and (b) for the enlarged image on the cathode/chip side.

the anode/chip and the cathode/chip sides were clearly shown after the selective etching of Sn. On the anode/chip side, as seen in Fig. 6(a), many IMCs formed at the contact opening and their composition is close to (Ni,Cu)₃Sn₄. However, on the cathode/chip side, dendritelike IMCs can be observed, with the composition close to (Cu,Ni)₆Sn₅. Compared with the reference bumps, it is concluded that the formation of (Ni,Cu)₃Sn₄ and (Cu,Ni)₆Sn₅ was mainly due to the current stressing because few IMCs formed in the reference bump. The morphology of dendritelike IMCs indicates that both (Ni,Cu)₃Sn₄ and (Cu,Ni)₆Sn₅ have highly anisotropic surface energy and that the solder may have melted. We shall discuss this point in Sec. IV.

To investigate the failure mechanism at a lower current density, another set of bump pairs was stressed by 5 $\times 10^3$ A/cm² at 150°C. In this set, failure occurred only in the cathode/chip end of the bump, whereas no noticeable damage was observed for the anode/chip side. Figure 7(a) shows the cross-sectional SEM image on the failure site after a 192-h current stressing. The UBM collapsed, and some of the SnAg solder filled in where the UBM had been located. The EDS analysis is shown in Fig. 7(b), indicating that the Al pad and the UBM were embedded into the solder. The IMCs of CuAl2 formed at the location where the Al pad had situated, as indicated in the figure. The plan views for another set of failed bump pairs are seen in Fig. 8. On the contact opening of the anode/chip side, no obvious damage was observed except for the mixing of Al and Cr atoms in the lower part of the opening, as seen in Fig. 8(a). Neverthe-

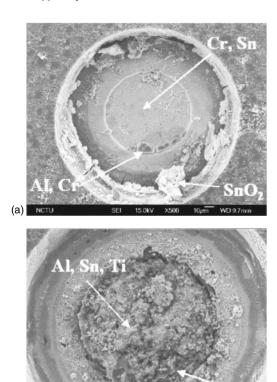


FIG. 8. Plan-view SEM images showing the morphology of the contact opening after stressing by $5\times10^3~{\rm A/cm^2}$ at $150\,^{\circ}{\rm C}$ for 218 h (a) on the anode/chip side and (b) on the cathode/chip side. Failure occurred at the cathode/chip side.

less, the contact opening on the cathode/chip side was destroyed completely, and the rough interface consisted of Al, Sn, Cr, and Ti, as shown in Fig. 8(b).

To examine the Joule heating effect on the failure mechanism, both the temperature increase and the thermal gradient were measured for the two stressing conditions. Figure 9(a) and 9(b) show the temperature increase and the thermal gradient, respectively, when the package was stressed at 1×10^4 A/cm²(0.59 A). The measured temperature increase in the solder was as high as 54.5°C. In addition, the temperature increase due to Joule heating slightly depended on the testing temperature. It decreased approximately by 5°C when the testing temperature increased from 70 to 100°C. Therefore, although the testing temperature was maintained at 150°C, the real temperature inside the solder might be over 200°C. The thermal gradient under the stressing condition was measured to be 369°C/cm. In contrast, when the package was stressed at 5×10^3 A/cm², the average temperature increase was detected to be 9.1°C and its thermal gradient became 127°C/cm.

IV. DISCUSSION

A. Failure mechanisms

Multiple driving forces may trigger the migration of atoms in the SnAg bumps during current stressing. According to the electromigration theory, ^{10,11} voids form at the cathode and extrusions or hillocks accumulate at the anode. Thus, open failure occurs at the cathode side. However, in SnAg

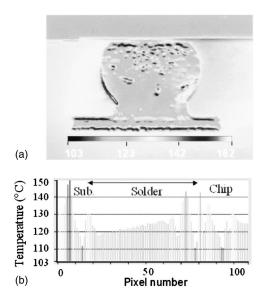


FIG. 9. (a) Temperature distribution in the SnAg bump when stressed at $1 \times 10^4 \text{ A/cm}^2$ at 70°C . The temperature increase due to the current was 54.5°C (b) The corresponding temperature profile along the dashed line in (a), showing a thermal gradient of 365°C cmacross the bump.

bumps, open failure happend not only in the cathode end but also in the anode side, which implies that other failure mechanisms may take place during the current stressing. During the current stressing of flip-chip solder bumps, the following two driving forces may operate due to their unique geometry and composition and thus, influence their electromigration behavior.

1. Electrical effect of current crowdling on electromigration

Current-crowding plays a critical role in the electromigration failure of the solder bump, because the current density in the Al trace is typically one or two orders in magnitude larger than that in the solder. 1,6 Current crowding occurs in the junction of the Al trace and the solder bump. However, current-density distribution in the flip-chip bumps is a threedimensional issue. Figure 10 depicts the current-density distribution by simulation of the solder joint. The 3D tilt view of the current-density distribution is shown in Fig. 10(a), in which a 0.59 A was applied. The corresponding current density in the Al trace is 9.8×10^5 A/cm², and the calculated average current density in the contact opening of the chip side is 1.0×10 A/cm². However, current crowding occurs at the entrance point of the Al trace into the solder bump. The maximum current density inside the solder is as high as 1.8×10^5 A/cm², as seen in the cross-sectional view along the Z axis in Fig. 10(b). On the substrate side, the currentcrowding phenomenon is much less due to the larger contact opening. Figure 10(c) illustrates the current-density distribution on the contact opening in the chip side. The red area close to the entrance into the solder bump represents the region with a high current density and the most vulnerable area in the joint during electromigration testing.

Void formation caused by current crowding can be observed in Fig. 4(a), in which the electron flow entered the bump from the right-back side. Significant flux divergence

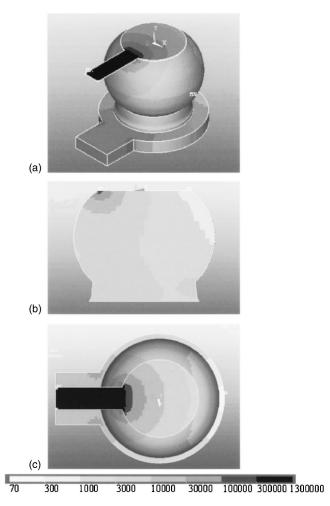


FIG. 10. Three-dimensional simulation of current-density distribution in a SnAg bump when powered by 0.59 A. (a) Tilt view of the current-density distribution for the whole joint. Current densities in the Al trace, solder bump, and Cu line are labeled in the figure. (b) Current-density distribution in the cross section along the dashed line in (a). (c) Top view showing the current-density distribution in the contact opening on the chip side. Current crowding occurs in the vicinity of the junction of the Al trace and the solder bump.

occurred in this area, causing a void formation in the vicinity of the entrance point. In addition, the IMC formation in Fig. 6(b) also demonstrates the current-crowding effect on electromigration. The electrons entered the bump from the location of the root of the IMCs situated on the chip side, going vertically to the paper plane toward the substrate, and then flowed downward to the Cu line. Thus, the growth direction of the IMCs matches the current-crowding path. This path can be seen in Fig. 10(b) and indicates that it is from the top-left corner downward to the bottom-left corner. Thus, current crowding plays a key role in the damage formation in the cathode/chip end.

2. Thermal effect of Joule beating on electromigration

During the current stressing in flip-chip package, Joule heating may cause a temperature increase and result in a thermal gradient. The former raises the testing temperature higher than the ambient temperature, resulting in a higher diffusion rate for the materials in the bumps. The latter produces another driving force for atomic migration, which may

trigger a failure mechanism other than the current-crowdinginduced failure. As shown in Fig. 9(a), the temperature increase when stressed at $1 \times 10^4 \,\mathrm{A/cm^2}$ was as high as 54.5°C, which means that the real testing temperature may be over 200°C. Thus, formation of many IMCs during the current stressing occurred on the anode/chip side, as shown in Fig. 6(b). Furthermore, prior to the failure, the temperature in the bump may exceed its melting point, causing local melting or the melting of the whole bump. It is reported that the SnAgCu solder bumps may have melted upon failure when they were stressed with a current density of 2 $\times 10^4 \ A/cm^2$ at $100 \, ^{\circ} C.^{12}$ Thus, it is hypothesized that the dendritic IMCs in Fig. 6(b) might be formed in the liquid state, since dendrite growth occurs only in the liquid state.¹³ Hence, it is worthy to note that the testing condition of 150° C and 1×10^{4} A/cm² may be too stringent for the SnAg solder, which has a melting point of 221°C.

In addition, this temperature increase will affect the measurement of the mean-time-to-failure (MTTF), which is typically expressed as ¹⁴

$$MTTF = A \frac{1}{j^n} \exp\left(\frac{Q}{kT}\right),$$

where A is constant, j is the current density, n is a model parameter for current density, Q is the activation energy, k is the Bolzmann's constant, and T is the average bump temperature. The real temperature in the solder during high-current stressing is much higher than the testing temperature. So the measured value of MTTF could be underestimated.

The thermal gradient drives the atoms from the chip side to the substrate side, leaving voids near the UBM on the chip side. Since the temperature in the solder near the chip side is higher than that in the substrate side, the jumping frequency of the solder in the chip side is higher, causing a net atomic flux from the chip to the substrate side. 15 Hopkins et al. reported that thermal migration may assist electromigration in the cathode/chip side and may oppose electromigration in the anode/chip side. The measured thermal gradient was 369° C/cm when stressed at 1×10^4 A/cm², which may contribute to the formation of voids in the anode/chip side, as seen in Fig. 4(b). On the other hand, when the bumps were stressed by 5×10^3 A/cm² at 150 °C, failure occurred only in the cathode/chip side. The average temperature increase was detected to be 9.1 °C at the current density, and its thermal gradient decreased to 127°C/cm, as seen in Fig. 9. Therefore, both the temperature increase and the thermal gradient effects became less profound and thus, current crowding dominated the failure mechanism at the lower current density.

V. CONCLUSIONS

Electromigration-induced failure in SnAg3.5 solder bumps has been investigated under the current densities of 1×10^4 A/cm² and 5×10^3 A/cm² at $150\,^{\circ}$ C. When stressed at 1×10^4 A/cm², failure may occur on both the anode/chip and the cathode/chip sides. Joule heating became very serious under the 1×10^4 A/cm² current stressing, causing a temperature increase of $54.5\,^{\circ}$ C in the solder and a thermal

gradient of 365°C/cm across the solder bump. Thermal migration due to the built thermal gradient and volume expansion due to the IMCs formation may account for the void formation on the anode/chip side under the stressing of $1\times 10^4~A/cm^2$. Three-dimensional simulation on current-density distribution supported the contention that current-crowding effect was considered to be responsible for the failure on the cathode/chip side. This is because for the solder bumps stressed under $5\times 10^3~A/cm^2$, migration of Al atoms in the Al trace may contribute to the UBM failure in the cathode/chip side.

ACKNOWLEDGMENTS

The authors would like to thank Professor D.J. Yao in National Tsing Hua University for the temperature measurement and Professor K. N. Tu at UCLA for the helpful discussions, and the National Science Council of R. O. C. for the financial support of this study through Grant No. 90-2216-E-009-042. In addition, the simulation assistance from the National Center for High-Performance Computing (NCHC) in Taiwan is appreciated.

- ¹K. N. Tu, J. Appl. Phys. **94**, 5451 (2003).
- ²K. N. Tu and K. Zeng, Mater. Sci. Eng., R. **R34**, 1 (2001).
- ³S. Brandenburg and S. Yeh, *Proceedings of Surface Mount International Conference and Exhibition, SM198, San Jose, CA, 23-27 August 1998* (San Diego, CA, 1998), pp. 337–344.
- ⁴C. Y. Liu, C. Chen, C. N. Liao, and K. N. Tu, Appl. Phys. Lett. **75**, 58 (1999).
- ⁵J. D. Wu, P. H. Zheng, K. Lee, C. T. Chiu, and J. J. Lee, *Proceedings of the 52nd Electronic Components and Technology Conference, ECTC 2002, San Diego, CA, 28 May 2002* (San Diego, CA, 2002) pp. 452–457.
- ⁶E. C. C. Yeh, W. J. Choi, K. N. Tu, P. Elenius, and H. Balkan, Appl. Phys. Lett. **80**, 580 (2002).
- ⁷H. Ye, C. Basaran, and D. Hopkins, Appl. Phys. Lett. **82**, 7 (2003).
- ⁸T. Y. Lee, D. T. Frear, and K. N. Tu, J. Appl. Phys. **90**, 4502 (2001).
- ⁹S. Y. Jang, J. Wolf, W. S. Kwon, and K. W. Paik, *Proceedings of the 52nd Electronic Component and Technology Conference, ECTC 2002, San Diego, CA, 28 May 2002* (San Diego, CA, 2002) pp. 1213–1220.
- ¹⁰I. A. Blech, J. Appl. Phys. **47**, 1203 (1976).
- ¹¹R. Landauer and J. W. F. Woo, Phys. Rev. B **10**, 1266 (1974).
- ¹²Y. C. Hsu, T. L. Shao, C. J. Yang, and C. Chen, J. Electron. Mater. 32(11), 1222 (2003).
- ¹³D. A. Porter and K. E. Easterling, *Phase Transformations in Metals and Alloys*, 2nd ed. (Chapman & Hall, London, 1992), p. 220.
- ¹⁴J. R. Black, IEEE Trans. Electron Devices **ED-16** (4), 338 (1969).
- ¹⁵P. Shewmon, *Diffusion in Solids*, 2nd ed. (The Minerals, Metals & Material Sociey, Warrendale, PA, 1989), Chap. 5.