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PAPER

Substrate Pick-Up Impacting on ESD Performances of Cascode NMOS Transistors

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SUMMARY The cascode NMOS architecture has been tested by the Human Body Model (HBM), Machine Model (MM) and Transmission Line Pulse Generator (TLP) in this paper. For the TLP, detailed silicon data have been analyzed well in many parameters, such as the first triggering-on voltage (Vt1), the first triggering-on current (It1), the holding voltage (Vh), and the TLP I-V curve. Besides the above three kinds of Electrostatic Discharge (ESD) events, the device gate oxide breakdown voltage is also taken into consideration and the correlations between HBM, MM and TLP are also observed. In order to explain the bipolar transistor turning-on mechanisms, two kinds of models have been proposed in this paper. In typical cases, substrate resistance decreases as the technology advances. On the one hand, for processes older than the 0.35 μm process, such as 0.5 μm and 1 μm, ESD designers can use pick-up insertions to trigger integrated circuits (IC) turn on uniformly. The NPN Side Model can dominate ESD performances in such old processes. On the other hand, in 0.18 μm and newer processes, such as 0.15 μm, 0.13 μm, 90 nm, etc., ESD designers must use non-pick-up insertion structures. The NPN Central Model can dominate ESD performances in such processes. After combining both models together, the bipolar turning-on mechanisms can be explained as "ESD currents occur from side regions to central regions." Besides ESD parasitic bipolar transistor turning-on concerns, another reason that ESD designers should use non-pick-up insertions in deep sub-micron processes is the decreasing of the gate oxide breakdown voltage. As IC size scales down, the gate oxide thickness lessens. The thinner gate oxide thickness will encounter a smaller gate oxide breakdown voltage. In order to avoid gate oxide damage under ESD stresses, ESD designers should endeavor to decrease ESD device turn-on resistances. ESD protecting devices with low turn-on resistances can endure larger currents for the same TLP voltage. In this paper, silicon data show that the non-pick-up insertion cascode NMOS transistor's turning on resistance is smaller than the pick-up insertion cascode NMOS transistor's turning on resistance. Although this paper discovers NPN turning-on mechanisms based on the cascode NMOS structure, ESD designers can adopt the same theories for other kinds of ESD protecting structures, such as one single poly Gate-Grounded NMOS transistor (GGNMOST). ESD designers can use pick-up insertion architecture for NMOS transistors in the low-end processes, but utilize the non-pick-up insertion architecture for GGNMOST in the high-end processes. Then they can obtain the optimized ESD performances.

key words: *ESD*

1. Introduction

This paper discusses positive-type substrate pick-up locations impacting on IC ESD performances of cascade GGNMOST. There are two kinds of substrate pick-up architectures, the pick-up insertion and the non-pick-up insertion, taken into consideration. After evaluating ESD data, both structures have similar HBM and MM behaviors. However, there is an enormously different TLP triggering-on behavior so ESD turn-on mechanisms based on TLP testing data are proposed. Furthermore, one conclusion is created to identify what kinds of processes IC designers should use for pick-up insertions and what kinds of processes they should use only for one pick-up surrounding.

The power reduction is a main driving force in integrated circuits. The clearest sign of this trend is the reduction of standard power supply voltage VDD from 5 V to 3.3 V [1] in the 0.35 μm process. During a long transition period, both 5 V and 3.3 V digital ICs are used. This poses several problems for the direct interface between two chips; the two power supplies may switch on with mutual delay, 5 V output ICs will drive 3.3 V inputs and vice-versa. The solutions have been published in [2] for problems that may occur when a 5 V output buffer drives a 3.3 V bi-directional bus driver. In that paper, the cascode NMOS structure can be found to solve voltage reliability issues.

The cascode NMOS structure is widely used for high voltage tolerant applications. For the 3.3–5 V compatible I/O circuit, the cascode NMOS structure can endure 5 V input from the external chips even though IC is made only with the 3.3 V thin gate oxide process [3]. In half-micron VLSI's, power supply voltage has been changed from 5 V to 3.3 V or to a lower voltage for reducing the power consumption and ensuring the sufficient reliability [4]. There are only circuit function studies in the above papers. In this paper, the cascode NMOS structure will be evaluated for ESD performances in detail.

The MOSFET design in high performance CMOS technologies is driven primarily by performance requirements and reliability issues such as the hot carrier degradation. These requirements generally lead to processes that are inherently weak in terms of ESD and Electrostatic Overstress (EOS) [5]. From ESD design points of views, ESD protecting devices must have both functions of normal-off and ESD-on. Here, "normal-off" means that ESD circuits must be turned off at IC normal operations. "ESD-on" stands for that ESD circuits must be turned on when ESD events come into ICs.

In order to make each ESD protecting device have the same function, the pick-up insertion into source regions is a necessary design practice [6]. However, on the contrary, ESD designers possibly arrange pick-up regions as only one guard ring outside all the protecting devices for increasing the base resistance in the parasitic lateral bipolar transistor [7]. The above two theories have a different point of

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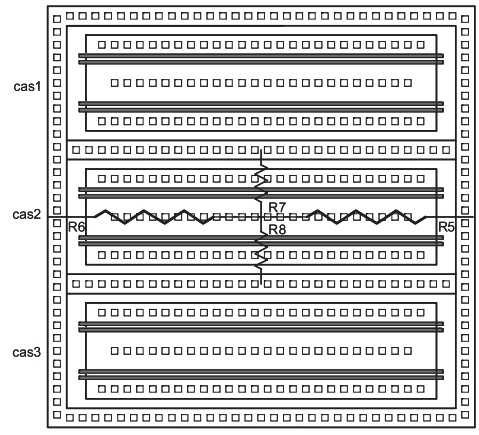

Fig. 1 (Structure A): The layout of the cascode NMOS structure with three cells and the pick-up insertion.

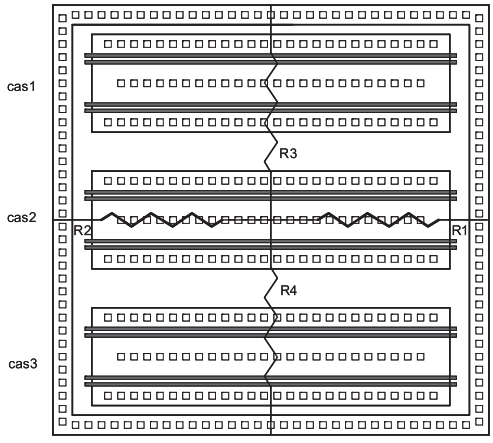

Fig. 2 (Structure B): The layout of the cascode NMOS structure with three cells and without the pick-up insertion.

view. One uses pick-up insertions into source regions, but the other one does not allow pick-up insertions into source regions. However, it's accepted to have different results for the same circuits in different processes from ESD points of view. The contradiction and consistence will be explained in next sections.

ESD designers often use the substrate pick-up insertion, such as the structure A in Fig. 1. The ESD device channel length is larger than $0.35\,\mu$m in the $0.35\,\mu$m process and older processes. When the channel length is smaller than $0.18\,\mu$m in the advanced processes, there are new ESD rules used in IC fabrications. Due to the parasitic bipolar turning-on concerns [7], the pick-up insertion is not allowed any more, such as the structure B in Fig. 2.

This paper discusses pick-up effect in the $0.35\,\mu$m silicon process. ESD device turning on mechanisms are discussed in detail. In order to explain ESD behaviors clearly, two tentative ESD turning on mechanisms are proposed in this paper. After analyzing silicon data, one kind of ESD turning on mechanism is adopted to explain ESD protecting events in this experiment.

Wafer level ESD testing is the only methodology to discover ESD performances in this paper. The package level testing is not involved. Both HBM and MM events are utilized to examine the effects of pick-up insertions impacting on IC at first. Then TLP measurements are applied on transistors for characterizing their ESD behaviors. There are several useful data obtained from transistor I-V measurements of the TLP system. The first ones are the drain breakdown condition data which relate to the bipolar transistor snapback and illustrate the triggering-on voltage Vt1 and the triggering-on current It1. The next feature of interest is the snapback voltage, V_{SB}, the minimum voltage at which the bipolar snapback can be maintained (equal to Vh, holding voltage in this paper). The final interest of TLP I-V curve is the second breakdown point, indicating the secondary breakdown current It2 and the secondary breakdown voltage Vt2. The relative values of Vt2 and Vt1 are also of great interests in [8]. All the silicon data are collected in Sect. 3.

In Sect. 4, two models for ESD device turning on mechanisms are proposed. One model is the bipolar turning on from sidewalls of the device and the other model is the central bipolar turning on from the central regions of the device. These two models can explain why different kinds of substrate pick-up insertions dominate on different technology ESD devices.

In Sect. 5, the theory applied in this experiment is discussed in detail. One kind of bipolar turning on mechanism is derived for this experiment. Furthermore, the correlations between three kinds of ESD stressing methodologies (HBM, MM and TLP) are taken into consideration.

Finally, the conclusion of this paper is listed in Sect. 6. Both kinds of parasitic bipolar turning on mechanisms are correct. Their differences can be applied for different process technologies. ESD designers should have different pick-up insertion types in different processes if they want to optimize their ESD device performances.

2. Cascode NMOS Architecture Experiment

The basic cell of this experiment is the cascode NMOS architecture that has the poly finger width equal to $60\,\mu$m and the poly finger length equal to $0.4\,\mu$m. The structure A layout is shown in Fig. 1 and the structure B layout is shown in Fig. 2. Both structures have the same equivalent circuit, as illustrated in Fig. 3. It includes three parallel cascode NMOS cells named as "cas1," "cas2" and "cas3." There are parasitic diodes existing between PAD1 and PAD2. PAD1 is considered as ESD stressing pad and PAD2 is considered as the grounding pad when ESD testing is processed.

The cross section of the cascode NMOS architecture is illustrated in Fig. 4. The drain side of the top NMOS transistor is connected to PAD1 and the source side of the bottom NMOS transistor is connected to PAD2. The common terminal of the top NMOS transistor and the bottom NMOS transistor is designed as the floating point. There are six poly fingers for top NMOS transistors and bottom NMOS

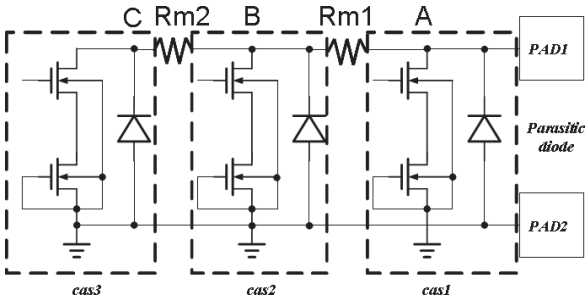

Fig. 3 The equivalent circuit of a cascode NMOS structure.

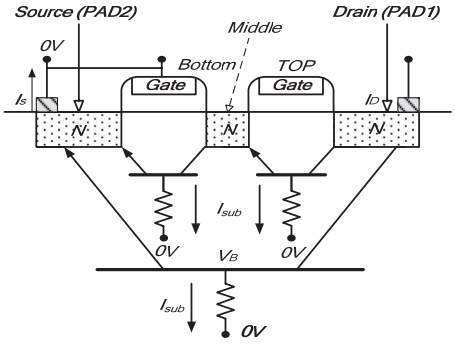

Fig. 4 The cross-section of the cascode NMOS structure shows the current flowing in the lateral NPN bipolar transistor.

transistors shown in Fig. 1 and Fig. 2.

This cascode structure is designed for the gate oxide reliability. It allows 5 V signals entering the IC when only thin gate oxide devices (3.3 V applications) are adopted in this 3.3 V/5 V 0.35 μm IC. The poly gate terminal of the top NMOS transistor is floating, but the poly gate terminal of the bottom NMOS transistor is connected to the ground node (0 V). This design makes sure that the current flowing from PAD1 to PAD2 can be kept in a low value under IC normal operations since the bottom NMOS transistor is always kept off. Before ESD zapping event occurs, we must measure I-V curves to ensure that the off current is very low. In this study, off current is about 0.1 nA under the conditions of PAD1 biased at 3.96 V and PAD2 tied to 0 V. 3.96 V comes from the operation voltage 3.3 V multiplied by a factor 1.2. The ESD testing failure criteria depend on the off current. If the off current reaches a value larger than 1 μA, IC is regarded as "fail."

Both equivalent circuits of with and without pick-up insertion structures are the same, which are shown in Fig. 3. The practical layouts for structures A and B are shown in Figs. 5 and 6, respectively. The pick-up/non-pick-up chip photos are illustrated on the right sides of Fig. 5 and Fig. 6. In this paper, there are contacts between the top NMOS transistor and the bottom NMOS transistor due to the layout historical factor, but the contacts are kept as floating so not to induce extra unexpected effects.

For electrical parameter analyses in Fig. 5, the resistances and currents are shown in the picture. Rm1 illustrates the resistance from terminal A of "cas1"to terminal

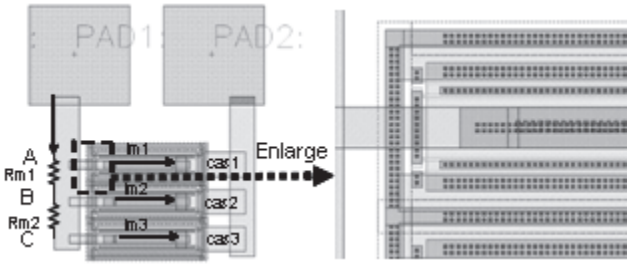

Fig. 5 The real layout for the cascode NMOS structure with the pick-up insertion (Structure A).

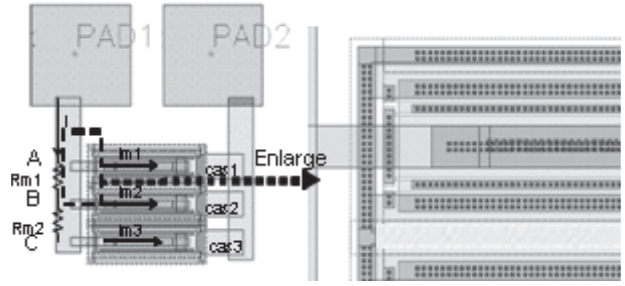

Fig. 6 The real layout for the cascode NMOS structure without the pick-up insertion (Structure B).

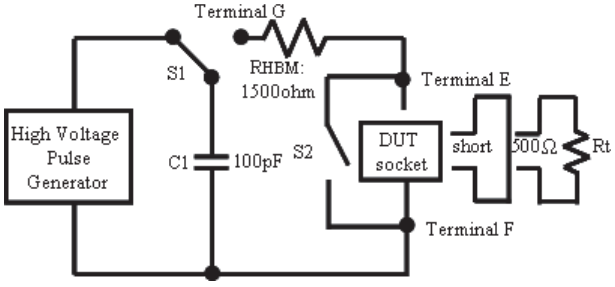

Fig. 7 The typical HBM circuit.

B of "cas2." Similarly, Rm2 means the resistance from terminal B of "cas2" to terminal C of "cas3." Im1, Im2 and Im3 are the currents from PAD1 to PAD2 through "cas1," "cas2" and "cas3," respectively. The same parameters are also applied in Fig. 6.

Three IC devices are tested for HBM and MM individually in order to fit ESD testing standards [9], [10] that describe 3 devices for each voltage level of ESD failure thresholds. Fresh IC devices are adopted for positive and negative ESD stresses individually in this study. However, for TLP testing, there is no testing standard to follow up. Two IC devices are chosen for TLP experiments.

As shown in JESD22-A114D, HBM has a capacitor C1 in 100 pF and one resistor R_{HBM} in 1500 Ω, illustrated as Fig. 7. When HBM proceeds, firstly, S1 is switched to the pulse generator. The high voltage pulse generator produces a large voltage and stores charges in capacitor C1. Then, S1 is switched to terminal G. Stored charges in C1 are released to the DUT (Device under Test). For the purposes of waveform calibrations, two kinds of resistances are

adopted. "Short" or "Rt (500 ohm)" is used as the calibration element so there are two kinds of waveforms for different resistances. The waveform details are not included in this paper. Similarly, MM has one 200 pF capacitor as stated in EIA/JESD22- A115-A, illustrated in Fig. 8. One extra resistor R_{MM} is applied to measure MM waveforms.

For TLP, a pulse will travel a finite distance (on coaxial cable) to the device, as shown in Fig. 9. A charging line has a 10-meter coaxial cable to form the 100 ns width pulse. The 10-meter coaxial cable resistance is about 50 Ω. In order to add waveform stabilities, another 50 Ω is utilized as a loading resistor. ESD device resistor (Zdev) could be composed of two elements, device resistor (Rdev), and device capacitor (Cdev). A 500 MHz oscilloscope is adopted to monitor waveforms. The oscilloscope is implemented between two 50 Ω elements so that the cable disturbance could be eliminated. The voltage source is increased in voltage step by step. Before the snapback of ESD device occurs, a smaller voltage step is designed in order to obviously observe the triggering-on voltage. On the one hand, a voltage step equal to 0.5 V or 1 V is used for the first step before ESD device triggering-on phenomenon occurs. On the other hand, a larger voltage step is used to monitor ESD device I-V curve behaviors after the snapback phenomenon occurs. A larger voltage step can be equal to 2 V or 5 V.

The positive voltage is the only voltage source at TLP testing. The negative voltage stressing is not experimented since negative charges are easily dissipated by the parasitic diode. The positive voltage stressing causes the ESD parasitic bipolar transistor to turn on. Record each I-V point with the voltage and the current monitored by the oscilloscope in the TLP equipment. Then I-V curve data can be saved as TLP results.

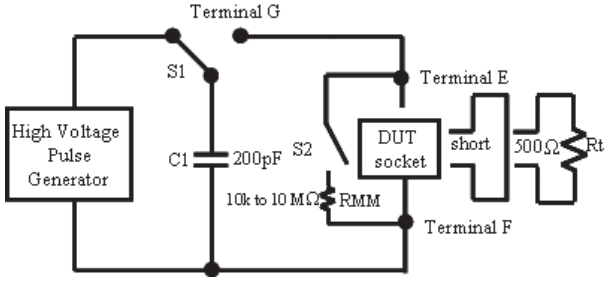

Fig. 8 The typical MM circuit.

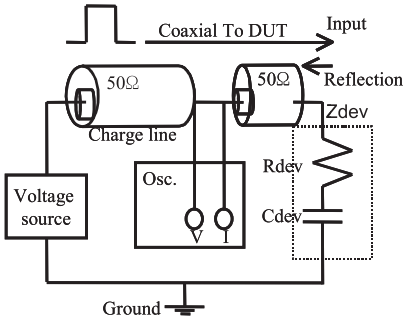

Fig. 9 The equivalent circuit of the device under the TLP.

3. ESD Testing Results

There are HBM and MM results in Tables 1 and 2, respectively. From these two tables, the cascode NMOS architecture can pass HBM +7 kV/−8 kV and MM +450 V/−500 V no matter the device is with or without pick-up insertions. The ESD capabilities are much larger than the typical IC application. For typical applications, company internal testing specifications usually require circuits to have a minimum pass threshold voltage of ±2 kV HBM stress on all pins, as they can be handled in an ESD-protected environment with no significant loss due to HBM-type discharges. For MM testing, typically required withstand voltage levels are ±200 V for regular and ±400 V for increased demands [11].

Table 3 illustrates TLP results of the cascode NMOS structure with pick-up insertions. TLP results of the cascode NMOS structure without the pick-up insertion are shown in Table 4. Figure 10 shows I-V curve results of TLP. There are two tested devices for each structure. Here, Vt1 stands for the first triggering-on voltage with snapback occurring at the first time. The corresponding current of the first triggering-on voltage Vt1 is It1. Similarly, voltages Vt2 and Vt3 represent the second and third turning-on voltages, respectively. The corresponding currents are It2 and It3. After the occurrence of the snapback phenomenon, the I-V curve comes back to the holding voltages (Vh1, Vh2, and Vh3).

At TLP testing, as currents increase, the heat of device would also increase. After device heat reaches the thermal runaway point, the cascode NMOS structure would be damaged permanently. The point has voltage and current records as Vt2 (or Vt4) and It2 (or It4). It2 and Vt2 illustrate the thermal runaway point current and voltage for ESD device without the pick-up insertion, respectively. It4 and Vt4 represent the thermal runaway point current and voltage for ESD device with the pick-up insertion because there are It2 (Vt2) and It3 (Vt3) occurring in such ESD devices. It2

Table 1 HBM and MM performances of a cascode NMOS structure with pick-up insertion (structure A).

ESD events	#1	#2	#3
+HBM	7.5kV	7kV	7kV
- HBM	>8kV	>8kV	>8kV
+MM	450V	500V	500V
- MM	500V	500V	500V

Table 2 HBM and MM performances of a cascode NMOS structure without pick-up insertion (structure B).

ESD events	#1	#2	#3
+HBM	7kV	7kV	7kV
- HBM	>8kV	>8kV	>8kV
+MM	500V	500V	450V
- MM	500V	500V	500V

Table 3 TLP performances of a cascode NMOS structure with pick-up insertion (structure A).

Sample	It1 (A)	Vt1 (V)	Ih1 (A)	Vh1 (V)	It2 (A)	Vt2 (V)	Ron1 (Ω)	Ih2 (A)	Vh2 (V)	It3 (A)	Vt3 (V)	Ron2 (Ω)	Ih3 (A)	Vh3 (V)	It4 (A)	Vt4 (V)	Ron3 (Ω)
#1	0.02	9.83	0.17	6.66	1.20	11.88	5.06	1.36	10.44	2.49	13.90	3.07	2.79	13.56	3.55	15.88	3.03
#2	0.02	9.85	0.17	6.66	1.19	12.10	5.32	1.35	10.82	2.48	13.97	2.78	2.78	13.73	3.50	15.68	2.70

Table 4 TLP performances of a cascode NMOS structure without pick-up insertion (structure B).

Sample	It1 (A)	Vt1 (V)	Ih1 (A)	Vh1 (V)	It2 (A)	Vt2 (V)	Ron (Ω)
#3	0.0147	9.96	0.13	6.21	3.58	16.19	2.89
#4	0.0094	10.23	0.12	6.65	3.59	15.80	2.64

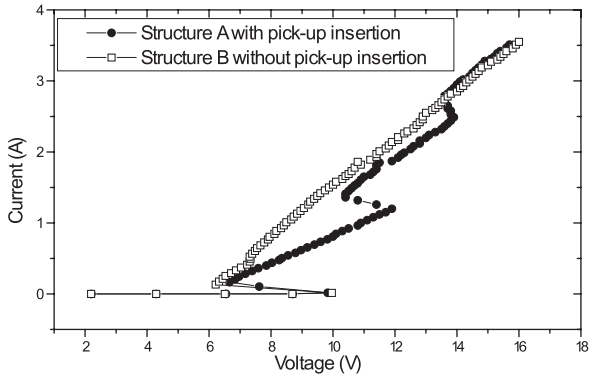

Fig. 10 TLP I-V results of the cascode NMOS structure.

Table 5 The correlation results of HBM, MM and TLP.

Value	Breakdown current (A) (It2 or It4)	It2 x 1500 Ω (kV)	V_HBM (kV)	V_MM (V)
Structure A	3.5	5.25	7	450
Structure B	3.6	5.40	7	450

(Vt2) and It3 (Vt3) own the non-thermal runaway phenomena since there are holding points after them and ESD device off-current does not exceed 1 μA after the second (It2) or third (It3) triggering-on points.

Since there are HBM, MM and TLP silicon data, all the data comparisons are listed in Table 5. On the one hand, −HBM currents would go through the parasitic N+/P-substrate diode. Because the cascode NMOS structure has a large drain side area, forward currents from −HBM stresses can be easily dissipated by ESD devices. This results in the absolute −HBM bypass voltage larger than 8 kV. On the other hand, the parasitic bipolar transistor must turn on to dissipate ESD heat when positive ESD event occurs on PAD1 with PAD2 grounded. The bipolar turning-on mechanism can't dissipate ESD currents well as forward diodes. This results in +HBM pass voltage only about +4.5 kV, not +8 kV.

The pick-up insertion device has three triggering-on points and three holding points. However, ESD device without the pick-up insertion has only one triggering-on point and one holding point. Both kinds of ESD devices have the same TLP thermal runaway current about 3.5 A. The thermal failure threshold is expected to occur at a specific temperature Tcrit for a given device, and can be expressed as (1) is stated in [12].

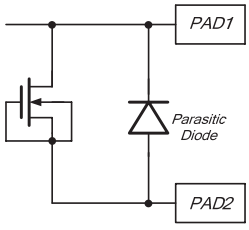

Fig. 11 The equivalent circuit of a gate grounded NMOS (GGNMOS) transistor.

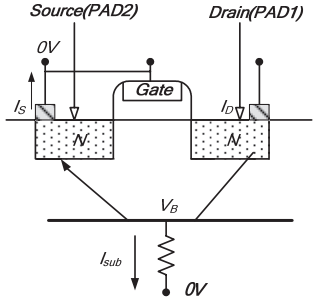

Fig. 12 The cross-section of the gate grounded NMOS transistor shows the current flowing in the lateral NPN bipolar transistor.

$$Pf = It2 * Vt2 \tag{1}$$

Where It2 is the failure current in mA/μm, and Vt2 is the failure voltage, the dissipated power Pf in mW/μm is expected to be a constant for a given technology provided that the LNPN action is not significantly affected by the device layout geometry. The power dissipation of this paper is approximately equal to (2).

$$Pf/\mu\text{m} = 3.5\,\text{A}/360\,\mu\text{m} * 16\,\text{V} = 0.16\,\text{watt}/\mu\text{m} \tag{2}$$

The power dissipation is similar no matter in the pick-up insertion devices or without pick-up insertion devices because the same process and similar layout geometry are used for both structures.

4. Parasitic Bipolar Turn on Mechanism

The current gain β of the LNPN, the drain-substrate multiplication factor M, and the p-substrate resistance Rsub directly relating to the second breakdown trigger current It2 have been evaluated in [12]. GGNMOST has been studied in that paper, such as Figs. 11 and 12.

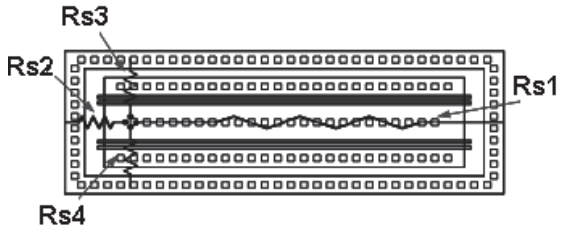

Fig. 13 (NPN Side Model). The layout for the turning-on structure at the side of a cascode NMOS structure with the equivalent resistances.

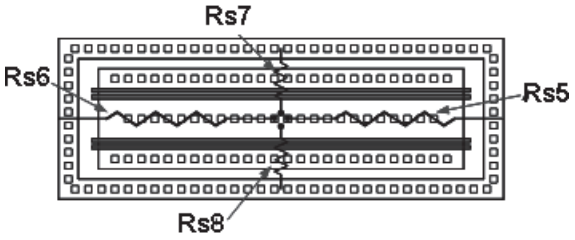

Fig. 14 (NPN Central Model). The layout for the turning-on structure at the center of a cascode NMOS structure with the equivalent resistances.

Since negative voltage stressing is easily dissipated by the forward diode, bipolar transistor turning on mechanism dominates ESD robustness. The bipolar turning on mechanism involves: (1) Holes generated by impact ionization in the depletion region of the drain flow into the substrate as the substrate current Isub. (2) Isub raises the P-substrate potential due to Isub flowing through the substrate resistance. (3) As a result, this voltage drop causes forward bias of the substrate-to-source junction. (4) Then the source inject electrons enter the substrate. (5) When part of the injected electrons survive without recombination with holes in the P-well, it will be pulled into the depletion region of the drain, and result in more impact ionization which causes more holes flowing into the substrate [6].

In Fig. 4, three bipolar devices are observed for structures A and B. However, in Fig. 10, there is only one triggering on point in the structure B. This illustrates that the NPN (drain-psub-middle) bipolar and the NPN (middle-psub-source) bipolar do not dominate parasitic bipolar turning-on behaviors of the cascode NMOS architecture. Namely, there is only one bipolar turning on for one cascode NMOS structure.

Furthermore, what is the first turning on mechanism? In Fig. 13, a simple NPN turning on model (NPN Side Model) is proposed: (1) Substrate resistances can be represented simply by Rs1, Rs2, Rs3 and Rs4. (2) The first turning on point is at the edge of the NMOS transistor drain region, near the substrate pick-up region. (3) The bipolar turning on operation would be majored by Rs2.

In Fig. 14, another simple NPN turning on model (NPN Central Model) is proposed: (1) Substrate resistances could be represented simply by Rs5, Rs6, Rs7 and R8 (2) The first turning on point is at the center of the NMOS transistor drain region, far away from the substrate pick-up region (3) The bipolar turning on is based on the total equivalent devices. (4) The equivalent resistance is shown as follows.

$$\frac{1}{Rsub} = \frac{1}{Rs5} + \frac{1}{Rs6} + \frac{1}{Rs7} + \frac{1}{Rs8} \tag{3}$$

From Tables 3 and 4, the first triggering-on voltage of the cascode NMOS structure with the pick-up insertion is similar to that without the pick-up insertion. If the mechanism follows the NPN Central Model, the structure B's substrate resistance will be larger than the structure A's resistance. In other words, structure B should obtain a smaller turning on voltage. However, the first triggering-on voltage of structure A is similar to that of structure B. It means that the mechanism should follow the NPN Side Model. The substrate current flows through Rs2 to make substrate voltage (V_B) larger than the bipolar turning on voltage. Then the snapback event occurs.

The similar occurrence can be found in [6]. It shows that maximum current (or power) density of the device under ESD zapping event is located at the region near the P-well pick-up region for conventional multi-finger structures. In this paper, the first turning-on point happens at the left side edge of the cascode NMOS structure since metal routing is from the left side of cascode NMOS structures, such as Fig. 5 and Fig. 6.

5. Discussion and Application

In Table 3, for the structure A, the second triggering-on voltage (Vt2) is larger than the first triggering-on voltage (Vt1) in 2 V and the third triggering-on voltage (Vt3) is larger than the second triggering-on voltage (Vt2) in 2 V. Why are the three triggering-on voltages different? From Fig. 5, it can be simply explained as the below.

According to the KCL law, the total currents are equal to the summation of Im1, Im2, and Im3. Im1 is the current flowing through "cas1." Im2 is the current flowing through "cas2." Thus, the value of Im2 is equal to (It2−Ih1=1.03 A). Besides, the voltage difference between two triggering-on voltages Vt2 and Vt1 is equal to Im2*Rm1 (=2 V). Then the metal resistor Rm1 between cas1 and cas2 is equal to 2 Ω.

Similarly, Vt3−Vt2=Im3*Rm2 and Im3=It3−Ih2. Im3 is defined as the current flowing through cas3 and approximates to 1.13 A. The voltage difference between two triggering-on voltages Vt3 and Vt2 is about 2 V. Then the metal resistor Rm2 between cas2 and cas3 is equal to 2 Ω. The existence resistors Rm1 and Rm2 can be the reasons to have three triggering-on points of the structure A. Here, Rm1 and Rm2 can represent "cas2" and "cas3" turn-on resistors, not only the metal resistors.

Furthermore, on the one hand, the structure A obtains a larger first turn-on resistance (Ron1>5 Ω) than the structure B's resistance. For structure A, the first cascode NMOS cell "cas1" turns on firstly and then, the second cascode NMOS cell "cas2" can be turned on after ESD devices reach the second triggering-on point. Then, the third cascode NMOS cell "cas3" is turned on after ESD device voltage exceeds the third triggering-on voltage. Hence, the structure A can reach

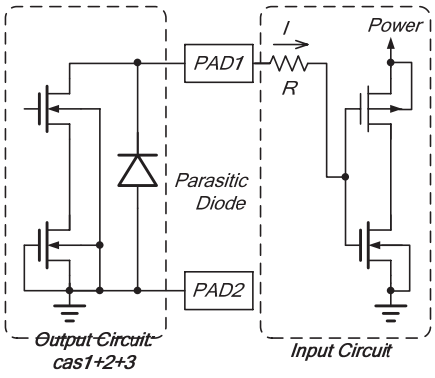

Fig. 15 The simple input/output circuit with the cascode NMOS structure.

ESD uniform turning-on characteristics to bypass ESD currents after all the three cascode NMOS cells are adequately turned on. This phenomenon is not like the double snapback event described in [13]. The double snapback occurs in one MOS transistor with only one parasitic bipolar transistor in that paper, but there are three cascode NMOS cells in this paper.

On the other hand, the structure B has only one turning-on resistance (2.5–3 Ω) because the parasitic bipolar transistor can be turned on at full p-type substrate regions although Rm1 and Rm2 still exists in the structure B. This phenomenon is unlike structure A that is confined by the inserted pick-up regions. The structure B can follow the NPN Side Model to obtain a similar triggering-on voltage value as structure A's value. However, the structure B has a large turning-on areas once the applied voltage reaches the snapback voltage.

In order to discuss an ESD impact on ICs, ESD protecting devices with being protected input circuits are illustrated in Fig. 15. Normally, there is one transmission NMOS transistor before the inverter gate terminal. However, this paper focuses on ESD protections, not I/O signal transmissions so the transmission NMOS transistor is ignored. The current entering gate oxides of the inverter should be very low (no voltage drop on the input resistance R) since gate leakage currents are very low in the 0.35 μm process. TLP data are taken into account for protecting gate oxides. When the structure A and the structure B voltage reaches 12 V, the current reaches 1.2 A and 2.1 A, respectively. The maximum DC breakdown voltage for 65 Å (about equal to the 0.35 μm device gate oxide thickness) is about 12.37 V [14]. This means that the structure B will protect gate oxides well, but structure A will not protect gate oxides well because the structure B owns a larger TLP current at 12 V. However, the gate oxide breakdown voltage should depend on TLP results, not DC measurements [14]. The gate oxide breakdown voltage could reach 18.34 V at TLP stresses in [13]. It implies that there will be no gate oxide damage risks for HBM and MM in this study because the thermal runaway breakdown voltage is around 16 V (<18 V).

Although ESD performances of both structures A and B are almost the same in this paper, for avoiding the non-uniform ESD currents and power distributions in conventional multi-fingers structure NMOS transistors [6], the structure A is recommended in the 0.35 μm process.

On the contrary, the parasitic bipolar turning-on mechanism would follow the NPN Central Model in the 0.18 μm process. The substrate resistance of 0.18 μm process has been degraded a lot than that of the 0.35 μm process. The NPN Central Model can obtain the maximum equivalent resistance, such as Fig. 14 (the central point can obtain the maximum Rs5/Rs6).

This is because the edge point can't be easily turned on in a low substrate resistance. The equivalent substrate resistance of central finger is the largest because the distance from its channel region to the guard ring is the longest in layout [7].

After comparing HBM, MM and TLP testing results, Eqs. (4)–(7) are applied, derived from [15], [16].

$$V_{HBM} = I_{t2} * (R_{HBM} + R_s) \tag{4}$$

$$R_s = \frac{\sum_{i=1}^{m} [V_{HBMi} - R_{\mathrm{HBM}} * I_{t2i}] * I_{t2i}}{\sum_{i=1}^{m} (I_{t2i})^2} \tag{5}$$

$$V_{MM} = I_{t2} * R_{SM} \tag{6}$$

$$R_{SM} = \frac{\sum_{i=1}^{m} V_{MMi} * I_{t2i}}{\sum_{i=1}^{m} (I_{t2i})^2} \tag{7}$$

V_{HBM} and V_{MM} are HBM and MM pass voltages, respectively. It2 (or It4) is thermal run away current. The definitions of resistances in the above equations are: R_{HBM} is the typical HBM resistor equal to 1.5 kΩ, R_S is HBM compensation resistor and R_{SM} is MM compensation resistor. We can obtain R_S = 468.87 Ω and R_{SM} = 126.57 Ω in this study.

The miscorrelation between HBM, MM and TLP can be found in [17], but the correlation between HBM, MM and TLP exists in this research since we can obtain R_S and R_{SM}. Furthermore, a large resistor might have a large resistor vibration so a large substrate resistor has a large R_S. MM has a very small typical resistor so there is a smaller R_{SM} (compared to R_S). The small typical MM resistor implies adding a small resistor can increase MM performances a lot.

ESD designers can create ESD device layout architectures in a large substrate resistance as shown in Fig. 16. This picture illustrates two cascode NMOS cells that each cell has two cascode NMOS transistors. The pick-up is inserted into the middle region of two cascode NMOS cells. The spacing from the NMOS central region to the right, left, top and bottom guard ring is the same. ESD devices can obtain a big substrate equivalent resistor, then resulting in a smallest triggering-on voltage and a better ESD performance. Nevertheless, this kind of layout will cost a huge layout area. In practice, it is not a good layout method.

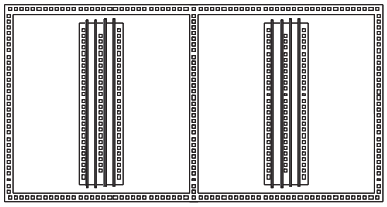

Fig. 16 Two cascode NMOS structure cells with square type p-substrates (not to scale).

6. Conclusion

In old processes (before 0.35 μm processes), ESD designers must use pick-up insertions to uniformly trigger on lateral bipolar transistors. However, in the processes which are after 0.18 μm, ESD designers are recommended to use non-pick-up insertions to trigger on lateral bipolar transistors. The first principle of ESD device design is to turn on lateral bipolar transistors. If the substrate resistor is not big enough to turn on lateral bipolar transistors, pick-up insertions are not allowed.

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