# Electrostatic Discharge Protection Design for High-Voltage Programming Pin in Fully-Silicided CMOS ICs

Ming-Dou Ker, *Fellow, IEEE*, Wen-Yi Chen, *Student Member, IEEE*, Wuu-Trong Shieh, and I-Ju Wei

***Abstract*—For integrated circuits (ICs) with voltage programming pin ($V_{PP}$ pin), a voltage higher than the normal power supply voltage of internal circuits is applied on the $V_{PP}$ pin to program the read-only memory (ROM). Because of the high programming voltage, the ESD diode placed from I/O pad to $V_{DD}$ cannot be applied to such $V_{PP}$ pin. In this work, a new ESD protection design is proposed to improve ESD robustness of $V_{PP}$ pin with the consideration of the mistriggering issue when $V_{PP}$ programming voltage has a fast rise time. In collaboration with the N-well ballast layout, the new proposed ESD protection design implemented in an IC product has been verified in a fully-silicided CMOS process to successfully achieve a high human-body-model ESD protection level of 5 kV.**

***Index Terms*—Electrostatic discharge (ESD), voltage programming pin ($V_{PP}$).**

## I. Introduction

ONE-TIME PROGRAMMING (OTP) read-only memory (ROM) has been widely implemented in micro-controllers (MCUs) [1]. To successfully program the memory cells, a high voltage (HV) on the voltage programming pin ($V_{PP}$ pin) is necessary to induce channel hot electrons or to burn out the fuse [2], [3]. Because the programming voltage ($V_{PP}$) is higher than the normal operating voltage ($V_{DD}$) of internal circuits, current paths from the $V_{PP}$ pin to the $V_{DD}$ power supply line are not allowable. With the forbidden current path from $V_{PP}$ pin to $V_{DD}$ power supply line, the $V_{PP}$ pin poses a stringent challenge in electrostatic discharge (ESD) protection design.

ESD-induced failure has been one of the most serious reliability issues affecting yields of IC products. As a result, on-chip ESD protection circuits have been an essential design in present-day ICs [4]. Dedicated process steps or mask layers for ESD protection such as silicide blocking (SB) are often omitted in CMOS ICs to reduce the fabrication cost [5]–[8]. Without the SB on ESD protection devices, fully-silicided ESD protection MOS field-effect transistors (MOSFETs) have been reported with poor ESD robustness [4], [8]. An efficient ESD protection design for fully-silicided ICs with the voltage programming pin is therefore a highly challenging reliability issue to IC designers [9], [10].

In this work, a new ESD protection design for fully-silicided $V_{PP}$ pin is proposed, which includes a circuit design to avoid the mistriggering of the ESD protection device during the programming conditions when $V_{PP}$ has a fast rise time. The proposed ESD protection design has been successfully verified on a commercial IC product with OTP memory cells in a 0.35 $\mu$m fully-silicided CMOS process.

Manuscript received July 31, 2010; revised November 10, 2010; accepted November 15, 2010. Date of publication January 06, 2011; date of current version January 28, 2011. This paper was approved by Associate Editor Domine M. W. Leenaerts. This work was supported by ELAN Microelectronics Corporation, Taiwan, and supported in part by the Ministry of Economic Affairs, Taiwan, under Grant 99-EC-17-A-01-S1-104, and in part by the "Aim for the Top University Plan" of National Chiao-Tung University and Ministry of Education, Taiwan, R.O.C.

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Digital Object Identifier 10.1109/JSSC.2010.2096114

## II. Design Considerations of Voltage Programming Pins

### A. OTP Memory Cells

To electrically program the OTP memory cells, Fig. 1 depicts the required bias conditions on the memory unit (nMOS cell) which has a control gate and a floating gate. Before programming, there is no charge or only a few charges in the floating gate. The original threshold voltage of a non-programmed nMOS cell is defined as $V_{t0}$. $V_{t0}$ is smaller than 5 V so that the nMOS cell can be turned on (channel can be induced) when the control gate is biased at 5 V [Fig. 1(a)]. To program the nMOS cell, a high gate bias of 12.5 V ($V_{PP}$ voltage) is applied on the control gate and the drain of nMOS cell is biased at $V_{DD}$ of 5 V. With the high gate bias of 12.5 V on the control gate, electrons permitted from the source can pass through the insulating layer beneath the floating gate to be accumulated in the floating gate [Fig. 1(b)]. After a span of field programming time, the 12.5 V $V_{PP}$ voltage is removed and the electrons that accumulated in the floating gate are trapped in the floating gate. The trapped electrons in the floating gate can substantially increase the threshold voltage of the nMOS cell from $V_{t0}$ to $V_{t'}$. As long as the number of electrons trapped in the floating gate is large enough (the programming time is long enough), $V_{t'}$ can be higher than 5 V. Consequently, the channel of nMOS cell can no longer be induced by 5 V gate bias, and the nMOS cell becomes an open circuit after programming, as shown in Fig. 1(c). By exploiting this principle, on-chip memory arrays can be programmed to represent different digital codes to calibrate IC products or to predefine different IC functions to broaden their application scopes [11].

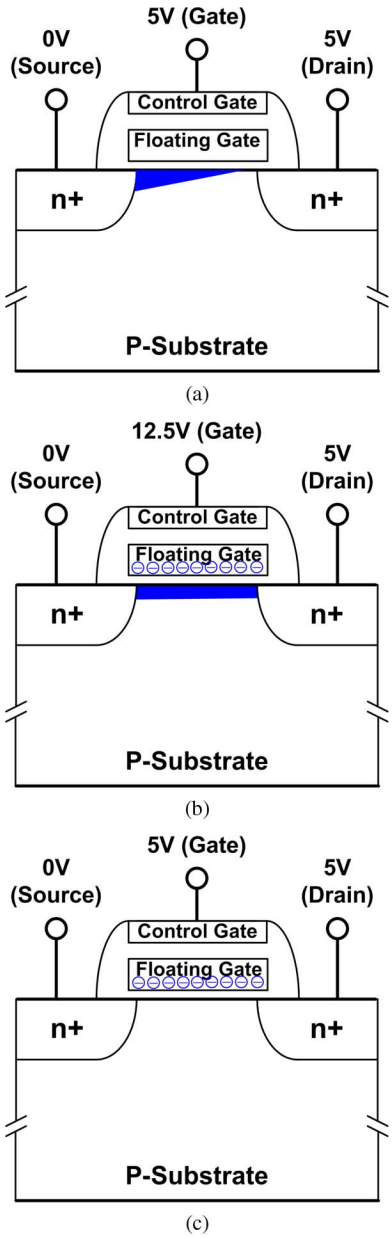


Fig. 1. (a) Normal operating condition of the memory unit before programmed. Channel can be induced under $V_{gs}$ of 5 V and $V_{ds}$ of 5 V. (b) Bias conditions of the memory unit during programming. A high control gate bias of 12.5 V is used to draw channel hot electrons into the floating gate. (c) Normal operating condition of the memory unit after programmed. Channel can not be induced under $V_{gs}$ of 5 V and $V_{ds}$ of 5 V due to the trapped electrons in the floating gate.

### B. $V_{PP}$ Programming Waveforms

To design an ESD protection circuit for voltage programming pins, it is essential to understand the $V_{DD}$ and $V_{PP}$ programming waveforms. The typical measured $V_{DD}$ and $V_{PP}$ programming waveforms are shown in Fig. 2. Under the $V_{PP}$ programming condition, $V_{DD}$ voltage is charged up from 0 V to 5 V before the onset of $V_{PP}$ voltage ramping, so that internal circuits such as control logic or address decoder can function properly. After the $V_{DD}$ voltage has been charged to 5 V, the programmer pulls the $V_{PP}$ voltage high from 0 V to 12.5 V, as shown in Fig. 2.

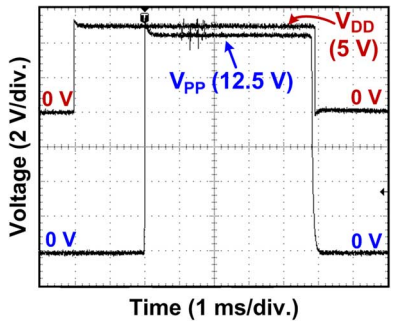


Fig. 2. Measured voltage waveforms on $V_{DD}$ and $V_{PP}$ pins during programming.

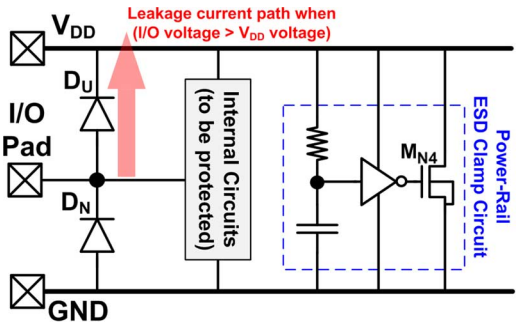


Fig. 3. Traditional whole-chip ESD protection scheme with the power-rail ESD clamp circuit. The diode $D_U$ results in an unwanted leakage current path when I/O voltage is higher than the $V_{DD}$ voltage during some special circuit operating conditions.

To comprehensively protect input/output (I/O) pins against ESD stresses, efficient current paths to discharge ESD stress energy at I/O pins are necessary. Because electrostatic charges may be either positive or negative, there are four ESD test modes at I/O pins with respect to the grounded $V_{DD}$ or $V_{SS}$ (GND) pins. The four ESD test modes are PS (positive-to-$V_{SS}$), PD (positive-to-$V_{DD}$), NS (negative-to-$V_{SS}$), and ND (negative-to-$V_{DD}$) modes [12]. A typical rail-based ESD protection scheme is shown in Fig. 3 [13], [14], where two diodes $D_U$ and $D_N$ are used to divert ESD stress energy at the I/O pad to the $V_{DD}$ or the GND power supply lines. Because the power-rail ESD clamp circuit is especially designed with a large ESD protection device ($M_{N4}$), it is effective to discharge ESD energy between power supply lines [13]–[15]. Through the $D_U$ and $D_N$ diodes in cooperation with the power-rail ESD clamp circuit, the rail-based ESD protection scheme has been reported as an effective method to significantly improve ESD robustness of the I/O pin. However, since the 12.5 V $V_{PP}$ voltage is higher than the 5 V $V_{DD}$ voltage during programming, the diode $D_U$ that diverts the high $V_{PP}$ voltage to the $V_{DD}$ power supply line is prohibited. Otherwise, the memory cells cannot be successfully programmed due to insufficient voltage on the $V_{PP}$ pin. Without the diode $D_U$, the power-rail ESD clamp circuit cannot help discharge ESD energy at the I/O pad under PS- and PD-mode ESD tests. Accordingly, I/O pins without a forward diode from the I/O pad to the $V_{DD}$ power supply line usually have a low ESD protection level, especially under PS- and PD-mode ESD tests. Mixed-voltage I/O buffers where I/O voltages would be higher than their $V_{DD}$ voltages suffer the same limitation, as well [16].

Besides the inability to employ power-rail ESD clamp circuits under PS- and PD-mode ESD tests, the rise time of the programming voltage on the $V_{PP}$ pin ($T_{R,VPP}$) is another design issue that strongly affects the ESD protection design for the $V_{PP}$ pin. Since the $V_{PP}$ programming voltage is externally supplied from a programmer, different programmers may have different driving capabilities, resulting in huge differences between slew rates of programming voltages on the $V_{PP}$ pin. The rise time of the programming voltage on the $V_{PP}$ pin may be as slow as several microseconds [17], or it may be as fast as several tens of nanoseconds in different programming environments [17], [18]. Because the rise time of ESD voltage has the same timescale as that of fast $V_{PP}$ programming voltage (several tens of nanoseconds), some of traditional ESD protection designs could be mistriggered by their ESD trigger circuits. A primary ESD protection pMOS with an *RC* timer to control its gate voltage was reported to protect the programming pin [19]. The *RC* timer should have a time delay over several hundreds of nanoseconds, so that the gate of ESD protection pMOS can be kept low to turn on pMOS during the ESD transition. However, when the rise time of the $V_{PP}$ programming voltage is also in the same scale as that of ESD transient voltage, the simple *RC* timer directly connected to the programming pin cannot distinguish between the normal programming event and the ESD transition event. The ESD protection pMOS in [19] would be turned on both during $V_{PP}$ programming and ESD transition. The turned-on pMOS during the programming event will pull down the $V_{PP}$ voltage to cause a false programming result. Additional modification should be added into the design of [19] to avoid the false programming issue when the programmer provides the $V_{PP}$ programming voltage pulse with a fast rise time. To avoid the mistriggering issue and make ICs comprehensively compatible to programmers from different manufacturers, a wide range of acceptable $V_{PP}$ voltage rise times during programming is requested by customers.

### C. Previous ESD Protection Design for $V_{PP}$ Pin

A previous ESD protection design for the $V_{PP}$ pin used in some IC products is shown in Fig. 4. Without any ESD trigger circuit in this ESD protection design, both the ESD protection devices, the field oxide device (FOD) and the diode $D_N$, are insensitive to the rise time of $V_{PP}$ programming voltage. Under ND- and NS-mode ESD tests, the power-rail ESD clamp circuit and the diode $D_N$ provide effective ESD discharging paths. Under PS-mode ESD test, ESD voltage induces breakdown of the diode $D_N$ to conduct ESD current through the reverse-biased junction of $D_N$. A FOD device is placed between the $V_{PP}$ pin and the $V_{DD}$ line, so that PD-mode ESD energy can be directly discharged to the grounded $V_{DD}$ line through the n-p-n bipolar junction transistor (BJT) inherent in the FOD [20]. Because the diode inherent in the FOD device has a breakdown voltage higher than 12.5 V, the FOD device does not result in current path from the $V_{PP}$ pin to the $V_{DD}$ line during programming. Under PS-mode ESD test, FOD can help divert some ESD energy to the $V_{DD}$ line, and it can be further discharged to the grounded GND through the power-rail ESD clamp circuit. By using this previous ESD protection design, the measured human-body-model (HBM) ESD protection level on the $V_{PP}$ pin is only 2 kV verified in an IC product.

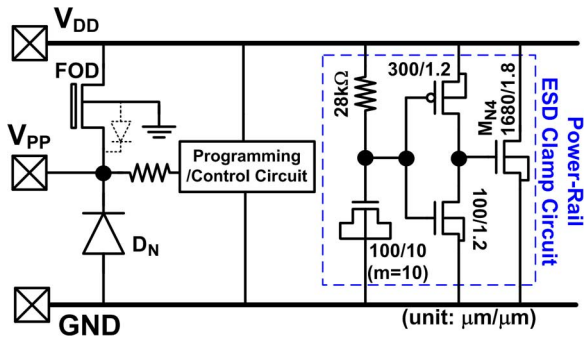


Fig. 4. Previous ESD protection design for $V_{PP}$ pin. It can be safely programmed with fast $V_{PP}$ voltage rise time but has a lower ESD protection level of only 2 kV in HBM.

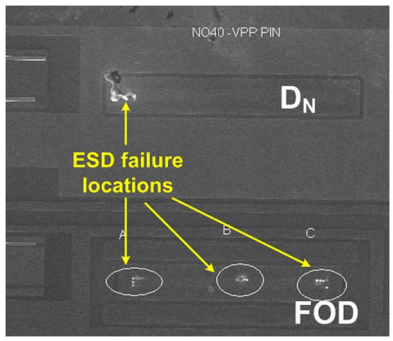


Fig. 5. SEM image of the previous ESD protection design after 2.5 kV PS-mode ESD test. ESD failure locations were found on both the FOD device and the diode $D_N$.

A scanning electron microscope (SEM) image of the previous ESD protection design after 2.5 kV PS-mode ESD test is shown in Fig. 5. ESD failure locations were found on both the FOD device and the diode $D_N$. Failure analysis (FA) verified that the FOD device can help discharge ESD energy under PS-mode ESD test. The previous ESD protection design can provide the typical HBM ESD protection level of 2 kV to the IC product, but the specified HBM ESD protection level has recently been increased from 2 kV to 4 kV by customers with high reliability requirements. Due to the lack of an ESD trigger circuit in the previous ESD protection design, further enlarging the device width of the FOD did not improve the HBM ESD protection level due to the well-known nonuniform triggering phenomenon [21]. Moreover, for cost reduction, silicide blocking (SB) was not used in such IC products. Without SB, severe current crowding phenomena and current filamentation have been reported to further deteriorate the linearity of ESD robustness to the device dimension of an ESD protection device [4]. ESD trigger techniques have been reported to effectively relieve the negative impact on ESD robustness due to silicidation [21]–[23]. Accordingly, with the inability to meet the new requirement of 4 kV HBM ESD protection level by the previous ESD protection design, a new ESD protection design is proposed in this work. The new proposed ESD protection design can not only exploit the ESD trigger technique to achieve high ESD robustness, but also avoid the mistriggering of an ESD protection device under $V_{PP}$ programming voltage with a fast rise time.

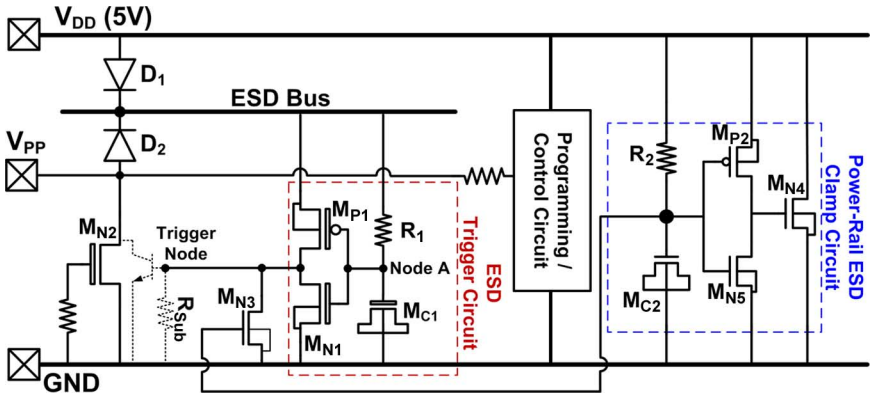


Fig. 6. The proposed ESD protection design for $V_{PP}$ programming pin.

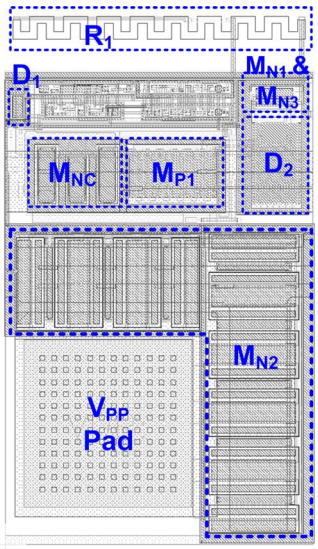


Fig. 7. Layout top view of the proposed ESD protection design for $V_{PP}$ pin, which was realized in a 0.35 $\mu$m fully-silicided CMOS process.

TABLE I
DEVICE DIMENSIONS OF THE PROPOSED ESD PROTECTION DESIGN USED IN THE IC PRODUCT

| | Device Dimension | |
|---|---|---|
| $R_1$ | 28.3 kΩ | – |
| $R_2$ | 28 kΩ | – |
| $M_{C1}$ | 43.5 μm/23 μm | HV Device |
| $M_{C2}$ | 100 μm/10 μm | LV Device |
| $M_{P1}$ | 300 μm/1.2 μm | HV Device |
| $M_{P2}$ | 300 μm/1.2 μm | LV Device |
| $M_{N1}$ | 20 μm/1.2 μm | HV Device |
| $M_{N2}$ | 720 μm/1.2 μm | HV Device |
| $M_{N3}$ | 40 μm/0.35 μm | LV Device |
| $M_{N4}$ | 1680 μm/1.8 μm | LV Device |
| $M_{N5}$ | 100 μm/1.2 μm | LV Device |

## III. NEW PROPOSED ESD PROTECTION DESIGN FOR VOLTAGE PROGRAMMING PINS

The new proposed ESD protection design on $V_{PP}$ pin is composed of a snapback ESD protection device ($M_{N2}$), an ESD trigger circuit ($R_1$, $M_{C1}$, $M_{P1}$, and $M_{N1}$), an ESD bus, two diodes ($D_1$ and $D_2$), and a fail-safe nMOS $M_{N3}$, as shown in Fig. 6. The ESD trigger circuit in the proposed design is connected to the $V_{PP}$ pin through the ESD bus and the diode $D_2$. The output of the ESD trigger circuit is connected to the substrate of $M_{N2}$ to fulfill the substrate-triggered technique [21]. The floor plan of the proposed ESD protection design in an IC product realized in a 0.35 $\mu$m fully-silicided CMOS process is shown in Fig. 7. Device dimensions of the proposed ESD protection design and the power-rail ESD clamp circuit used in the IC product are listed in Table I. In the proposed ESD protection design, $M_{N1}$, $M_{N2}$, $M_{C1}$, and $M_{P1}$ are HV symmetry devices that have thick gate oxide and lightly doped n-drift (for HV nMOS) or p-drift (for HV pMOS) regions at source/drain to sustain the high programming voltage [24], [25].

During normal circuit operating conditions, the $V_{DD}$ pin is biased at 5 V and the $V_{PP}$ pin is either 0 V or 5 V. Through the $D_1$ diode, the ESD bus is charged up to a voltage level close to $V_{DD}$ of 5 V. The resistor $R_1$ passes the voltage on ESD bus to the node A ($V_A$) during normal circuit operating conditions. With the same source voltage and gate voltage on $M_{P1}$, $M_{P1}$ is kept off and the output current from the ESD trigger circuit to the trigger node is 0 A. With the gate of $M_{N2}$ being grounded, $M_{N2}$ is safely kept off during normal circuit operating conditions without interfering I/O signals at $V_{PP}$ pin.

Under $V_{PP}$ programming where the $V_{PP}$ voltage has a slow voltage rise time ($T_{R,VPP}$ in the order of microseconds), voltage on the node A ($V_A$) can follow up the $V_{PP}$ voltage transition because the time delay from $R_1$ and $M_{C1}$ in Fig. 6 is smaller than the $V_{PP}$ voltage rise time. Consequently, $M_{P1}$ is safely kept off when $T_{R,VPP}$ is slow, and $M_{N2}$ is off as well. The proposed ESD protection design therefore does not interfere with $V_{PP}$ programming when $T_{R,VPP}$ is slow. However, when the $V_{PP}$ programming voltage has a rise time as fast as several tens of nanoseconds, $V_A$ can no longer follow up the voltage transition on $V_{PP}$ pin. Because the ESD protection nMOS ($M_{N2}$) in the proposed design is with substrate-triggered design, the amount of substrate-triggered current that flows into the trigger node could turn on parasitic BJT inherent in $M_{N2}$. Accordingly, to suppress the current that may falsely flow into the substrate of $M_{N2}$ during fast $V_{PP}$ voltage rising, a fail-safe nMOS ($M_{N3}$) was added at the output of ESD trigger circuit. The gate of $M_{N3}$ is connected to $V_{DD}$ through the resistor $R_2$ so that $M_{N3}$ is kept on during $V_{PP}$ programming to provide a low-impedance

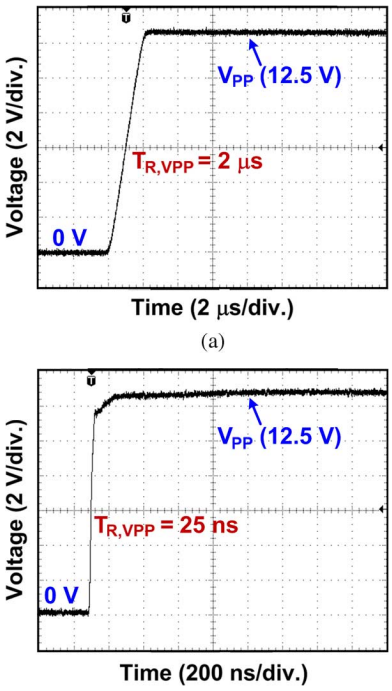


Fig. 8. Measured voltage waveforms on $V_{PP}$ pin during programming with (a) slow $T_{R,VPP}$ of 2 $\mu$s and (b) fast $T_{R,VPP}$ of 25 ns. $V_{DD}$ was biased at 5 V during the tests.

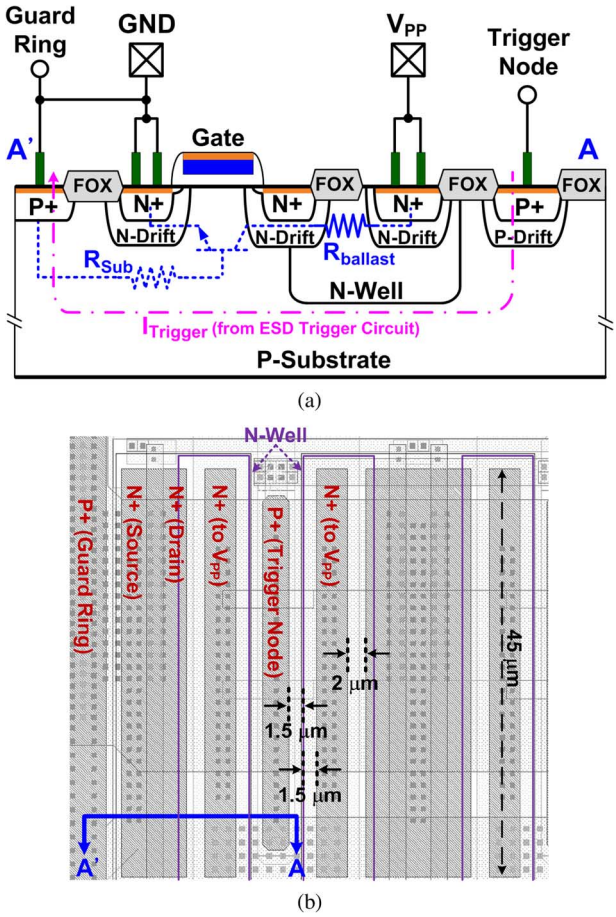


Fig. 9. (a) Device cross-sectional view and (b) layout top view of the high-voltage ESD protection nMOS ($M_{N2}$) with P+ trigger node and the N-well ballast layout realized in a fully-silicided CMOS process.

current path to shunt any $M_{P1}$ output current to ground. $M_{N3}$ can thus stabilize ground potential of the trigger node to prevent $M_{N2}$ from being mistriggered during $V_{PP}$ programming. Because the drain of $M_{N3}$ is connected to the trigger node, parasitic $R_{Sub}$ and body diode of $M_{N2}$ keeps the drain of $M_{N3}$ at a low voltage level. Without a high voltage across $M_{N3}$, it was realized with a low-voltage device to maximize its capability of stabilizing the trigger node during $V_{PP}$ programming with a fast rise time. Moreover, the initial voltage at node A is biased at $V_{DD}$ through the diode $D_1$ and the ESD bus, which reduces the $M_{P1}$ overdrive voltage to suppress the amount of mistriggering current that may falsely flow into the trigger node due to fast $V_{PP}$ programming voltage.

To verify the ability of the proposed design against mistriggering during $V_{PP}$ programming, 0-to-12.5 V voltage pulses with different pulse rise times ($T_{R,VPP}$) were applied to the $V_{PP}$ pin of the IC product realized in 0.35 $\mu$m CMOS process. $V_{DD}$ was biased at 5 V during the tests. Fig. 8(a) and (b) shows the measured voltage waveforms on $V_{PP}$ pin with slow (2 $\mu$s) and fast (25 ns) input voltage rise times, respectively. Both measured voltages on the $V_{PP}$ pin were successfully ramped up to 12.5 V, which has verified that the mistriggering issue of $M_{N2}$ was successfully prevented in the new proposed ESD protection design.

## IV. Implementation and ESD Testing Results

### A. Ballast Layout to Fully-Silicided High-Voltage nMOS

In a multi-finger nMOS, different distances from the drain region of each finger to the grounded guard ring result in asymmetry of substrate resistance ($R_{Sub}$), which causes the central fingers of nMOS to be more easily triggered on under ESD stresses [21]. After triggering of the central fingers under ESD stresses, the ESD overstress voltage is clamped down by these earlier turned-on fingers. Without sufficient ballast resistance, it is highly possible that the central fingers are burned out before the clamped voltage is large enough to trigger the remaining fingers of the nMOS [6], [8]. As a result, ESD current is concentrated in some earlier turned-on area and the rest of the area cannot be triggered on in time to discharge the ESD current. Such nonuniform turn-on behavior among the multiple fingers of nMOS limits its ESD robustness, even if the nMOS was drawn with a large device dimension. By introducing the ballast resistance $R_{\rm ballast}$ to balance the turn-on resistance of the multi-finger nMOS, turn-on uniformity of the multi-finger nMOS during ESD stresses can be improved [6]. Moreover, it has been reported that by increasing the ballast resistance, the ESD current path can be spread deeper into the substrate of a large volume, which in turn improves ESD robustness as well [26]. As a result, sufficient ballast resistance can force ESD current to be conducted into the deeper substrate to have a better heat dissipation, and also increase the ESD robustness due to the improvement of turn-on uniformity among the multiple fingers of nMOS.

Since SB is not used in this work for cost reduction, the N-well ballast layout was applied to adequately increase ballast

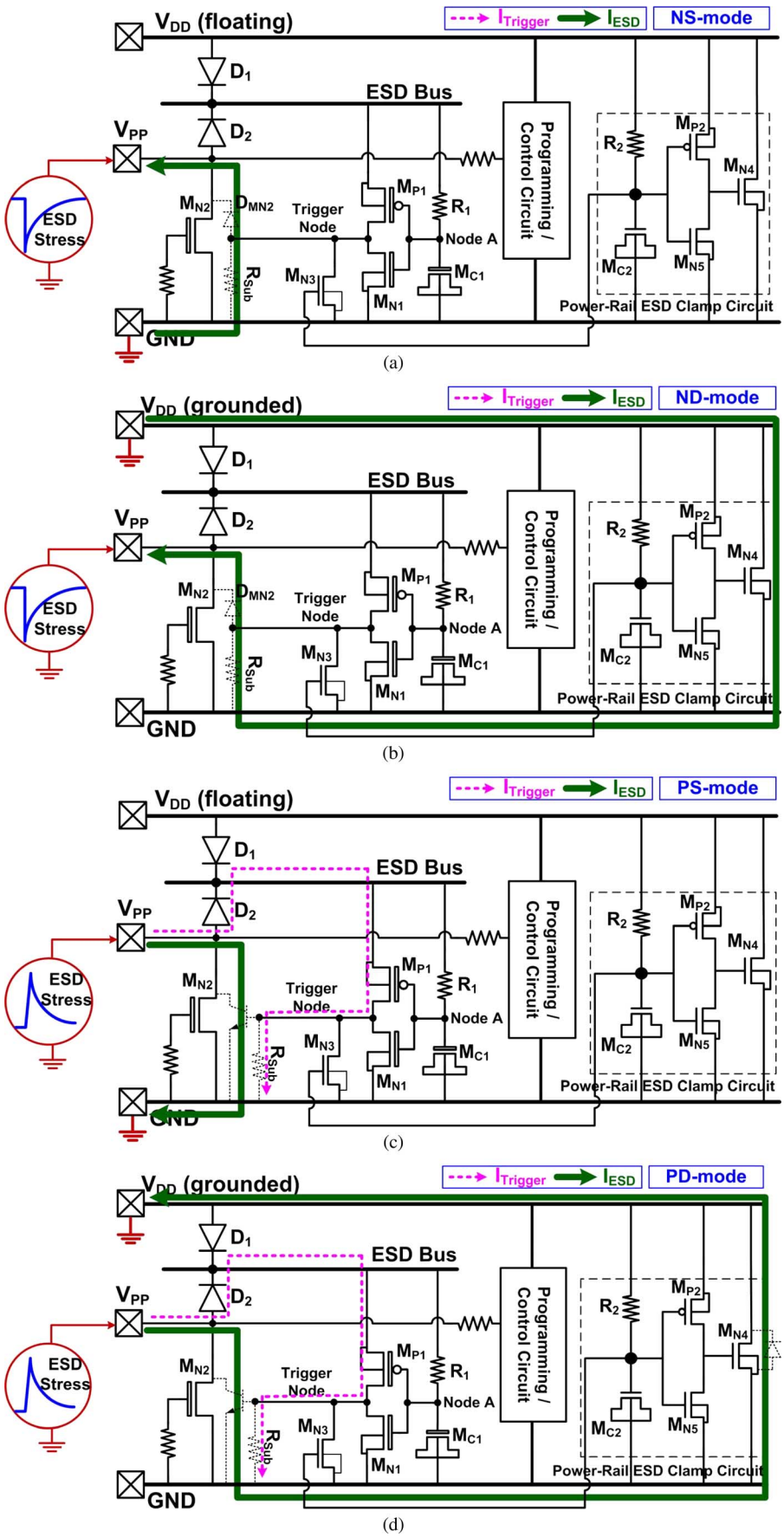


Fig. 10. ESD current discharging path under (a) NS-, (b) ND-, (c) PS-, and (d) PD- mode, ESD test at $\mathrm{V_{PP}}$ pin with the new proposed ESD protection design. The dashed lines denote the substrate-triggered current to trigger on the ESD protection device $\mathrm{M_{N2}}$. The solid lines show the primary ESD current flow.

resistance to $M_{N2}$ without use of the SB [8], [27]. A device cross-sectional view of the fully-silicided high-voltage ESD protection nMOS ($M_{N2}$) with the N-well ballast layout is shown in Fig. 9(a). The drain of $M_{N2}$ is electrically short to the $V_{PP}$ pad through the N-well. With the high sheet resistance of the N-well due to its relatively low doping concentration, the N-well can provide the $R_{ballast}$ to improve ESD robustness of the fully-silicided $M_{N2}$. Moreover, the P+ trigger nodes inserted in the device were short to the output of the ESD trigger circuit (Trigger Node in Fig. 6), so the $M_{N2}$ is implemented with substrate-triggered design to further improve its ESD protection level. A layout top view of $M_{N2}$ is shown in Fig. 9(b). No additional mask layers or process steps are required to implement this ESD device in a fully-silicided CMOS process.

### *B. ESD Discharging Paths*

Current discharging paths of the proposed ESD protection design to protect the $V_{PP}$ pin against the four I/O ESD test modes are illustrated in Fig. 10(a)–(d). Under NS-mode ESD test, the ESD current is discharged through the P-substrate/N+ diode $D_{MN2}$ inherent in $M_{N2}$ [Fig. 10(a)]. Under ND-mode ESD test, the ESD current is discharged through the power-rail ESD clamp circuit, the GND line, and the $D_{MN2}$ [Fig. 10(b)]. Because the $D_{MN2}$ is efficient in discharging ESD energy under forward conduction conditions and the gate-driven $M_{N4}$ in the power-rail ESD clamp circuit has a large device dimension of 1680 $\mu$m/1.8 $\mu$m, the $V_{PP}$ pin can have high ESD robustness under the NS- and ND-mode ESD tests.

Under PS-mode ESD test, initial ESD energy is diverted to the ESD bus through the diode $D_2$ to elevate the voltage level on the ESD bus. The time delay from $R_1$ and $M_{C1}$ keeps the node A at a low voltage level relative to that of the ESD bus. Consequently, $M_{P1}$ is turned on to provide substrate-triggered current into P+ trigger nodes of $M_{N2}$, as the dashed line ($I_{Trigger}$) shown in Fig. 10(c). The substrate-triggered current can efficiently trigger on the parasitic n-p-n BJT inherent in $M_{N2}$, and the PS-mode ESD current ($I_{ESD}$) is primarily discharged to the grounded GND line through the parasitic BJT. Under PD-mode ESD test, the ESD trigger circuit can provide substrate-triggered current $I_{Trigger}$ to turn on $M_{N2}$ as well. The PD-mode ESD current $I_{ESD}$ is therefore discharged to the grounded $V_{DD}$ line through the substrate-triggered $M_{N2}$, the floating GND line, and the parasitic diode inherent in $M_{N4}$ [Fig. 10(d)].

### *C. ESD Measurement Results*

Among the ESD current discharging paths, it is known that PS- and PD-mode ESD tests are critical to $V_{PP}$ pin ESD protection because the ESD current is primarily discharged through the parasitic BJT inherent in the fully-silicided $M_{N2}$. The proposed ESD protection design under PS-mode ESD stresses was evaluated by using 100 ns transmission-line-pulse (TLP) system [28]. Failure criterion during TLP test was defined with 1 $\mu$A leakage current under 5 V bias on $V_{PP}$ pin. With the substrate-triggered technique, the parasitic BJT inherent in $M_{N2}$ was triggered on at ~10 V, and the measured secondary breakdown current was 3.8 A, as shown in Fig. 11. Measured HBM ESD protection levels of the IC product equipped with previous ESD protection design (Fig. 4) or the new proposed ESD protection design (Fig. 6) at $V_{PP}$ pin are summarized in Table II. In the HBM ESD tests, the starting test voltage was 0.5 kV, and the step voltage was 0.5 kV. The $V_{PP}$ pin was stressed three times at each HBM ESD level. The shift of *I–V* curve is the typical failure criterion used in the HBM ESD tests. Before ESD stress, a ±25 V voltage sweep with limited current supply was applied on $V_{PP}$ pin to acquire a fresh *I–V* curve as the reference. Another post-stress *I–V* curve was measured and compared to this fresh *I–V* curve after the $V_{PP}$ pin had been stressed three times at each selected ESD test level. It was judged as failure when the post-stress *I–V* curve deviated more than 20% from its fresh *I–V* curve.

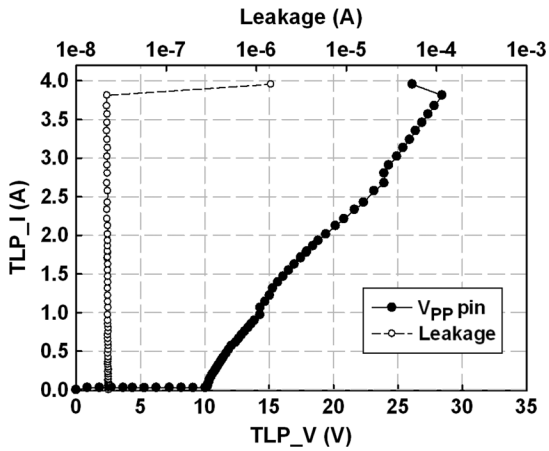


Fig. 11. TLP-measured *I–V* characteristics of the proposed ESD protection design under PS-mode ESD stress.

TABLE II
MEASURED HBM ESD ROBUSTNESS OF THE IC PRODUCT WITH PREVIOUS ESD PROTECTION DESIGN OR THE PROPOSED ESD PROTECTION DESIGN AT $V_{PP}$ PIN

| | PS-mode | PD-mode | NS-mode | ND-mode |
|---|---|---|---|---|
| Previous Design (Fig. 4) | 2 kV | 3.5 kV | 4.5 kV | 4.5 kV |
| Proposed Design (Fig. 6) | 5 kV | 5 kV | > 8 kV | > 8 kV |

With the PS- and PD-mode test results on the $V_{PP}$ pin listed in Table II, the substrate-triggered technique in collaboration with the N-well ballast layout can successfully enhance the turn-on speed and turn-on uniformity of $M_{N2}$. Therefore, HBM ESD protection levels can be significantly increased up to 5 kV. For NS- and ND-mode ESD tests, because the device dimension of the parasitic diode $D_{MN2}$ is larger than that of the diode $D_N$ in the previous ESD protection design, the proposed ESD protection design showed a higher HBM ESD protection level of over 8 kV. From the measurement results shown in Table II, the custom-specified 4 kV HBM ESD protection level has been successfully achieved by the proposed ESD protection design. A die photograph of the IC with the proposed ESD protection design is shown in Fig. 12, with a die size of 3.72 mm$^2$. The layout area of the proposed ESD protection circuit for the $V_{PP}$ pin is 24,186 $\mu$m$^2$, where $M_{N2}$ occupies a silicon area of 15,900 $\mu$m$^2$.

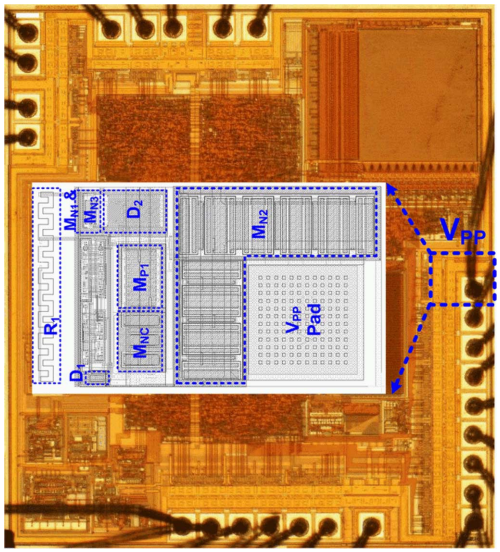


Fig. 12. Die photograph of the IC with proposed ESD protection design at $V_{PP}$ pin. Technology node used in this work is a 0.35 $\mu$m fully-silicided CMOS process with OTP memory cells.

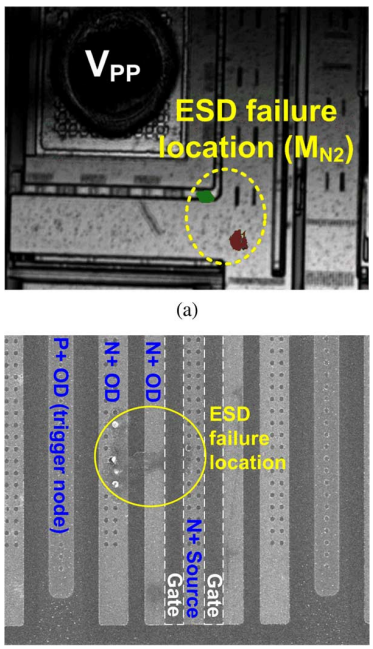


Fig. 13. (a) OBIRCH and (b) SEM images of the $V_{PP}$ pin with the proposed ESD protection design after 5.5 kV PD-mode HBM ESD stress.

The $V_{PP}$ pin with the proposed ESD protection design after 5.5 kV PD-mode HBM ESD test was analyzed by optical beam induced resistance change (OBIRCH) and SEM, as shown in Fig. 13(a) and (b), respectively. OBIRCH analysis revealed the location of ESD damage on the ESD protection nMOS $M_{N2}$. No light spots (no ESD damage) were found on internal circuits or the ESD trigger circuit. SEM analysis further confirmed that ESD failure spots were located on $M_{N2}$. These failure analyses have verified that the proposed ESD protection design at $V_{PP}$ pin is effective to protect internal circuits from being damaged by ESD stresses.

## V. Conclusion

Due to the high programming voltage on $V_{PP}$ pin, the placement of ESD diode from I/O pad to $V_{DD}$ is prohibited, which results in a stringent ESD design challenge for $V_{PP}$ pin. Moreover, the rise time of $V_{PP}$ programming voltage could be as fast as several tens of nanoseconds to cause mistriggering issue in some traditional ESD protection designs. In this work, a new ESD protection design has been proposed to overcome the mistriggering issue due to fast $V_{PP}$ programming voltage. A low-voltage nMOS was added at the output of ESD trigger circuit to overcome the mistriggering issue on the ESD protection device during $V_{PP}$ programming. Moreover, ESD bus in the proposed design can help prevent the mistriggering issue as well by reducing the overdrive current from ESD trigger circuit. The proposed ESD protection design has been successfully implemented on a commercial IC product fabricated in a 0.35 $\mu$m fully-silicided CMOS process with OTP memory cells. Experimental results showed that the new design can successfully avoid the mistriggering issue on ESD protection device when $V_{PP}$ voltage had a rise time as fast as 25 ns. Under ESD stress conditions, ESD protection device can be efficiently triggered on by substrate-triggered current to achieve a high HBM ESD protection level of 5 kV. Accordingly, with a high immunity against mistriggering and a good ESD robustness, the new proposed design is a competent ESD protection solution to the CMOS IC products with high-voltage programming pin.

## Acknowledgment

The authors would like to express their thanks for the TLP equipment from Hanwa Electronic Ind. Co., Ltd., Japan. Especially, thanks to Mr. Takumi Hasebe, Mr. Keiichi Hasegawa, and Mr. Masanori Sawada for setting up the TLP measurement system at National Chiao-Tung University, Taiwan.

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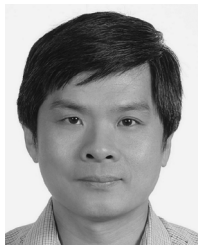

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