Novel Sub-10-nm Gate-All-Around Si Nanowire Channel Poly-Si TFTs With Raised Source/Drain

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***Abstract*—We have successfully fabricated novel sub-10-nm gate-all-around Si nanowire (NW) poly-Si TFTs with raised source/drain structure (GAA RSDNW-TFTs). The Si NW dimension is about 7 × 12 nm. A superior smooth elliptical shape is obtained, for the first time, in the category of poly-Si NW TFTs through the use of a novel fabrication process requiring no advanced lithographic tools. The GAA RSDNW-TFTs exhibit low supply gate voltage (3 V), steep subthreshold swing ∼99 mV/dec, and high $I_{ON}/I_{OFF} > 10^7$ ($V_D = 1$ V) without hydrogen-related plasma treatments. Furthermore, the DIBL of GAA RSDNW-TFTs is well controlled. These improvements can be attributed to the 3-D gate controllability, raised S/D structure, and sub-10-nm Si NW channel. These novel GAA RSDNW-TFTs are, thus, quite suitable for system-on-panel and 3-D IC applications.**

***Index Terms*—Gate-all-around (GAA), nanowire (NW), poly-Si thin-film transistors (poly-Si TFTs), raised source/drain (S/D).**

I. Introduction

RECENTLY, nonplanar device structures have been developed for better gate electrostatic control of channel potential [1]–[4]. Among these, gate-all-around silicon nanowire (GAA Si NW) transistors are promising candidates for future CMOS devices due to their reduced short-channel effects [2], [3]. Applications of Si NW transistors include nanoscale CMOS [2], memories [5], light-emitting devices [6], large-area electronics [7], and sensors for sensing chemical or biological species [8], [9]. The fabrication processes of NWs are traditionally prepared by either top–down or bottom–up approaches [5]–[8]. The top–down approaches employ advanced lithographic tools like deep UV steppers or e-beam writer tools. By contrast, the bottom–up methods may suffer from the uncontrollability of structural parameters, such as the length and diameter of NWs. Recently, several NW TFTs structures have been proposed [10]–[13]. These NW TFTs primarily use parasitic structures that have the advantages of low cost and simple fabrication methods. However, several issues, including the nonuniform, asymmetric wire shape, and rough wire surface, require solutions. Therefore, these devices have to be fabricated with additional treatments, such as hydrogen-related plasma treatments for more than 1 h, which improve the device characteristics. Furthermore, the thicknesses of thin n^+ source/drain (S/D) in conjunction with nanoscale NW will result in large parasitic resistance and poor driving currents. A nanoscale NW channel and a thick n^+ S/D region may not be satisfied simultaneously. Therefore, a raised S/D structure is essential in an ideal GAA Si NW device.

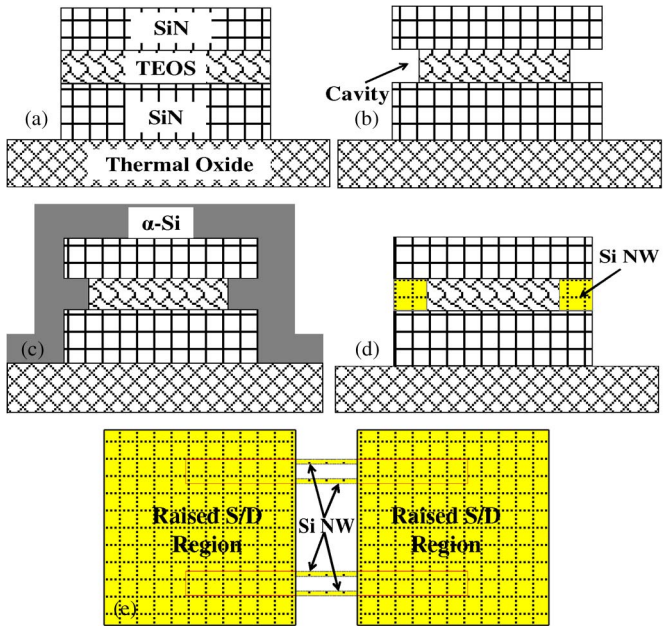

Fig. 1. (a)–(d) Key process flows of the GAA RSDNW-TFTs and (e) top view schematic structure after removing the dummy N/O/N.

In this letter, for the first time, novel sub-10-nm GAA Si NW poly-Si TFTs with raised S/D structure (GAA RSDNW-TFTs) are successfully fabricated and demonstrated. A superior smooth elliptical shape is obtained, for the first time, in the category of poly-Si NW TFTs through the use of a novel fabrication process. The proposed device simultaneously possesses sub-10-nm scaled Si NW and raised S/D without the use of advanced lithographic tools. The characteristics of GAA RSDNW-TFTs are superior and do not require hydrogen-related plasma treatments.

II. Experiment

The key process steps are shown in Fig. 1. The GAA RSDNW-TFTs were fabricated on Si wafers grown with a 500-nm thermal oxide layer. $Si_3N_4/SiO_2/Si_3N_4$ [N (70 nm)/O (15 nm)/N (30 nm)] dummy sandwich structures were then

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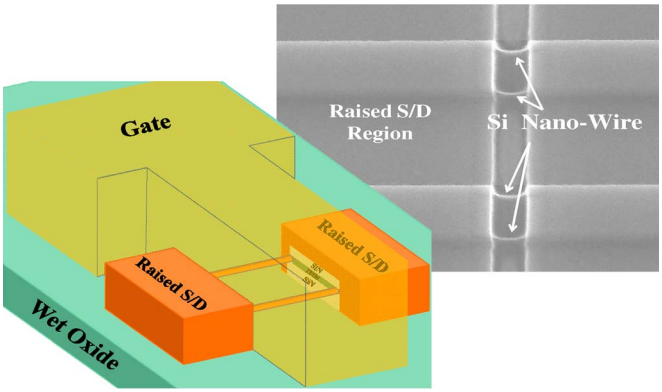

Fig. 2. Three-dimensional schematic structure of the multiple-channel GAA RSDNW-TFTs and SEM image of the structure formed after removing the dummy N/O/N.

deposited by low-pressure chemical vapor deposition (LPCVD) [Fig. 1(a)]. After the patterning and etching of NW definition region, lateral cavities in the N/O/N dummy sandwich structures were formed by selective wet etching of the sandwiched oxide [Fig. 1(b)]. The clamped structure formed by the top and bottom nitride thus controls the shape of the lateral cavities quite well. After the formation of the lateral cavity, a 100-nm-thick amorphous Si (a-Si) layer was deposited by LPCVD at 500 °C [Fig. 1(c)], which formed the nanoscale Si NW and the raised S/D simultaneously. Next, the a-Si layer was crystallized by solid-phase crystallization (SPC) at 600 °C for 24 h in N_2 ambient. The raised S/D region patterns were then defined by an I-line stepper. The raised S/D and the Si NW inlaid in the lateral cavities were fabricated by an anisotropic selective dry-etching step [Fig. 1(d)]. The Si NW channels with raised S/D were then selectively formed by removing the dummy N/O/N using hot phosphoric acid and dilute HF; top view was shown in Fig. 1(e). Fig. 2 shows the 3-D schematic structure of the multiple-channel GAA RSDNW-TFTs and the SEM image after removing the dummy N/O/N. A 7-nm LPCVD TEOS oxide and *in situ* doped n^+ poly-Si gate with a thickness of 250 nm were then deposited. After the gate patterning, the raised S/D regions were implanted with arsenic (As^+, 40-keV at 5×10^{15}-cm^{-2}) and activated at 600 °C in an N_2 ambient. Conventional top gate planar-TFTs with 50-nm-thick SPC channel and TEOS gate oxide/poly-Si gate were also fabricated to serve as controls. All devices, for comparison, have identical gate lengths of 0.35 μm, and the channel width of planar-TFTs is 0.35 μm. After passivation and metallic processes, the GAA RSDNW-TFTs and planar-TFTs were fabricated without hydrogen-related plasma treatments.

III. Result and Discussion

A cross-sectional transmission electron microscope (TEM) of a gate stacked GAA Si NW is shown in Fig. 3. The corner of Si NW was slightly etched during hot phosphoric acid process resulting in a smooth elliptical shape (about 7 × 12 nm), and the Si NW was surrounded by 7 nm of TEOS oxide and a poly-Si gate. A single crystalline cross-sectional view is observed in the Si NW. Fig. 4 shows the transfer characteristics of GAA RSDNW-TFTs and planar-TFTs. The GAA

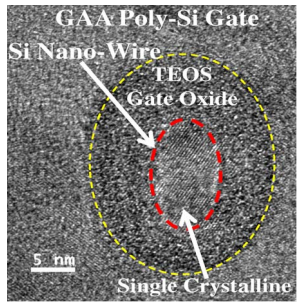

Fig. 3. Cross-sectional TEM microphotograph of a gated stacked GAA Si NW. A single crystalline cross-sectional view is observed in the GAA Si NW.

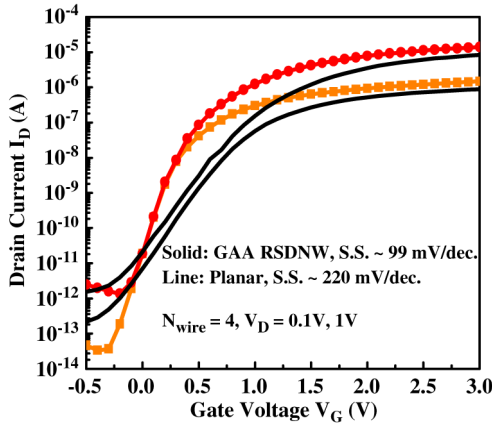

Fig. 4. Transfer characteristics of GAA RSDNW-TFTs and planar-TFTs. The well-behaved transfer characteristics for the GAA RSDNW-TFTs without hydrogen-related plasma treatments are illustrated.

RSDNW-TFTs with a channel length of 0.35 μm ($N_{\rm wire} = 4$, effective width $\sim 0.03 \times 4 = 0.12$ μm) exhibit steeper swing, lower supply gate voltage, and higher $I_{\rm ON}/I_{\rm OFF}$ ratio than the planar-TFTs. It is believed that the electrical characteristics of poly-Si TFTs can be improved if the poly-Si grain size can be enhanced and the number of grain boundaries in the channel can be reduced. In this letter, a single crystalline cross-sectional view is observed in the sub-10-nm scaled Si NW. Thus, the probability of the channel region to cover a grain boundary in the width direction decreases resulted in significant reduction of the number of grain boundaries in Si NW. Although the Si NW is not single crystalline for all channel, the characteristics of the GAA RSDNW-TFTs without hydrogen-related plasma treatments are close to those of single-crystalline MOSFETs. Furthermore, the DIBL of the channels during device operation of the GAA RSDNW-TFTs is negligible at $V_D = 2.5$ V (< 10 mV) due to the good gate controllability by the GAA structure and sub-10-nm Si NW channel. The surface-to-volume ratio results in higher performance on $I_{\rm ON}/I_{\rm OFF}$, S.S., and DIBL as well.

The output characteristics of the GAA RSDNW-TFTs and the planar-TFTs were compared in Fig. 5. In GAA RSDNW-TFTs, the saturation current ($\sim$26.2 μA) improvement over the planar-TFT device ($\sim$20.5 μA) is about 27% at $V_G - V_{\rm TH} = 2.5$ V and $V_D = 3.5$ V [width-normalized driving current (218.3 μA/μm) is about 3.7 times that of the planar-TFTs (58.5 μA/μm)]. The GAA RSDNW-TFTs exhibit higher driving currents than the planar-TFTs due to the raised S/D of the GAA RSDNW-TFTs (parasitic resistance R_p : 1.2 kΩ/5.78 kΩ

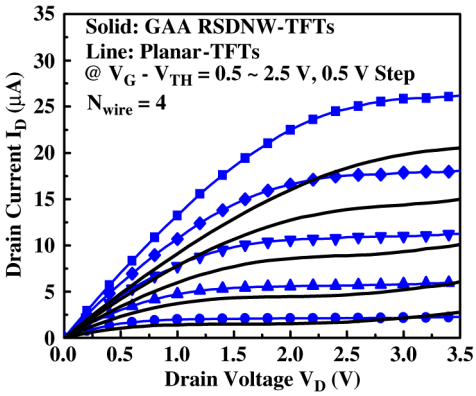

Fig. 5. Output characteristics of GAA RSDNW-TFTs and planar-TFTs, respectively. The RSDNW-TFTs exhibit higher driving and control well the floating-body effect.

TABLE I
COMPARISON OF SEVERAL IMPORTANT PARAMETERS OF THE GAA RSDNW-TFTs WITH NW-TFTs INVESTIGATED IN OTHER RESEARCH

	This Work	Ref. [10]	Ref. [11]	Ref. [12]	Ref. [13]
NW cross-section	Elliptical	Rectangular	Rough Triangular	Rough Rectangular	Triangular
NW dimensions (nm)	7×12	67	80×50×40	40×30	130×85×85
NH_3 Plasma	w/o	w/ 2hrs	w/ 3hrs	w/ 2hrs	w/ 3hrs
W/L (μm/μm)	0.03×4/0.35	0.067×10/5	0.17×2/1.5	0.13×2/0.4	1.2/1
S.S. (mv/dec.)	99	>200	150	251	~360
I_{ON}/I_{OFF} (V_G;V_D)	$>10^7$ (3V;1V)	~10^6 (10V;3V)	$>10^6$ (5V;2V)	$>10^7$ (8V;3V)	$>10^7$ (10V;2V)

for GAA RSDNW/planar-TFTs) [14]. In the planar-TFTs, the floating-body effects can be observed in output characteristics [14], [15]. These effects can be alleviated by either grounding the body with modified device structures or by using fully depleted SOI MOSFETs [16], [17]. The GAA RSDNW-TFTs exhibit kink-free output characteristics, indicating that the sub-10-nm Si NW channels are fully depleted by the GAA structure. In addition, we show a comparison of several important parameters of the GAA RSDNW-TFTs with NW-TFTs investigated in other research [10]–[13] in Table I. We can observe a smooth elliptical shape of NW channel in our work. This is the first time that this has been realized in the category of poly-Si NW TFTs. Furthermore, GAA RSDNW-TFTs exhibit steeper S.S., high $I_{\rm ON}/I_{\rm OFF}$, and lower supplied voltage without NH_3 plasma treatments. In contrast, the referenced NW-TFTs require additional plasma treatments more than 1 h to enhance the performance of devices. The applied gate voltage is significantly reduced to 3 V, and the $I_{\rm ON}/I_{\rm OFF} > 10^7$ can be achieved at $V_G = 3$ V and $V_D = 1$ V in GAA RSDNW-TFTs.

IV. CONCLUSION

Novel GAA Si NW TFTs with sub-10-nm Si NW and raised S/D structures have been successfully demonstrated. The GAA RSDNW-TFTs have steeper S.S., higher $I_{\rm ON}/I_{\rm OFF}$, and improved driving currents than planar-TFTs. The DIBL and floating-body effect were significantly suppressed due to the good gate controllability and fully depleted operation. This combination of GAA gate stacked structure, raised S/D, and sub-10-nm NW channel appears to be promising for SOP and future monolithic 3-D IC applications.

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