Design of Analog Pixel Memory for Low Power Application in TFT-LCDs

Li-Wei Chu, *Student Member, IEEE*, Po-Tsun Liu, *Senior Member, IEEE*, and Ming-Dou Ker, *Fellow, IEEE*

***Abstract*—Two types of analog memory cells realized in a 3-μm low temperature polycrystalline silicon (LTPS) technology are proposed to achieve low power application for thin film transistor liquid crystal displays (TFT-LCDs). By employing the inversion signal in the storage capacitor with complementary source follower, the frame rate to refresh the static image can be reduced from 60 to 3.16 Hz with the output decay less than 0.1 V under the input data from 1 to 4 V. To further diminish threshold voltage drop from source follower structure, a compensation technique is implemented to the proposed analog memory cells. In addition, asymmetric output voltage can be also minimized by adding a reference voltage to achieve symmetric output waveform.**

***Index Terms*—Analog memory, low power consumption, low temperature polycrystalline silicon (LTPS), thin-film transistor liquid-crystal displays (TFT-LCDs).**

I. Introduction

THIN-FILM transistor liquid crystal displays (TFT-LCDs) have become a mainstream in display markets due to its compact, light weight, and high contrast ratio. However, power consumption becomes a serious issue for the TFT-LCDs, especially for the portable products. The research reports mentioned that the power consumption almost comes from the backlight system and AC power supplying to liquid crystal of the source drivers [1]. Therefore, the memory-in-pixel (MIP) concept was proposed to meet low power application [2]–[8], which provided a low power standby mode for continuous display of static images without the power wastage on the source drivers. By refreshing the voltage level of scan lines, polarity inversion could be easily achieved even though the data is no longer furnished. So far, the literatures were reported with the digital MIP circuits [2]–[5]. They can be classified as two basic approaches: the static type and the dynamic type. In general, the static digital MIP circuit exhibits the lowest power consumption since the dynamic power is only consumed while pixels are charged during polarity inversion. However, the main drawback of the static digital MIP is too large in layout area for displays with a fine pixel pitch. The static MIP circuits typically required seven or eight TFTs and six row lines per pixel. On the contrary, the dynamic digital MIP circuits are more attractive because of fewer TFTs and row lines per pixel. Fig. 1 shows the dynamic digital MIP circuit which is realized with three n-type TFTs for one bit operation [2]. The manipulation starts at pre-charging the data line in the initial state. During the reading period, the data line voltage can be defined by the gate bias (Vp) of M3. Whereas Vp is a higher voltage, the voltage of data line will be a lower one. After that, the inverse data is then written back onto Vp via M1 in the writing period. Consequently, Vp is coupled by the scan signal through Cs and held until the next operation period, where C_{LC} and Cs are the capacitance of liquid crystal and storage capacitor. The refresh operation must be performed

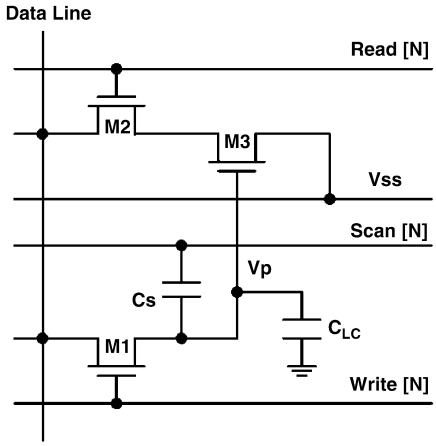

Fig. 1. Dynamic digital MIP circuit realized with three n-type TFTs for one bit operation [2].

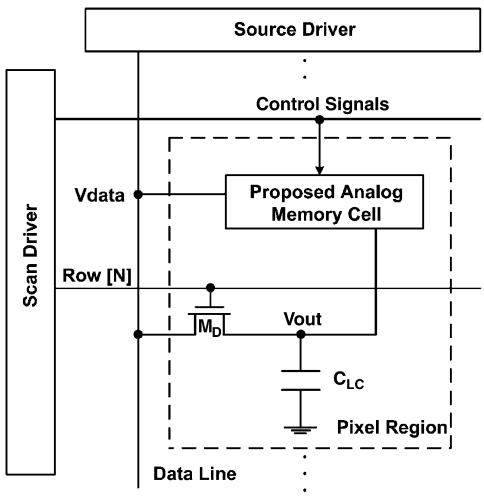

Fig. 2. Block diagram of the proposed analog memory cell in a conventional pixel.

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L.-W. Chu and P.-T. Liu are with the Department of Photonics & Display Institute, National Chiao-Tung University, Hsinchu 30078, Taiwan (e-mail: bambool.eo95g@nctu.edu.tw; ptliu@mail.nctu.edu.tw).

M.-D. Ker is with the Institute of Electronics, National Chiao-Tung University, Hsinchu 30078, Taiwan (e-mail: mdker@ieee.org).

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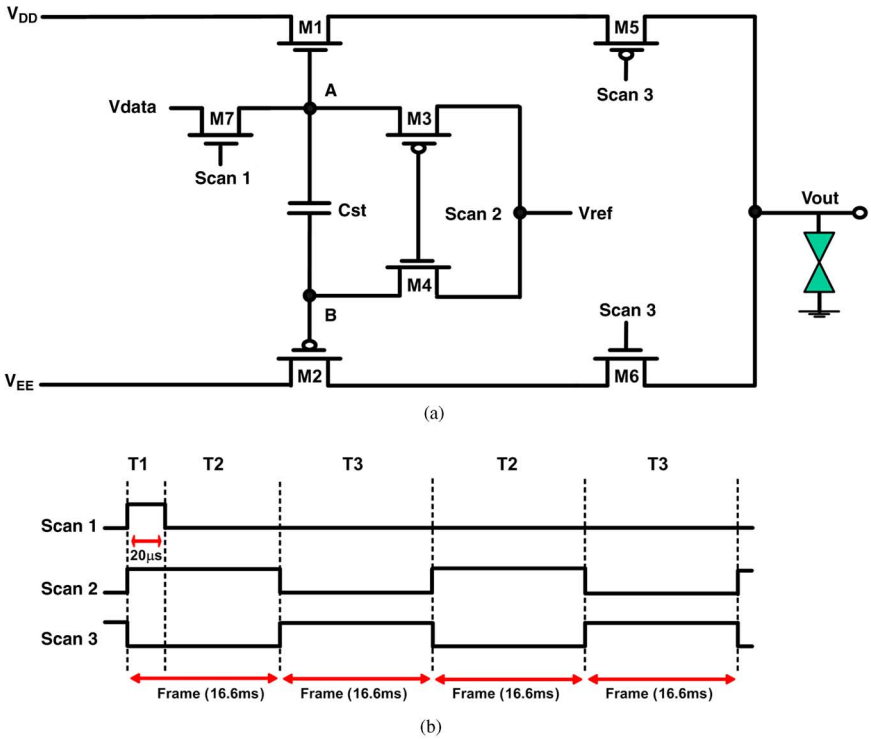


Fig. 3. Schematic of (a) the proposed memory cell I and (b) its corresponding control signals. The circuit is composed of two driving transistors (M1 and M2) and five switch transistors denoted as (M3, M4, M5, M6, and M7).

row by row so the largest power is consumed in pre-charging of the data line.

For multi-bits application, static and dynamic digital MIP circuits still require many scan lines and capacitors to reach polarity inversion. Therefore, the adoption of analog concept for MIP circuit is attempted since it can achieve higher image quality with fewer components. However, the output voltage of the analog memory circuit may have inaccuracy with corresponding data signal, which means that the static image may be distorted by the asymmetric inversion voltage.

In this work, two types of analog memory cells with self voltage inversion for MIP application are proposed, which have been realized in a conventional 3-μm LTPS process without additional process modification. By using the proposed circuits, the operating rate to refresh static image can be reduced from 60 to 3.16 Hz. Asymmetric inversion voltage can be also minimized by adding a reference voltage to achieve symmetric output waveform. Moreover, a compensation technique is implemented to improve the threshold voltage drop on the output from the input data [9].

II. Operation and Simulation of Proposed Circuits

Fig. 2 shows the block diagram of the proposed analog memory cell in a conventional pixel of LCD. There are two modes for dynamic and static operation of LCD image. During the normal mode, dynamic image can be performed by the conventional pixel operation through $\mathrm{M_D}$. Furthermore, during the standby mode for static image, the scan driver switches input from row signal ($\mathrm{Row[N]}$) to control signals. The proposed analog memory cell samples Vdata from source driver and cooperates with control signals to generate self inversion voltage at Vout.

A. New Proposed Analog Memory Cell I

Source driver provides Vdata ($\mathrm{Vdata} = |\mathrm{Vp}| + |\mathrm{Vt}|$) to the data line for the proposed analog memory cell I, where Vp is the original pixel data and Vt is the threshold voltage of Poly-Si TFT. Fig. 3(b) depicts its corresponding waveforms of scan lines [10]. After the proposed analog memory cell I samples the Vdata, the source driver can be turned off until the specific time is arrived. With 315.4 ms as an example (19 times of typical TFT-LCD frame time), the source driver can be operated from 60 to 3.16 Hz for refreshing static image to save power.

The proposed analog memory cell I shown in Fig. 3(a) is composed of two driving transistors (M1 and M2), and five switch transistors (M3, M4, M5, M6, and M7). During the standby mode, the operation of the proposed analog memory cell I is divided into three periods, including the pre-charging period (T1), the positive voltage holding period (T2), and the negative voltage holding period (T3). In the T1 period, Scan2 and Scan3 are set to turn M3 and M6 off. The driving transistor M1 is operated as a source follower, and Vout becomes $\mathrm{Vdata}-\mathrm{Vtn}$ at the end of this period, where Vtn is the threshold voltage of M1. In the meanwhile, the node voltages of the storage capacitor (Cst) are set with $\mathrm{V_A} = \mathrm{Vdata}$ and $\mathrm{V_B} = \mathrm{Vref}$. In the T2 period, Scan1 becomes low to turn M7 off, and the other transistors are all kept at the previous states. The gate voltages of M1 and M2 are Vdata and Vref, respectively. Vout remains $\mathrm{Vdata} - \mathrm{Vtn}$ at the positive data holding period (T2). At the T3 period, Scan2 and Scan3 are set to turn M4 and M5 off. Because M3 is turned on, Vref is applied to the node A. The voltage of node B goes to $2\,\mathrm{Vref} - \mathrm{Vdata}$ because Cst is boosted by the voltage at node A ($\mathrm{V_A}$). At the beginning of T3 period, M2 is operated as a source follower. The output voltage goes to $2\mathrm{Vref} - \mathrm{Vdata} + |\mathrm{Vtp}|$

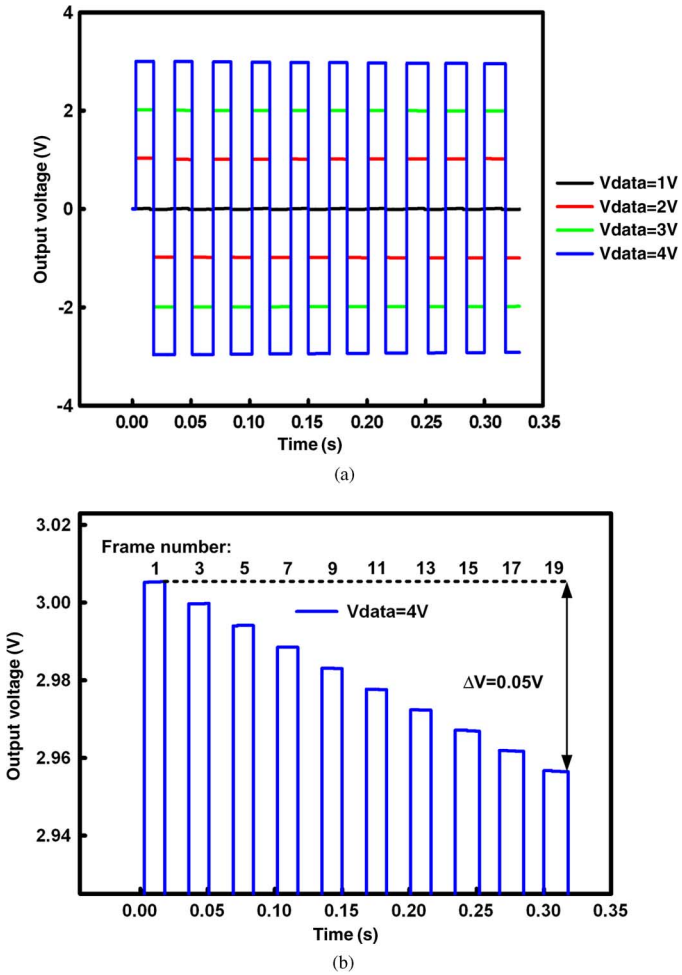


Fig. 4. Simulation results of the output (Vout) in the proposed analog memory cell I under: (a) Vdata of 1, 2, 3, and 4 V, respectively, in 20-frame time per Scan1 pulse and (b) the partial enlarged plot when Vdata is 4 V.

and then holds this voltage level until the next period comes, where $|\mathrm{Vtp}|$ is the absolute threshold voltage of M2.

The aspect ratio of channel width (W) to channel length (L), W/L, for M1 and M2 are 30 μm/5 μm, and those for switch transistors (M3, M4) and (M5, M6, M7, M8, M9) are 3 μm/5 μm and 5 μm/5 μm, respectively. Furthermore, the storage capacitor (Cst) is 5 pF and the DC voltage supplies are $\mathrm{V_{DD}} = 5$ V and $\mathrm{V_{EE}} = -5$ V. Fig. 6 depicts the simulation results of the output (Vout) for the proposed analog memory cell II under Vdata of 1, 2, 3, and 4 V, respectively. The output voltage levels of Fig. 6(a) are all the same as the input data. These results have successfully verified that the outputs are independent to the threshold voltage. Fig. 6(b) gives the partial enlarged plot of Fig. 6(a) when Vdata is 4 V. After 19-frame time, the simulation result shows that the output voltage decay (ΔV) is only 0.06 V. This represents the proposed circuit can be effectively operated higher than 6-bit (data range/one gray scale $= 4/0.06 = 66.67$) digital memory at the frame rate of 3.16 Hz. Fig. 7 shows the output voltage (Vdata $= 3$ V) for M1 and M2 with equal threshold voltage shifts. The threshold voltage shifts are caused by the process variation or the stress under operation. The initial threshold voltage shifts can be minimized by adding the reference voltage (Vref) to achieve symmetric output waveform in the proposed analog memory cells. Besides, the proposed analog memory cells are composed of complementary source follower, the stress condition at $\mathrm{V_A}$ and $\mathrm{V_B}$ in Fig. 3(a) and Fig. 5(a) are similar under different input data. In Fig. 7, there is no apparent difference between the absolute threshold voltages from 0.9 to 1.9 V with the step of 0.5 V. The error rates, which is derived from the output voltage difference (ΔV in Fig. 7) dividing the threshold voltage difference, are just 1.14% and 2.12%. The proposed analog memory cells are quite suitable for MIP application. In the standby mode, Vout is varied according to the M1 and M2 source followers, respectively. The threshold voltage difference ΔVt between Vtn and $|\mathrm{Vtp}|$ will cause non-symmetric output waveforms at Vout, so liquid crystal can't present equal transmittance. In order to solve this issue, assume

$$\Delta\mathrm{Vt} = \mathrm{Vtn} - |\mathrm{Vtp}|. \tag{1}$$

The request for the negative data holding period (T3) is generating the opposite sign of the output voltage ($-$Vout) during the positive data holding period (T2). Hence, Vout can be defined as $-(\mathrm{Vdata} - \mathrm{Vtn})$, and which gives

$$-(\mathrm{Vdata} - \mathrm{Vtn}) = \mathrm{V_B} + |\mathrm{Vtp}| = 2\mathrm{Vref} - \mathrm{Vdata} + |\mathrm{Vtp}|. \tag{2}$$

Derived from (2), the optimized reference voltage (Vref) can be set to achieve the cancellation of threshold voltage difference between M1 and M2. The reference voltage should be

$$\mathrm{Vref} = (\mathrm{Vtn} - |\mathrm{Vtp}|)/2 = \Delta\mathrm{Vt}/2. \tag{3}$$

By adjusting the reference voltage, the problem of asymmetric inversion voltage in the proposed analog MIP can be solved by this design.

The proposed analog pixel memory cell I has been designed and verified by the HSPICE simulation with the RPI model (Level $= 62$) of a 3-μm LTPS process provided by the foundry. The threshold voltage values of Vtn and Vtp are 0.9 V and -0.9 V, respectively. The aspect ratio of channel width (W) to channel length (L), W/L, for driving transistors M1 and M2 are 30 μm/5 μm, and those for switch transistors (M3, M4) and (M5, M6, M7) are 3 μm/5 μm and 5 μm/5 μm, respectively. Furthermore, the storage capacitor is $\mathrm{Cst} = 5$ pF and the DC voltage supplies are $\mathrm{V_{DD}} = 5$ V and $\mathrm{V_{EE}} = -5$ V. Fig. 4 depicts the simulation results of the output (Vout) for the proposed analog memory cell I under Vdata of 1, 2, 3, and 4 V, respectively. The 20-frame time ($20 * 16.6$ ms $= 332$ {ms}) per Scan1 pulse is set for the timing duration of Scan1 signal. The power consumption comes from the source driver only when Vdata is sampled by the proposed analog memory cell I. Afterward, the cell works between the positive and negative data holding periods to generate positive and negative pixel voltages at Vout only by the control signals. Fig. 4(a) shows the simulated output symmetric voltages no matter how the input data changes. Besides, the high and low voltage levels are decreased approximately a threshold voltage due to the operation of source followers.

Fig. 4(b) gives the partial enlarged plot of Fig. 4(a) when Vdata is 4 V. After nineteen frame time, the simulation result shows that the output voltage decay (ΔV) is only 0.05 V.

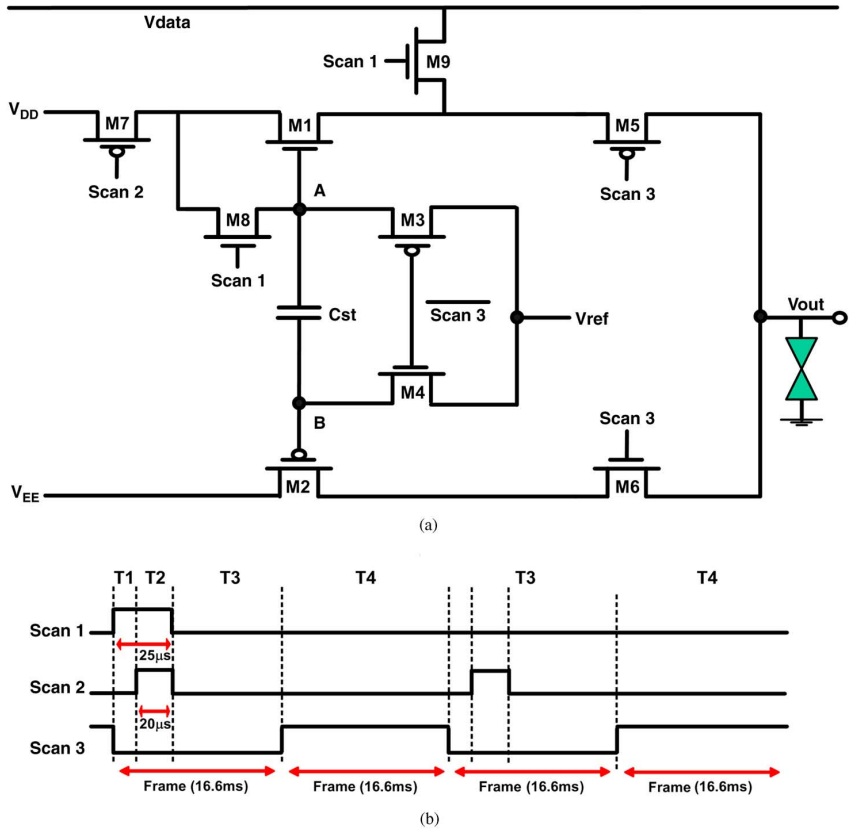


Fig. 5. Schematic of (a) the proposed memory cell II and (b) its corresponding control signals. The circuit is composed of two driving transistors (M1 and M2) and seven switch transistors denoted as (M3, M4, M5, M6, M7, M8, and M9).

This represents the proposed circuit can be effectively operated higher than 5-bit $(\text{data range/one gray scale} = 3/0.05 = 60)$ digital memory at the frame rate of 3.16 Hz.

B. New Proposed Analog Memory Cell II With Threshold Voltage Compensation

Due to the threshold voltage drop of the output voltage from the input data in the proposed analog memory cell I, the analog memory cell II is then proposed to release this limitation. By applying the proposed analog memory cell II, source driver needs not provide Vdata of $|\text{Vp}|+|\text{Vt}|$ to data line but provide Vdata of $|\text{Vp}|$ only. Therefore, source driver doesn't have to modify the data signal with a threshold voltage shift and further reduce the algorithm complexity of source driver.

Fig. 5(a) depicts the proposed analog memory cell II and its corresponding waveforms of scan lines. The proposed analog memory cell II is composed of two driving transistors (M1 and M2), and seven switch transistors (M3, M4, M5, M6, M7, M8, and M9). The operation is divided into four periods, including the pre-charging period (T1), the threshold voltage (Vt) compensation period (T2), the positive voltage holding period (T3), and the negative voltage holding period (T4). In the T1 period, scan signals turn on the switches (M4, M5, M7, M8, and M9) and turn (M3 and M6) off, respectively. Vout becomes Vdata through M9, and V_A is charged to V_DD. In the T2 period, Scan2 goes to high to turn M7 off. M1 starts to release charge from V_A through M8 in a diode connect structure and V_A becomes $\text{Vdata}+\text{Vtn}$ at the end of this period, where Vtn is the threshold voltage of M1. In the meanwhile, the storage capacitor (Cst) is set to $\text{V}_\text{A} = \text{Vdata} + \text{Vtn}$ and $\text{V}_\text{B} = \text{Vref}$. In the T3 period, Scan1 becomes low to turn M8 and M9 off. Scan2 goes to low to turn on M7, and the other transistors are all kept at the previous states. The gate voltages of M1 and M2 are $\text{Vdata}+\text{Vtn}$ and Vref, respectively. Vout remains Vdata at the positive data holding period (T3). At the T4 period, Scan3 becomes high to turn M4 and M5 off. Because M3 is turned on, Vref is applied to the node A. The voltage of node B goes to $2\text{Vref}-(\text{Vdata}+\text{Vtn})$ because Cst is boosted by the voltage at node A (V_A). At the beginning of T4 period, M2 is operated as a source follower. The output voltage goes to $2\text{Vref}-(\text{Vdata}+\text{Vtn})+|\text{Vtp}|$ and then holds this voltage level until the next period comes, where $|\text{Vtp}|$ is the absolute threshold voltage of M2.

The threshold voltage difference between Vtn and $|\text{Vtp}|$ will cause non-symmetric output waveforms, so that liquid crystal cannot present equal transmittance. In order to solve this issue, the request for negative data holding period (T4) is to generate opposite sign voltage $(-\text{Vout})$ during the positive data holding period (T3). Vout will become $-\text{Vdata}$, which gives

$$\begin{aligned} -\text{Vdata} &= \text{V}_\text{B} + |\text{Vtp}| \\ &= 2\text{Vref} - (\text{Vdata} + \text{Vtn}) + |\text{Vtp}|. \end{aligned} \tag{4}$$

Derived from (4), the optimized reference voltage (Vref) can be set to achieve the cancellation of threshold voltage difference between M1 and M2. The reference voltage is the same as that shown in (3). By adjusting this reference voltage, the problem of asymmetric inversion voltage for analog MIP can be completely solved by the proposed analog memory cell II.

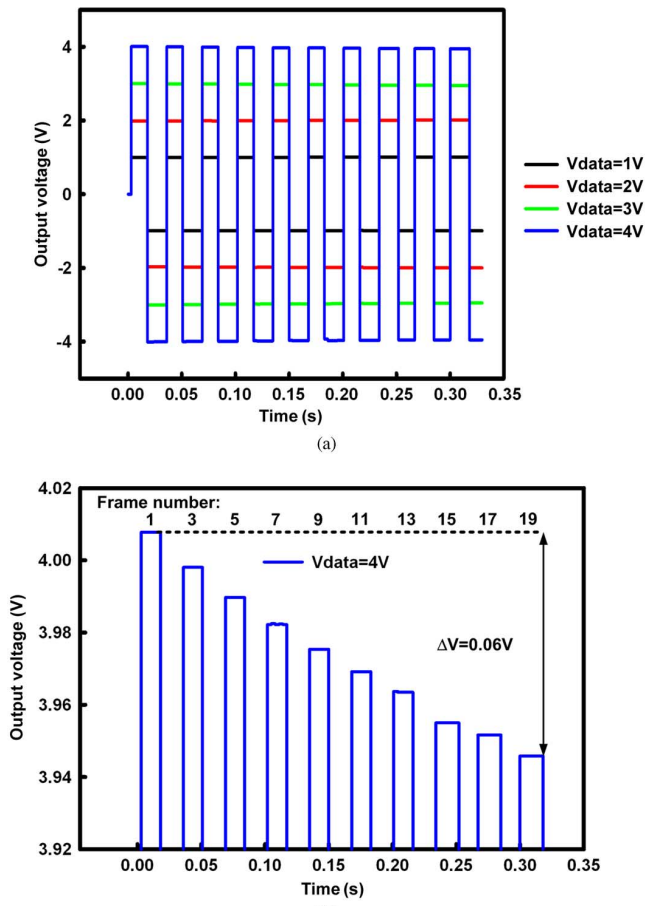


Fig. 6. Simulation results of the output (Vout) in the proposed analog memory cell II under: (a) Vdata of 1 V, 2 V, 3 V, and 4 V in 20-frame time per Scan1 pulse, and (b) the partial enlarged plot when Vdata is 4 V.

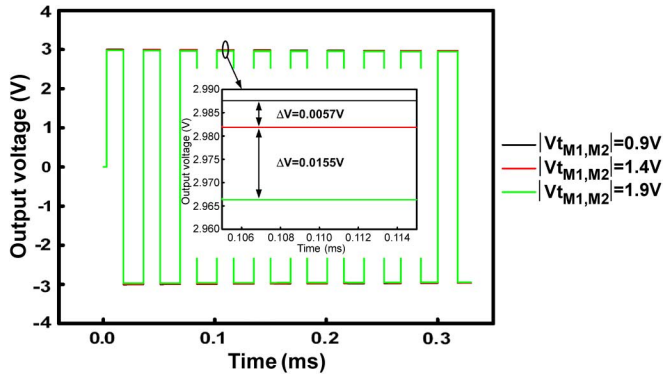


Fig. 7. Output voltage for M1 and M2 with equal shifts on threshold voltage of 0.9 V, 1.4 V, and 1.9 V when Vdata is 3 V.

III. Experimental Results and Discussion

A. New Proposed Analog Memory Cell I

For measurement setup, synchronous signals are generated by the pulse card option for Keithley 4200 (4205-PG2). Input range of Scan1 is set as 0 to 10 V. Scan2 and Scan3 are set as −5 to 5 V. Digital oscilloscope is utilized to observe the output waveforms. The die photo of fabricated two types of the proposed analog memory cells are shown in Fig. 8. A large layout area is occupied by the storage capacitor (Cst) since it is fabricated by the interlayer oxide. The equivalent oxide thickness

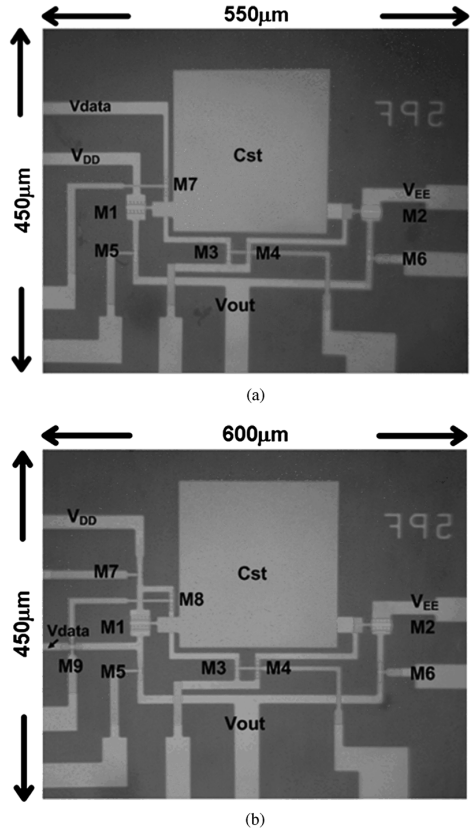
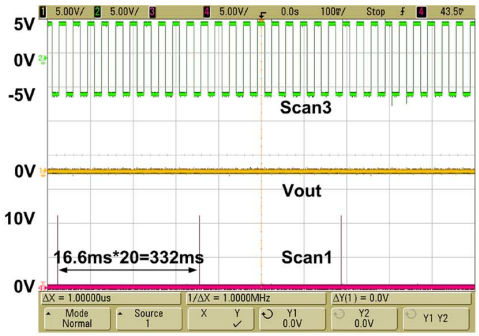


Fig. 8. Die photo of the proposed. (a) Analog memory cell I. (b) Analog memory cell II, fabricated in a 3-μm LTPS process.

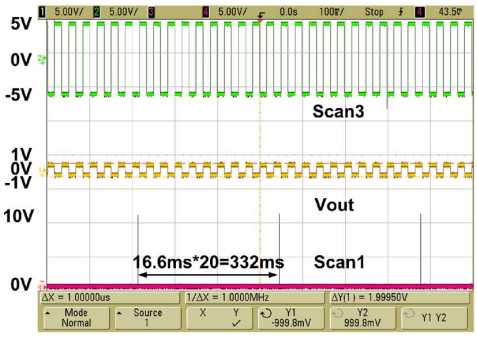
of the interlayer oxide is about eight times thicker than the gate oxide in TFT. For circuit verification, twenty frame time per Scan1 is used to verify the output waveforms whether it can meet the desired function. As shown in Fig. 9, the output inversion signal (Vout) are from 0 to 0 V, 1 to −0.998 V, 2 to −2.015 V, and 3 V to −2.975 V, when Vdata varies from 1 to 4 V with a step of 1 V and Vref is 0.2 V (ΔVt is about 0.4 V). The definition of the inaccuracy for polarity inversion difference is |Vout_positive − |Vout_negative||, and which is no more than 0.025 V because of Vref feeding. The threshold voltages of M1 (Vtn) and M2 (Vtp) are about 1 V and −0.6 V from the output results. Fig. 10 shows the enlarged plot for Vout as 0.5 V/scale in Fig. 9(d) when Vdata is 4 V. The frame numbers are listed from the 1st to 19th, and which are corresponding to 3 V (Y2: the first frame number) and 2.925 V (Y1: the 19th frame number). Fig. 11 shows the summary of the output voltage under different frame numbers with Vdata of 2, 3, and 4 V, respectively, in the proposed analog memory cell I for the positive output voltage. The maximum output voltage decay is less than 0.075 V after nineteen frame time when Vdata is 4 V. It verified that the operating frequency of source driver can be reduced from 60 to 3.16 Hz for static image. Besides, frame number can be chosen by the tolerance of specified output decay for higher resolution.

B. New Proposed Analog Memory Cell II With Threshold Voltage Compensation

Fig. 12 shows the output inversion signal (Vout) of the proposed analog memory cell II which are from 1 to −0.998 V,



(a)



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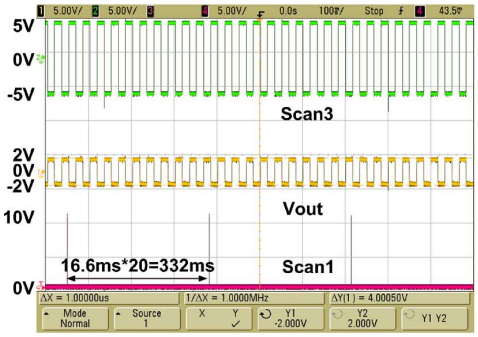
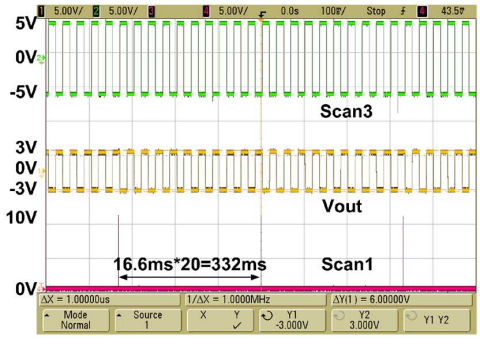


(c)



(d)

Fig. 9. Measured results of analog memory cell I with: (a) $\mathrm{Vdata} = 1$ V; (b) $\mathrm{Vdata} = 2$ V; (c) $\mathrm{Vdata} = 3$ V; and (d) $\mathrm{Vdata} = 4$ V in 20-frame time (16.6 ms $* 20 = 332$ ms) per Scan1 pulse.

2 to -2.015 V, 3 to -3.015 V, and 4 V to -4.025 V, when Vdata varies from 1 to 4 V with a step of 1 V and Vref is 0.2 V (ΔVt is about 0.4 V). The inaccuracy for polarity inversion difference is no more than 0.025 V. The output voltage can be directly obtained from Vdata without the threshold voltage issues which are consistent with the simulation results. Furthermore, the maximum output voltage decay is less than 0.1 V after

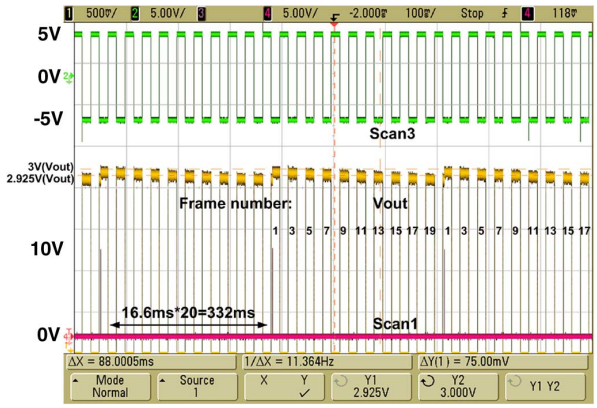


Fig. 10. Enlarged plot for Vout as 0.5 V/scale in Fig. 9(d) when Vdata is 4 V.

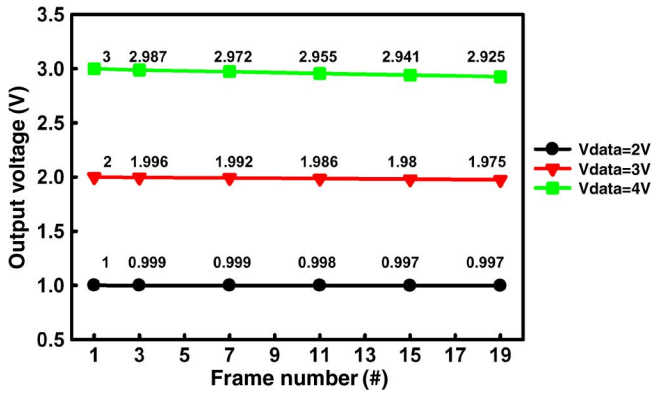


Fig. 11. Output voltage under different frame numbers with Vdata of 2, 3, and 4 V, respectively, in the proposed analog memory cell I for the positive output voltage.

nineteen frame time when Vdata is 4 V. Fig. 13 shows the enlarged plot for Vout as 1 V/scale in Fig. 12(d) when Vdata is 4 V. The entire output waveform is contained to show the output symmetry. The frame numbers are listed from 1st to 19th, and which are corresponding to 4 V (Y1: the first frame number) and 3.9 V (Y2: the 19th frame number). Fig. 14 shows the summary of output voltage under different frame numbers with Vdata of 1, 2, 3, and 4 V, respectively, in the proposed analog memory cell II for the positive output voltage. The frame number can be chosen by the tolerance of specified output decay for the application of better resolution. By integrating the proposed MIP circuit into the pixel, better image quality can be obtained.

The reason for the voltage decay as shown in Fig. 11 and Fig. 14 is caused by the parasitic effects of transistors. During the T3 to T4 periods in Fig. 5, $\mathrm{V_A}$ changes from Vdata+Vtn to Vref, and this transient voltage will couple the node B through the storage capacitor (Cst). Nevertheless, the existence of parasitic capacitance will decrease the coupling amount, and which will directly affect the output voltage. The voltage at node B can be shown in the following [11]:

$$\mathrm{V_B} = \mathrm{Vref} \frac{\mathrm{Cst}}{\mathrm{Cgs2} + \mathrm{Cgd2} + \mathrm{Cst} + \mathrm{Cgs4}} (\mathrm{Vdata} + \mathrm{Vtn} - \mathrm{Vref}). \quad (5)$$

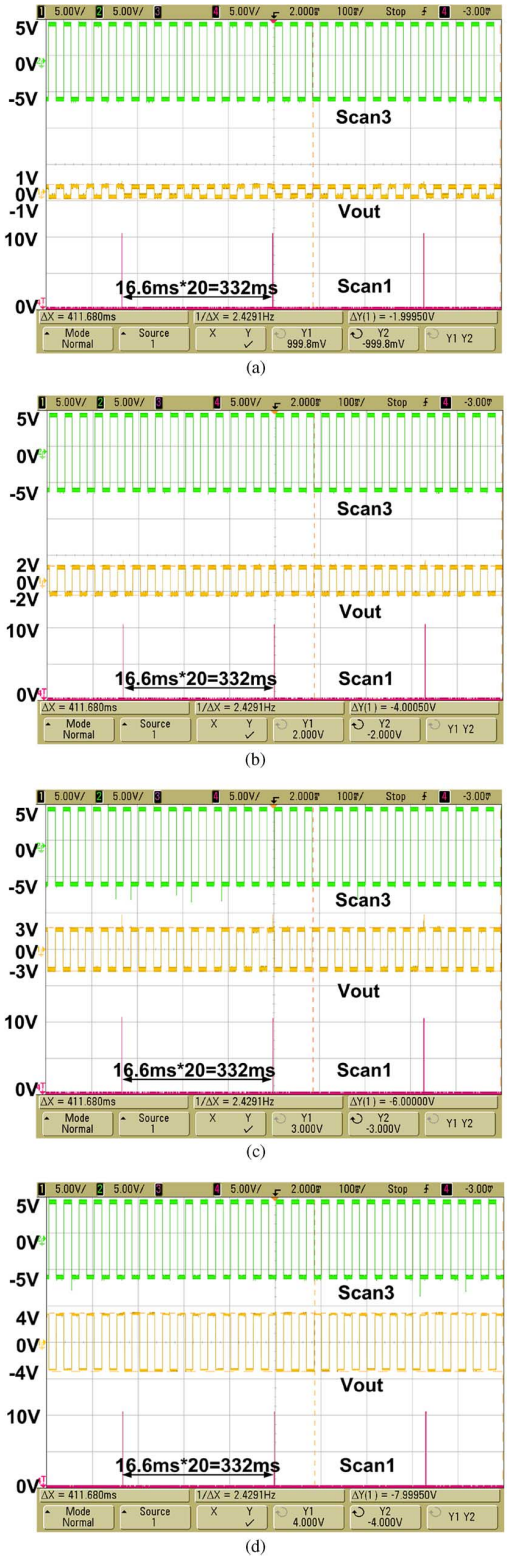


Fig. 12. Measured results of analog memory cell II with: (a) $\mathrm{Vdata} = 1$ V; (b) $\mathrm{Vdata} = 2$ V; (c) $\mathrm{Vdata} = 3$ V; and (d) $\mathrm{Vdata} = 4$ V in t20-frame time (16.6 ms $* 20 = 332$ ms) per Scan1 pulse.

The second term of (5) shows that the coupling amount is reduced due to the capacitive division, where $\mathrm{Cgs2}, \mathrm{Cgd2}$, and $\mathrm{Cgs4}$ are the parasitic capacitance of M2 and M4. Moreover, this effect takes place at every transition of polarization inversion to cause the output decay

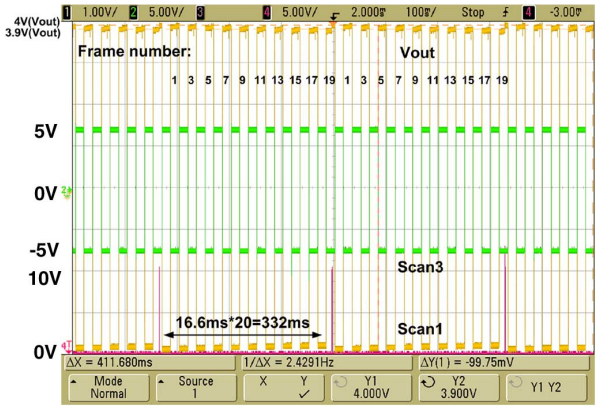


Fig. 13. The enlarged plot for Vout as 1 V/scale in Fig. 12(d) when Vdata is 4 V. The entire Vout waveform is contained to show the output symmetry.

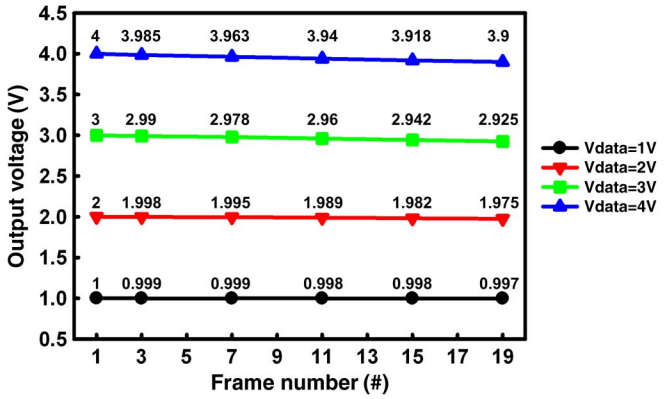


Fig. 14. The output voltage under different frame numbers with Vdata of 1, 2, 3, and 4 V, respectively, in the proposed analog memory cell II for the positive output voltage.

since there is no refreshed data to the storage capacitor. After more frame cycles, the holding voltage will be smaller than the previous one. In order to reduce such a non-ideal effect, storage capacitor (Cst) has to be designed as greater as possible to meet the ideal case in (4). However, it will become a trade off to the LCD's aperture ratio. The row time of this work is approximately 25 μs and which limits the aspect ratio of M1 and M2 to charge the output. The simulation results show that the aspect ratio of 3 μm/5 μm is quite enough for the output loading of real pixel (300 fF) in TFT-LCDs. On the contrary for the measurement consideration, the larger aspect ratio of 30 μm/5 μm has to be designed for the output loading of oscilloscope (10 pF) and it leads to greater parasitic capacitance. Therefore, the storage capacitor ($\mathrm{Cst} = 5$ pF) is applied to verify the functionality of the proposed circuits. The comparison of the conventional storage capacitor is about 0.2–0.3 pF.

Although equal threshold voltage shifts is applied in the proposed analog memory cell II in Fig. 7, the different threshold voltage shifts should be concerned in the real devices. When the stress poses different threshold voltage shifts between M1 and M2, the error rate (the output voltage difference (ΔV in Fig. 7) dividing the threshold voltage difference) of the proposed analog memory cell II becomes quite larger. Besides, the error rate is proportional to the difference value between the threshold

voltage shifts of M1 and M2, since the threshold voltage of M1 is utilized to compensate the threshold voltage of M2 in the proposed analog memory cell II. Even though it can not compensate this difference value, the design concept still can decrease the effect of the equal threshold voltage shifts. Furthermore, the same Vref is utilized in the proposed analog memory cells under different input data. It can be derived that the higher input data (Vdata) results to larger inaccuracy for polarity inversion difference from the (2), (4), and (5). Nevertheless, the pixels are addressed in rows and columns in TFT-LCDs. The layout of Vref line should be parallel with the gate line (row) or source line (column) to control a large number of pixels. Therefore, the same Vref is applied in the measurement results under different input data.

IV. Conclusion

Two proposed analog pixel memory cells for power saving application in TFT-LCDs have been successfully verified in a 3-μm LTPS process. The frame rate to refresh the static image can be reduced from 60 to 3.16 Hz with the voltage decay at the output only less than 0.1 V under the input data varies from 1 to 4 V. Experimental results have successfully verified that both of the proposed analog memory cells are suitable for the MIP application of high resolution. Besides, the compensation technique is used to improve the output voltage decay due to the threshold voltage drop.

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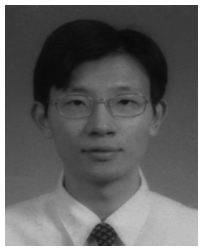
Li-Wei Chu (S'10) received the B.S. degree from the Department of Electrical Engineering, National Sun Yat-sen University, Taiwan, in 2006, and the M.S. degree in electro-optical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2008. Since August 2008, he has been working toward the Ph.D. degree at the National Chiao Tung University.

His current research interests include the peripheral circuits integrated on panel for flat panel display applications and the design of 60-GHz ESD protection circuits in 65-nm CMOS process.



Po-Tsun Liu (SM'07) received the Ph.D. degree from the Institute of Electronics, National Chiao-Tung University (NCTU), Hsinchu, Taiwan, in 2000.

He is currently a professor and director at the Department of Photonics and Display Institute, NCTU, Taiwan. He also was a visiting professor at the Department of Electrical Engineering at Stanford University, Palo Alto, CA, from August 2008 to July 2009. In his specialty, he has made a great deal of pioneering contributions to ULSI technology, semiconductor memory devices and TFT-LCD displays. In his previous researches on low-dielectric-constant (low-k) materials and copper interconnects, he utilized hydrogen plasma treatment technique for the first time to improve electrical characteristics of low-k silicate-based materials and to resist copper diffusion. In addition, he proposed a low-temperature supercritical carbon dioxide fluids ($SCCO_2$) technology for the first time to improve the dielectric characteristics of the sputter-deposited HfO_2 film by passivating trap states. His current researches focus on the advanced flat panel display device technologies, specialized in thin-film transistors (TFTs), the advanced nano-scale semiconductor devices, nonvolatile memory devices, and nano-fabrication technologies.

He is a member of Society for Information Display. So far, he has published 150 articles of SCI international journals/letters, 80 international conference papers and obtained 17 US patents and 46 Taiwan patents. Because of the prominent contributions, he was selected in Marquis Who's Who in the World (20th edition, 2003) and obtained 2007 Outstanding Young Electrical Engineer Award of Chinese Institute of Electrical Engineering. Furthermore, Dr. Liu has superior performance in teaching, and obtained twice Excellent Teaching Awards at NCTU.

Ming-Dou Ker (S'92–M'94–SM'97–F'08) received the Ph.D. degree from National Chiao-Tung University, Hsinchu, Taiwan, in 1993.

He worked as the Department Manager with the VLSI Design Division, Computer and Communication Research Laboratories, Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan. Since 2004, he has been a Full Professor with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan. From 2008, he was rotated to be Chair Professor and Vice President of I-Shou University, Kaohsiung, Taiwan. He has been the Distinguished Professor in the Department of Electronics Engineering, National Chiao-Tung University; and also served as the Executive Director of National Science and Technology Program on System-on-Chip (NSoC) in Taiwan. He has published over 400 technical papers in international journals and conferences In the technical field of reliability and quality design for microelectronic circuits and systems. He has proposed many solutions to improve the reliability and quality of integrated circuits, which have been granted with 167 U.S. patents and 148 Taiwan patents. He had been invited to teach and/or to consult the reliability and quality design for integrated circuits by hundreds of design houses and semiconductor companies in the worldwide IC industry. His current research interests include reliability and quality design for nanoelectronics and gigascale systems, high-speed and mixed-voltage I/O interface circuits, on-glass circuits for system-on- panel applications, and biomimetic circuits and systems for intelligent prosthesis.

Prof. Ker has served as a member of the Technical Program Committee and the Session Chair of numerous international conferences for many years. He has served as the Associate Editor for the IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2006–2007. He was selected as the *Distinguished Lecturer* in the IEEE Circuits and Systems Society (2006–2007) and in the IEEE Electron Devices Society (2008–2010). He was the President of Foundation in Taiwan ESD Association. In 2009, he was awarded as one of the top ten Distinguished Inventors in Taiwan.