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Correlation of Polysilicon Thin-Film Transistor Characteristics to Defect States via Thermal Annealing

Horng Nan Chern, Chung Len Lee, and Tan Fu Lei

***Abstract*—Based on the response of electrical characteristics of hydrogenated polysilicon thin-film transistors (TFT's) to post-hydrogenation thermal annealing, the relationship of device parameters to deep states and tail states are distinguished. The deep states which affect the threshold voltage and subthreshold swing recover quickly, while the tail states which influence the leakage current and field effect mobility respond to the thermal annealing only after the annealing temperature exceeds 375°C for 30 min.**

I. INTRODUCTION

To realize high-performance TFT's, it is necessary to reduce the defects of the polysilicon film. When polysilicon TFT's are subjected to H_2 plasma treatment, their defect states are reduced and the performance is improved [1]–[5]. Recently, the passivation mechanisms of the H_2 plasma treatment on defect states in the polysilicon film have been widely investigated [2]–[5]. It is generally recognized that the density of defect states in the polysilicon is continuous across the forbidden band gap [6], and the deep-states and the tail-states have different effects on the characteristics of polysilicon TFT's [2]–[5]. Migliorato and Meakin [2] found that the deep-states associated with dangling bonds result in high generation rates and anomalous off current, while the tail-states associated with the local disorder pin the Fermi-level and lead to a high threshold voltage and a low field effect mobility. From the on-state current simulation, A. Ono *et al.* [5] obtained the same results. On the other hand, different relationship was reported by B. A. Khan *et al.* [4] and I.-W. Wu *et al.* [3]. They found that the leakage current is dominated by the tail state density. In this brief, the correlation of polysilicon TFT characteristics to defect states is studied through post-hydrogenation thermal annealing. Experimentally, it is found that the deep states which affect the threshold voltage (V_{th}) and subthreshold swing (S) recover quickly under the thermal annealing, and the tail states which influence the leakage current (I_{off}) and field effect mobility (μ) respond slowly to the thermal annealing.

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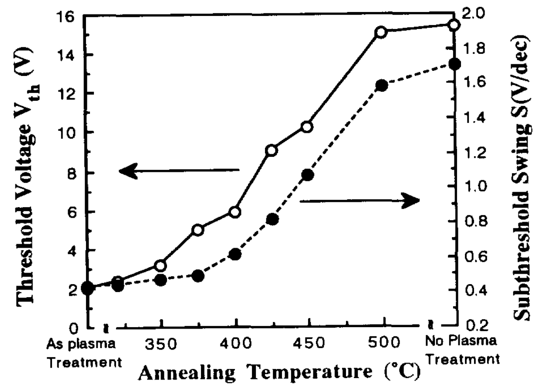
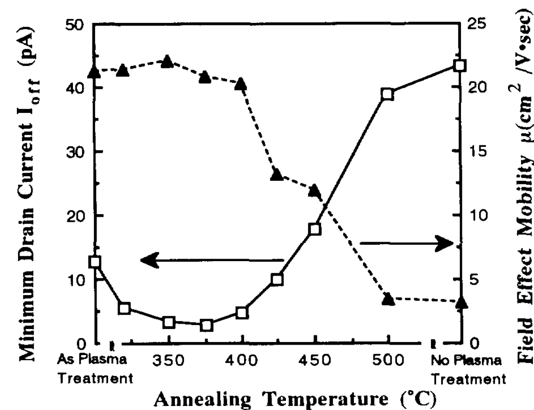


(a)



(b)

Fig. 1. The variation of (a) threshold voltage and subthreshold swing, and (b) minimum drain current measured at $V_d = 5$ V and field effect mobility after thermal annealing at the temperature range from 320°C to 500°C. The characteristics of as plasma-treated and no plasma-treated devices are also shown for comparison.

II. EXPERIMENTS

Amorphous silicon films of thickness 1100 Å were deposited on thermally oxidized silicon wafers by a low-pressure chemical vapor

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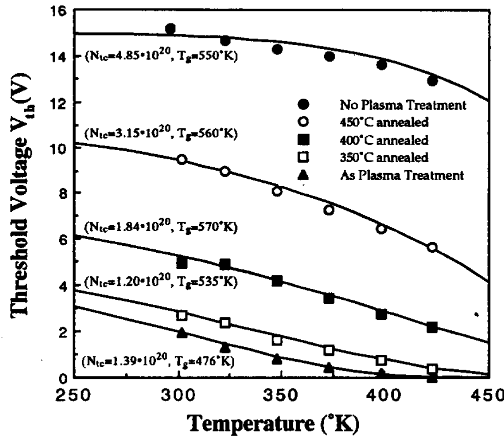

Fig. 2. The experimental (symbols) and calculated results (solid lines) of $V_{th}(T)$ for as plasma-treated, 350°C, 400°C, 450°C annealed and no plasma-treated devices. The derived $N_{tc}(\text{cm}^{-3}\ \text{eV}^{-1})$ and T_g values are also shown for each device.

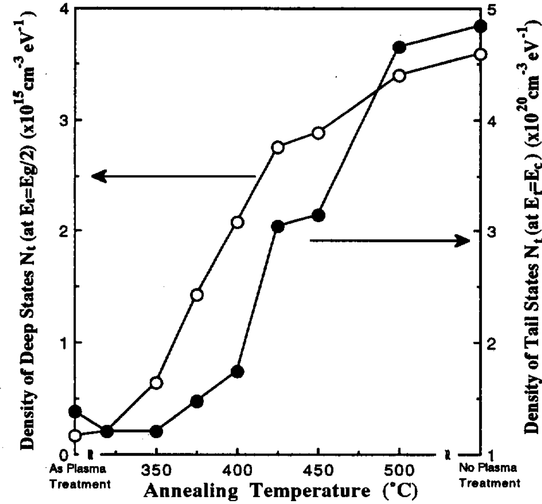

Fig. 3. The derived values of the density of deep-states N_t (at $E_t = E_g/2$) and tail-states N_t (at $E_t = E_c$) with respect to the annealing temperature.

deposition (LPCVD) system at 550°C. The wafers were then annealed at 550°C for 48 hours in an N_2 ambient to transform the film to polysilicon. After defining the active islands, 750 Å gate oxide was grown in dry O_2 at 1000°C . Another 3500 Å polysilicon film was then deposited at 625°C by the LPCVD system to be the gate electrode. After defining the gate length,5 × 10^{15} cm^{-2} phosphorous was implanted to dope the source, drain and gate. The dopants were activated at 900°C for 30 min in N_2 gas. Hydrogenation was performed in a commercial 13.56 MHz parallel-plate plasma reactor with H_2 and N_2 gas mixture at 300°C for 30 min. All wafers were then covered with 5000Å plasma-enhanced chemical vapor deposition (PECVD) SiO_2 for passivation. Contact holes were opened, and Al +1%Si was deposited and then patterned. Finally, the wafers were subjected to thermal annealing at the temperature range of 320°C–500°C for 30 min in N_2 ambient.

III. RESULTS AND DISCUSSIONS

The threshold voltage (V_{th}) and subthreshold swing (S) and the minimum drain current (I_{off}) and field effect mobility (μ) after thermal annealing for different annealing temperatures are plotted in Fig. 1 (a) and (b), respectively. The field effect mobility is measured in the linear region at $V_d = 0.1$ V, and at the maximum transconductance. The V_{th} increases with the annealing temperature and the S increases slightly at the low annealing temperature (< 375°C) and increases rapidly at the higher annealing temperature. For I_{off} and μ, they do not respond to the thermal annealing until the annealing temperature is greater than 375°C. These two different types of responses of device parameters to the annealing imply that different kinds of defect states are involved during the annealing. From the data of Fig. 1 (a) and (b), it can be derived that V_{th} and S are related to the same type of defect states which recover quickly under the annealing, and I_{off} and μ are related to another type of defect states which have a stronger S-H bonding and recover only at the annealing temperature above 375°C. It had been experimentally demonstrated that for the band tail states [6], the density of defect states (N_t) can be expressed in an exponential form in the energy bandgap as $N_t(E_t) = N_{tc} \cdot \exp[(E_t - E_c)/\ kT_g]$, where the N_{tc} is the defect state density at conductance band E_c, E_t is the energy level of the defect state and T_g is a characteristic parameter of defect states. Using the above exponential distribution of defect states, Fortunato and Migliorato [7] developed an analytical expression for the threshold voltage:

$$V_{th} = \frac{t_{ox}}{\varepsilon_{ox}} \left(\frac{q \cdot N_c}{k \cdot T_g \cdot N_{tc}} \right)^{\frac{T}{2(T-T_g)}} \times \left(\frac{2\varepsilon_s}{q} \cdot N_{tc} \cdot (k \cdot T_g)^2 \cdot \left(1 + \frac{T}{T_g}\right)\right)^{\frac{1}{2}} \quad (1)$$

where t_{ox} is the thickness of the gate oxide and T is the temperature. This value is very close to the extracted value from the intercept on the voltage axis of the straight line in the drain current I_d versus the gate voltage V_g plot [7]. Equation (1) can be fitted with our experimental data for V_{th} measured at the temperature range of 28°C ~ 150°C for our TFT's annealed at different temperatures. These fittings are shown in Fig. 2, and the derived N_{tc} and T_g values are also shown for each device. A good agreement with the experiment is found. The derived values for T_g are in the range of 476°K to 570°K which are very closed to the values reported in the literature [6]. The extracted values for the deep-state and tail-state density are plotted in Fig. 3 with respect to the annealing temperature. It can be seen that the tail-state density does not respond, in fact, decreases slightly, to the annealing until the annealing temperature reaches 375°C. This behavior is very consistent with those of I_{off} and μ of Fig. 1 (b), where I_{off} and μ decreases and increases slightly respectively in the temperature range of 320°C and 350°C and then increases and decreases respectively after the annealing temperature exceeds 375°C. While the deep-state density, which is defined as the N_t (at $E_t = E_g/2$), increases quickly with the annealing temperature. This behavior is the same as those of V_{th} and S of Fig. 1 (a). This observed correlation of TFT characteristics to defect states can be explained as follows: As the device is operated from the OFF-state to the ON-state, the surface Fermi-level will move from the position of bulk Fermi-level toward E_c. If there are deep states, the gate-induced carriers will be trapped by these deep-states. Hence, V_{th} as well as the subthreshold swing S are affected. As the device is fully turned on, the surface Fermi-level will move close to E_c. At this moment, it is the mobility which is affected by the tail states since the ON-state current is mainly determined by the mobility.

IV. Conclusion

The correlation of the electrical characteristics of polysilicon TFT to defect states has been studied through the post-hydrogenation thermal annealing. It is found that V_{th} and S degrade quickly after annealing above 320°C for 30 min through the recovery of mid-gap deep-states, while I_{off} and μ respond slowly to annealing through the recovery of tail-states.

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The Effects of Metal-n^+ Interface and Space Charge Limited Conduction on the Performance of Amorphous Silicon Thin-Film Transistors

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***Abstract*—We derive a contact current density expression that accounts for both the metal-n^+ film interface resistance and the space charge limited conduction in amorphous silicon thin-film transistors. Our model demonstrates that the metal-n^+ interface behavior dominates over space charge limited conduction for the a-Si:H film thicknesses used in pixel switching.**

I. Introduction

Amorphous silicon thin-film transistors (a-Si:H TFT's) form the basic building block for contact image sensors and active matrix LCDs. In such applications the resistances associated with the source and drain contacts significantly affect the TFT performance. Fig. 1(a) shows that an overlap exists between the source/drain contacts and the gate. The behavior of the TFT is independent of the overlap length, d_{OL}, provided that the overlap is longer than a critical length of approximately 1 μm [1]. In this work d_{OL} is assumed to be longer than this critical overlap length. The inverted channel current density, J (A/cm), flows at the gate-insulator/semiconductor interface. Within the gate-contact overlaps the *contact limited current per unit contact area*, J_y (A/cm^2), flows vertically between the contacts and the channel. J_y is a function of the space charge limited (SCL) conduction through the intrinsic a-Si:H layer and the resistance of the metal-n^+ layer interface. The former was shown to be the dominant factor for a-Si:H layer thicknesses of ≈0.2–0.3 μm [1]. Consequently, workers have ignored the interface resistance when formulating device models [2]–[4]. In this brief we develop an expression for J_y that accounts for both resistances. We then investigate the independent effects of the interface resistance and the SCL conduction on the TFT current by incorporating our J_y expression into a full TFT model.

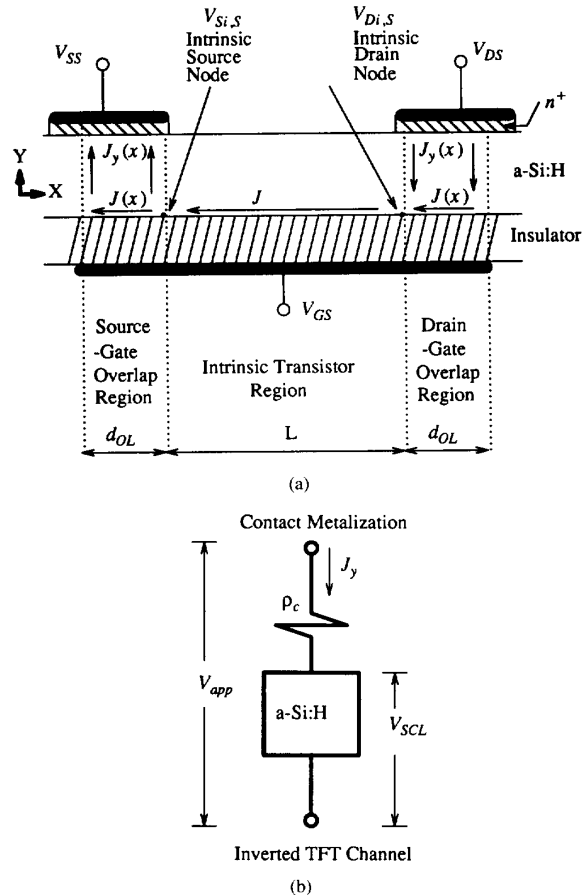

Fig. 1. (a) An idealized TFT structure showing the three regions of the TFT: two gate-contact overlap regions and an intrinsic TFT region. $J(x)$ flows horizontally in the inverted channel while $J_y(x)$ flows vertically between the channel and the contact metallizations. (b) A simple model representing the contact resistances.

Although a Schottky barrier is formed at the metal-n^+ interface, measurements have shown that it may be modeled as an ohmic element [5]. In this work we assume an ohmic contact with a

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