Analog Integr Circ Sig Process (2011) 66:1–7
DOI 10.1007/s10470-010-9520-6

Linear low voltage nano-scale CMOS transconductor

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Received: 16 August 2009 / Revised: 23 July 2010 / Accepted: 5 August 2010 / Published online: 18 August 2010

Abstract This paper presents a high linearity MOSFET-only transconductor based on differential structures. While a precise BSIM4 transistor model is introduced through analysis, the linearity can be improved by mobility compensation techniques as the device size is scaled down in the nano-scale CMOS technology. When the compensation utilizes transistors in subthreshold region, rather than the transistors in saturation region, the value of transconductance can be maintained. The circuit is fabricated in TSMC 0.18-μm CMOS process. The measurement results show 18 dB improvement of the proposed version, and 65 dB HD3 can be achieved for a 2.1 MHz 700 mV_{pp} differential input. The static power consumption under 1-V power supply voltage is 183 μW. Measurement results demonstrate the agreement with theoretical analyses.

Keywords Transconductor · Subthreshold · THD

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1 Introduction

The transconductor is an important building block in the analog signal processing circuits, such as analog filters, data converters, voltage controlled oscillators, and multipliers [1]. The main function of the transconductor is to convert the voltage applied to the input terminals into current at output nodes, and the building block is generally referred as a V–I converter. The linearity of the voltage-to-current conversion should usually be maintained because the linearity of the transconductor would determine the linearity of the overall system. However, this feature is getting harder to achieve, especially with the low supply voltage.

In recent years, numerous linearization techniques have been designed and reported [2–4]. The passive resistor, which is often implemented by the poly-silicon in the CMOS process, would be used in the high linearity transconductor circuit. Unfortunately, the use of passive resistors would cost larger area and it does not allow continuous transconductance tuning even using an array of resistors. Therefore, the transconductors with MOSFET-only configuration was developed. In such a configuration, the linearity of the architecture is limited to below 50 dB owing to the non-ideal characteristic of the active device. Moreover, the degradation of linearity happens for small feature sizes of MOS transistors due to the influence of second-order effects, like velocity saturation and mobility reduction, under nano-scale CMOS technology [5].

In the paper, the design of a low distortion under low supply voltage transconductor is presented. The proposed high linearity transconductor by using mobility compensation technique in the differential structure is discussed in Sect. 2. In Sect. 3, the measurement results of the proposed transconductor are discussed. Finally, some conclusions are presented in Sect. 4.

2 Operational transconductor amplifier

2.1 Review of the conventional transconductors

Figure 1(a) shows the conventional transconductor, where the voltage-to-current conversion is obtained by using an operational amplifier through a passive resistor. The current is then sensed and mirrored to the output node. For the MOSFET-only configuration, a single transistor under linear region operation, shown in Fig. 1(b), is used to replace the passive resistor. When the NMOS operates in the linear region, the drain current can be given, and the voltage-to-current relationship in Fig. 1(b) can be obtained as follows

$$I_{D,lin} = K_{lin}(V_{GS} - V_{thn})V_{DS} - \frac{1}{2}K_{lin}V_{DS}^2 \quad (1)$$

where $K_{lin} = \mu_n C_{ox}(W/L)$, W and L are the width and length of the device, respectively, C_{ox} is the oxide capacitance per unit channel area, μ_n is the low-field mobility, and V_{thn} is the NMOS threshold voltage. In the BSIM1 model, the mobility reduction effect is given by $\mu_n = \mu_0/[1 + \theta(V_{GS} - V_{th})]$, where μ_0 is the zero filed mobility of carriers and θ is the mobility reduction parameter. V_{GS} and V_{DS} are the gate-to-source and drain-to-source voltage, respectively.

We can find that the output current would not hold a linear relationship to the input voltage owing to the additional second term in (1), which thus degrades the linearity of the transconductor. Previous research reports that another transistor could be added to cancel out the second term in (1) based on the large signal square-law equation in the saturation region, and the −40 dB total harmonic distortion (THD) was achieved [6]. However, the technique needs extra operational amplifiers, which implies much more power consumption. Besides, it would not work well in the modern nano-scale CMOS technology owing to that the short channel effect would largely affect the ideal characteristic of the square-law behavior.

Although the technique reported in [6] is not suitable to provide the high linearity and low power transconductor in modern nano-scale CMOS process, we can take the circuit in Fig. 1(b) to become the differential version. As shown in Fig. 2, the simple operational amplifiers are formed by transistors M1 to M2, M3 to M4, and level shifter circuits. While transistors M7 and M8 operate in the linear region, the input voltage variation can be passed down to the source of transistors M5 and M6, and converted by transistors M7 and M8 for one voltage-to-current conversion path. We should note that the V_{sf} voltage is composed by simple source follower. Therefore, the second term in (1) can be cancelled out by inherent differential structure, and the linear relationship would be given by

$$I_{out} = \frac{K_{lin}(V_{GS} - V_{thn})}{1 + \theta(V_{GS} - V_{thn})}V_{in} \quad (2)$$

The equation shows that the linear voltage-to-current conversion could be obtained by taking short channel effects into consideration. Unfortunately, high order nonlinearity components still occur in the V–I conversion, especially for our nano-scale technology because (1) is resulted from the analysis of an approximation.

2.2 The transconductor by using transistors in saturation region

Figure 3 shows the transconductor by using transistors in saturation region [7]. To see how the circuit works, we should at first deal with the drain current of the linear

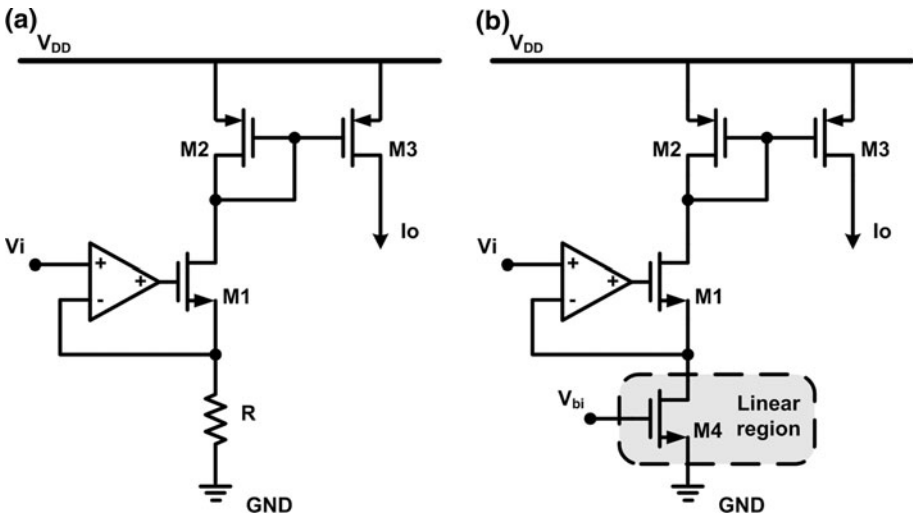

Fig. 1 **a** The conventional transconductor. **b** The MOSFET-only transconductor

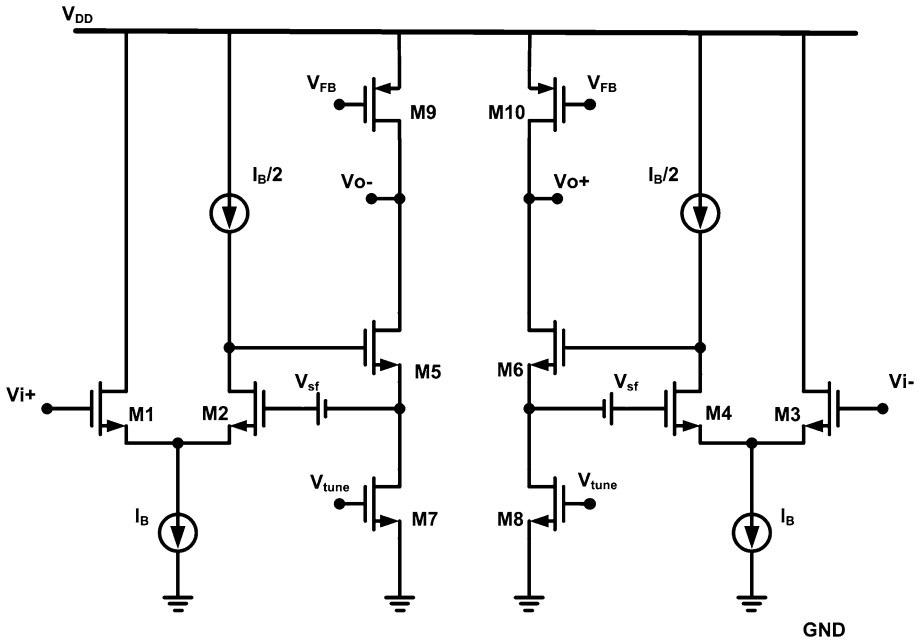

Fig. 2 The differential transconductor

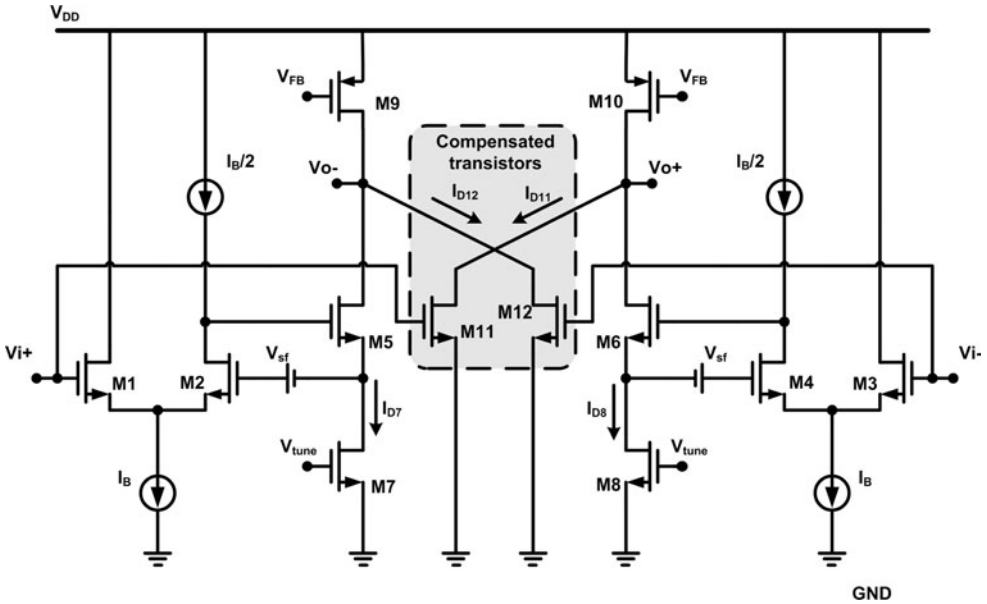

Fig. 3 The modified transconductor by using saturated transistors

region transistor in more details. A precise LEVEL 54 BSIM4 transistor model is expressed as [8]

$$I_{D,lin} = K_{lin}\left[\frac{(V_{GS}-V_{thn})V_{DS}-\frac{1}{2}\alpha V_{DS}^2}{1+\theta(V_{GS}-V_{thn})}\right] \times \left\{1+\frac{R_{eq}K_{lin}}{V_{DS}}\left[\frac{(V_{GS}-V_{thn})V_{DS}-\frac{1}{2}\alpha V_{DS}^2}{1+\theta(V_{GS}-V_{thn})}\right]\right\}^{-1} \quad (3)$$

where R_{eq} is the default device equivalent resistance in the linear region. In the equation, the value of α would be set to one for simplification. In the BSIM4 model, parameters UA and UB are the coefficients of the first and second order mobility degradation due to a vertical field. In this paper, we choose $\theta = \tau \times$ UA, where τ is a constant parameter relative to device length. The coefficient UB of the second order mobility degradation is not considered here due to smaller impact in distortion terms.

By giving $V_{GS,7} = V_{GS,8} = V_{tune}$, $V_{DS,7} = V_{cm} + v_d/2$, and $V_{DS,8} = V_{cm} - v_d/2$, where V_{cm} is the input common-mode voltage and v_d is the differential voltage, we can derive the differential voltage-to-current characteristic of MOS transistors M7 and M8. To analyze the linearity of the V_{DS} voltage against the drain current, a Taylor series expansion is used and then the relationship would be expressed by

$$I_{D,lin} = I_{D7} - I_{D8} = a_{1,lin}v_d + a_{2,lin}v_d^2 + a_{3,lin}v_d^3 + a_{4,lin}v_d^4 + \cdots \quad (4)$$

where

$$a_{1,lin} = \frac{K_{lin}\{R_{eq}K_{lin}V_{cm}^2 + 4(V_{DD} - V_{th} - V_{cm})[1 + (R_{eq}K_{lin} + \theta)(V_{DD} - V_{th})]\}}{\{2 + R_{eq}K_{lin}[2(V_{DD} - V_{th}) - V_{cm}] + 2(V_{DD} - V_{th})\theta\}^2}$$

$$a_{3,lin} = \frac{-4R_{eq}K_{lin}^2[1 + \theta(V_{DD} - V_{th})][1 + (R_{eq}K_{lin} + \theta)(V_{DD} - V_{th})]}{\{2 + R_{eq}K_{lin}[2(V_{DD} - V_{th}) - V_{cm}] + 2(V_{DD} - V_{th})\theta\}^4}$$

In the equation, the even-order harmonic terms can be cancelled out by the differential structure. In real circuit implementation, the matching can be maintained by carefully layout technique, and a value of less than 2% can be achieved. Thus the third-order harmonic distortion would become the dominant component.

In this transconductor, the other saturation region transistors based on the differential structure are used to compensate the third-order harmonic distortion. The concept of the topology comes from that the output current of the saturated transconductor in the differential pair also suffers the problems of short channel effects as the feature size of the transistors is chosen to be small, and thus the output current is given by

$$I_{D,sat} = \frac{K_{sat}(V_{GS} - V_{th})^2}{2[1 + \theta(V_{GS} - V_{th})]} \quad (5)$$

where K_{sat} is the device parameter of saturation region transistors. By giving $V_{GS,11} = V_{cm} + v_d/2$, and $V_{GS,12} = V_{cm} - v_d/2$, a Taylor series expansion is introduced and then the voltage-to-current relationship would be expressed by

$$I_{D,sat} = I_{D11} - I_{D12} = a_{1,sat}v_d + a_{2,sat}v_d^2 + a_{3,sat}v_d^3 + a_{4,sat}v_d^4 + \cdots \quad (6)$$

where

$$a_{1,sat} = \frac{K_{sat}(V_{cm} - V_{th})V_{thn}[2 + \theta(V_{cm} - V_{th})]}{[1 + \theta(V_{cm} - V_{th})]^2}$$

$$a_{3,sat} = \frac{-K_{sat}\theta}{[1 + \theta(V_{cm} - V_{th})]^4}$$

We can find that the dominant distortion of the saturation region transistor occurs due to the short channel effects in the third-order harmonic component under the topology of the differential structure. The introduced transistor in the saturation region seems to provide another distortion term. However, although the third-order harmonic terms of (4) and (6) have the same signs, we can put the output node of saturation region transistors in the opposite position as corresponding to the linear region transistors. Thus, when fixed values of parameters are given, the aspect ratios of compensated transistors can be found to achieve a highly linear voltage-to-current conversion. However, the main disadvantage of the modified circuit is the reduced transconductance.

2.3 The modified transconductor by using transistors in subthreshold region

In order to maintain a large transconductance value with the high linearity performance, subthreshold region transistors are used to replace saturation region transistors as shown in Fig. 4. By giving a voltage shifter to make sure the subthreshold operation, the drain current of the subthreshold region transistors can be expressed as

$$I_{D,sub} = I_0\left(\frac{W_w}{L_w}\right)e^{\frac{V_{GS}}{\xi V_T}}\left(1 - e^{\frac{-V_{DS}}{V_T}}\right) \quad (7)$$

where W_w and L_w are the width and length of the device, respectively, I_0 is the process-dependent parameter, ξ is the subthreshold slope factor, and V_T is the thermal voltage. Again, a Taylor series expansion is introduced while the voltage follower is well maintained, and then the voltage-to-current relationship would be expressed by

$$I_{D,sub} = I_{D11} - I_{D12} = a_{1,sub}v_d + a_{2,sub}v_d^2 + a_{3,sub}v_d^3 + a_{4,sub}v_d^4 + \cdots \quad (8)$$

where

$$a_{1,sub} = \frac{I_0}{\xi V_T}\left(\frac{W_w}{L_w}\right)e^{\frac{V_{cm} - V_{sf}}{\xi V_T}}$$

$$a_{3,sub} = \frac{I_0}{24(\xi V_T)^3}\left(\frac{W_w}{L_w}\right)e^{\frac{V_{cm} - V_{sf}}{\xi V_T}}$$

The third-order harmonic distortion term would be decreased by smaller device width and smaller input common-mode voltage. In the 0.18-μm CMOS process,

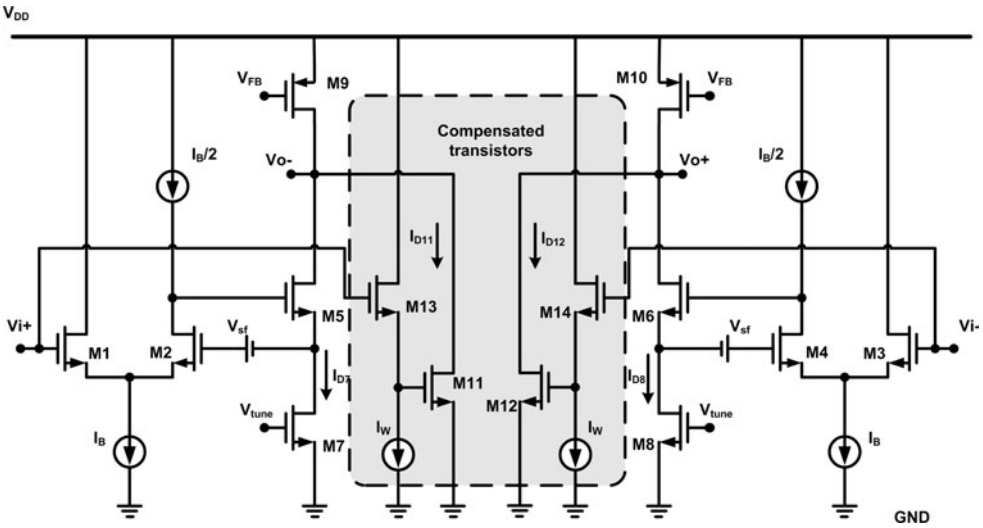

Fig. 4 The modified transconductor by using subthreshold region transistors

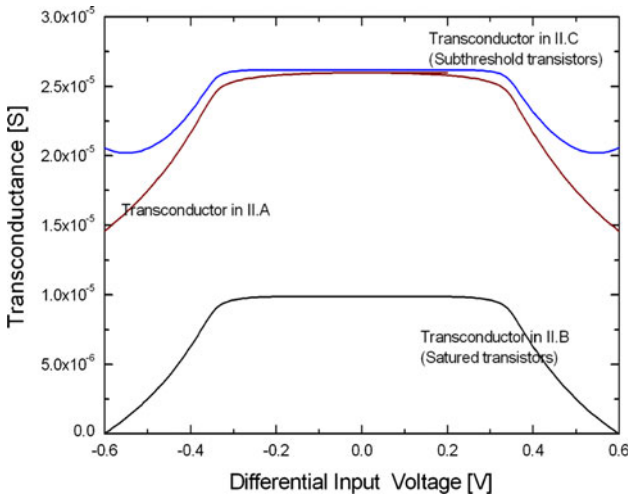

Fig. 5 The simulated G_m ranges of the proposed transconductors

typical parameters are $V_{thn} = 0.54$ V, $V_{thp} = -0.65$ V, $\mu_n C_{ox} = 47\ \mu A/V^2$, $\theta = 0.095/V$, $V_T = 26$ mV, $I_0 = 43.54\ nA/V^2$, $\xi = 2.2$. In our simulation, the optimized value is achieved by giving $(W_w/L_w) = 14 \times (W_s/L_s)$, where W_s and L_s are the width and length of the saturation region transistor, respectively. When the optimal sizes are designed, the combined current would provide a higher transconductance with minimized third-order distortion term. In Fig. 5, large signal simulation shows the function of differential input voltage to transconductance variation, where the expected performance is shown and matched with theoretical prediction.

3 Experimental results

The chip was fabricated in TSMC 180-nm CMOS process. The chip micrograph is shown in Fig. 6 with the area less

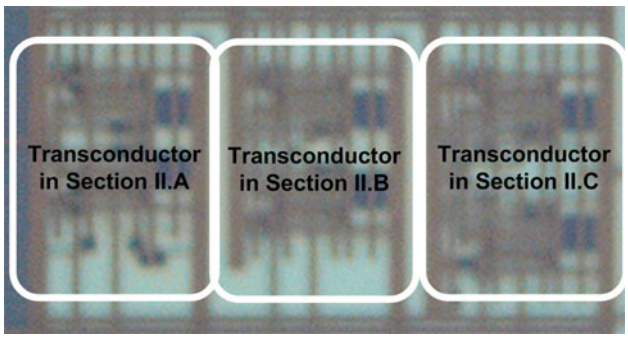

Fig. 6 The chip micrograph

than 27.1×10^{-3} mm^2. These three transconductors use almost the same area. A supply voltage of 1-V was employed over the circuits. The third-order harmonic distortion (HD3) measured with a sinusoidal tone of 0.7 V_{pp} amplitude at the speed of 2.1 MHz is shown in Fig. 7. Figure 7(a) shows the performance of the differential transconductor without any linearity enhancement circuit, and the measured HD3 of 47 dB is obtained. In Fig. 7(b), the HD3 is improved, but the transconductance decreases as well. Then, the HD3 in Fig. 7(c) is shown to about 65 dB, a 18 dB improvement with the same transconductance value as compared with Fig. 7(a). For the power consumption of the designed circuit, the nominal static power consumption of transconductor in Fig. 7(a)–(c) is 175, 180, and 183 μW, respectively. Thus, the linearity can be highly improved with less than 4% of the increased power.

4 Conclusions

A novel differential transconductor under nano-scale CMOS technology has been reported. It is based on the

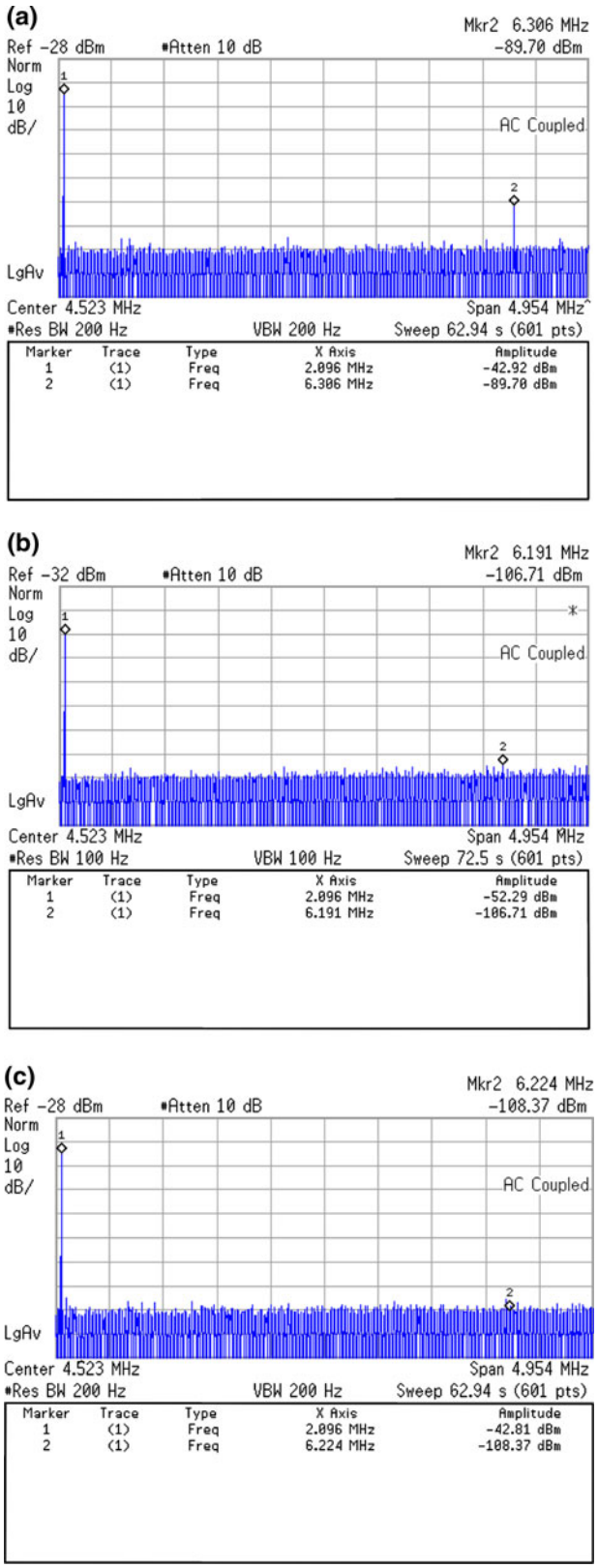

Fig. 7 Measured third-order harmonic distortion (HD3). **a** The differential transconductor. **b** The modified transconductor by using saturated transistors. **c** The modified transconductor by using subthreshold transistors

principle that the third-order harmonic distortion term could be cancelled by the addition of the two drain current, one in the linear region and the other in the subthreshold region, to improve the linearity while the transconductance is maintained. The technique employed leads to a significant improvement of the linearity performance in the voltage-to-current conversion in the MOSFET-only topology. We can conclude that the transconductor could be provided as a high linearity building block in low voltage applications.

Acknowledgment Authors would like to thank the National Chip Implementation Center of Taiwan for supporting the chip fabrication.

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