

Power-Efficient and Cost-Effective 2-D Symmetry Filter Architectures

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Abstract—This paper presents two-dimensional (2-D) VLSI digital filter structures possessing various symmetries in the filter magnitude response. For this purpose, four Type-1 and four Type-2 power-efficient and cost-effective 2-D magnitude symmetry filter architectures possessing diagonal, fourfold rotational, quadrantal, and octagonal symmetries with reduced number of multipliers and one power-efficient and cost-effective multimode 2-D symmetry filter are given. By combining the identities of the four Type-1 symmetry filter structures, the proposed multimode 2-D symmetry filter is capable of providing four different operation modes: diagonal symmetry mode (DSM), fourfold rotational symmetry mode (FRSM), quadrantal symmetry mode (QSM), and octagonal symmetry mode (OSM). The proposed diagonal, fourfold rotational, quadrantal, and octagonal symmetry filter structures can attain power savings of 16.77%, 36.30%, 22.90%, and 37.73% with respect to that of the conventional 2-D filter design without symmetry. On the other hand, the proposed DSM, FRSM, QSM, and OSM modes can reduce power consumption by 11.01%, 31.42%, 17.53%, and 35.26% compared with that of the conventional 2-D filter design. The proposed multimode filter can result in a 63.25% area reduction compared with the sum of the areas of the four individual Type-1 symmetry filter structures.

Index Terms—Cost effective, multimode, power efficient, symmetry filter, 2-D filter.

I. INTRODUCTION

TWO-DIMENSIONAL (2-D) digital filters are widely used in a variety of digital signal processing (DSP) systems such as image restoration [1], [2], image enhancement [3], frequency response analysis [4]–[7], and beamformer [8], [9]. Although 2-D digital filters can be simulated on a general purpose computer for the above applications, dedicated computing structures are needed in order to meet the high throughput demands. Several conventional very large scale integration (VLSI) architectures for 2-D filters have been studied in [10]–[12], and an existing application-specific integrated circuit (ASIC) approach has been applied to the design of beam filter [8], [9], 2-D diagonal symmetry filter [13], [14], and fourfold rotational symmetry filter [15]. Recently the authors have presented 2-D digital filter architectures with separable denominators [13]. The significant feature of filters studied in [13] is that they exhibit the denominator separability as a

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filter structural property. This means that the separability of the denominator is maintained independent of the choice of multiplier values. This important property is essential for the design of the multimode symmetry filter discussed in this paper. In addition, the denominator separability is a requirement for the stability of quarter-plane 2-D transfer functions possessing quadrantal, fourfold rotational, and octagonal magnitude symmetries. Further, the filter architectures in [13] are shown to realize the filters possessing diagonal symmetry and separable denominators with fewer multipliers than other architectures presented in [14] and [15]. Thus, all the above indicates that the separable structures in [13] are highly suitable for the design of 2-D filters possessing various magnitude symmetries.

It is well-known that symmetry presented in the frequency responses of 2-D filters can be used to reduce the number of multipliers [5]–[7]; however, the corresponding 2-D filter architectures have not been fully explored. In this paper, eight power-efficient and cost-effective symmetry filter architectures based on the structures in [13] are presented (four Type-1 and four Type-2). They possess diagonal, fourfold rotational, quadrantal, and octagonal symmetries, and require less number of multipliers. Further, in order to integrate the support of multiple symmetry functions, one power-efficient and cost-effective Type-1 multimode 2-D filter design with four symmetries is proposed. The new multimode structure providing four modes can attain power reduction by 11.01%, 31.42%, 17.53%, and 35.26% compared with that of the conventional 2-D filter design without symmetry [12].

This paper is organized as follows. Section II briefly reviews the separable denominator filter transfer function and proposes the corresponding Type-1 and Type-2 structures. In Section III, four Type-1 and four Type-2 cost-effective symmetry filter structures with less number of multipliers are presented. The generalized design procedure of the Type-1 and Type-2 symmetry filters is addressed. A cost-effective Type-1 multimode filter architecture with four symmetries is discussed in Section IV. The power consumption and core area of the proposed symmetry filter structures and the multimode filter architecture are profiled and evaluated in Section V. Finally, the conclusions are given in Section VI.

II. PRELIMINARIES OF SEPARABLE DENOMINATOR FILTER

The general transfer function of a 2-D IIR quarter-plane digital filter can be represented as

$$H(z_1, z_2) = \frac{Y(z_1, z_2)}{X(z_1, z_2)} = \frac{\sum_{i=0}^{N_1} \sum_{j=0}^{N_2} a_{ij} z_1^{-i} z_2^{-j}}{\sum_{i=0}^{N_1} \sum_{j=0}^{N_2} b_{ij} z_1^{-i} z_2^{-j}} \quad (1)$$

where $X(z_1, z_2)$ and $Y(z_1, z_2)$ denote the input and output of the digital filter, respectively, a_{ij} and b_{ij} denote the numerator and denominator coefficients, respectively, and $b_{00} = 1$, $N_1 \times N_2$ is the order of the IIR digital filter. Throughout this paper, we

assume that an image $M_1 \times M_2$ is fed to the following structures in raster-scan mode, and thus the delay $z_2^{-1} = z^{-1}$ and $z_1^{-1} = z^{-M_2}$, where z^{-1} and M_2 denote a unit delay element and the width of an image, respectively. A separable denominator transfer function is adopted in this paper due to the following reasons. First, the separable denominator is needed in realizing stable 2-D magnitude responses possessing various symmetries [5]–[7] of quarter-plane filters with the exception of diagonal symmetry. Second, the stability of this transfer function is easy to detect by simply calculating the poles of the two one-dimensional (1-D) polynomials. Third, the transfer function with symmetry requires fewer multipliers to realize [5]–[7]. Consider the separable denominator transfer function described in (2)

$$H(z_1, z_2) = \frac{Y(z_1, z_2)}{X(z_1, z_2)} = \frac{\sum_{i=0}^{N_1} \sum_{j=0}^{N_2} a_{ij} z_1^{-i} z_2^{-j}}{\left(1 - \sum_{i=1}^{N_1} b_{i0} z_1^{-i}\right) \cdot \left(1 - \sum_{j=1}^{N_2} b_{0j} z_2^{-j}\right)}. \quad (2)$$

Without loss of generality, we can assume the filter order $N_1 = N_2 = N$. Since the fourfold rotational and octagonal symmetry filter structures are the same when $N = 2$, $N = 3$ is selected in the following proposed filter structures. The Type-1 separable denominator transfer function of the 2-D filter can be recast in (3)

$$H(z_1, z_2) = \frac{Y_1(z_1, z_2)}{X(z_1, z_2)} \cdot \frac{Y(z_1, z_2)}{Y_1(z_1, z_2)} \quad (3)$$

where $Y_1(z_1, z_2)/X(z_1, z_2)$ is defined in (4)

$$Y_1 = X + \sum_{i=1}^N b_{i0} z_1^{-i} Y_1 \quad (4)$$

where $X = X(z_1, z_2)$ and $Y_1 = Y_1(z_1, z_2)$. Thus, $Y(z_1, z_2)/Y_1(z_1, z_2)$ can be generally represented as follows:

$$Y = \sum_{i=0}^N \sum_{j=0}^N a_{ij} z_1^{-i} z_2^{-j} Y_1 + \sum_{j=1}^N b_{0j} z_2^{-j} Y \quad (5)$$

where $Y = Y(z_1, z_2)$. The proposed Type-1 3×3 2-D IIR filter with separable denominator is depicted in Fig. 1 [13]. It can be verified through Mason's Gain Formula [16] that the structures of Block 1 and Block 2 in Fig. 1 satisfy (4) and (5), respectively, with $N = 3$ (It is to be noted that to verify (5), one needs to always treat X as the input and to determine Y/X and Y_1/X . That gives the relationship between Y and Y_1 . This is true for all the structures discussed in this paper). Since the image is raster scanned, the delay $z_1^{-1} = z^{-M_2}$ is realized by a shift-register (SR) with size of M_2 .

Similarly, the Type-2 separable denominator transfer function of the 2-D filter can again be recast in (6) as

$$H(z_1, z_2) = \frac{Y_2(z_1, z_2)}{X(z_1, z_2)} \cdot \frac{Y(z_1, z_2)}{Y_2(z_1, z_2)} \quad (6)$$

where $Y_2(z_1, z_2)/X(z_1, z_2)$ is defined in (7)

$$Y_2 = X + \sum_{j=1}^N b_{0j} z_2^{-j} Y_2 \quad (7)$$

where $Y_2 = Y_2(z_1, z_2)$. Thus, $Y(z_1, z_2)/Y_2(z_1, z_2)$ can be generally represented as follows:

$$Y = \sum_{i=0}^N \sum_{j=0}^N a_{ij} z_1^{-i} z_2^{-j} Y_2 + \sum_{i=1}^N b_{i0} z_1^{-i} Y. \quad (8)$$

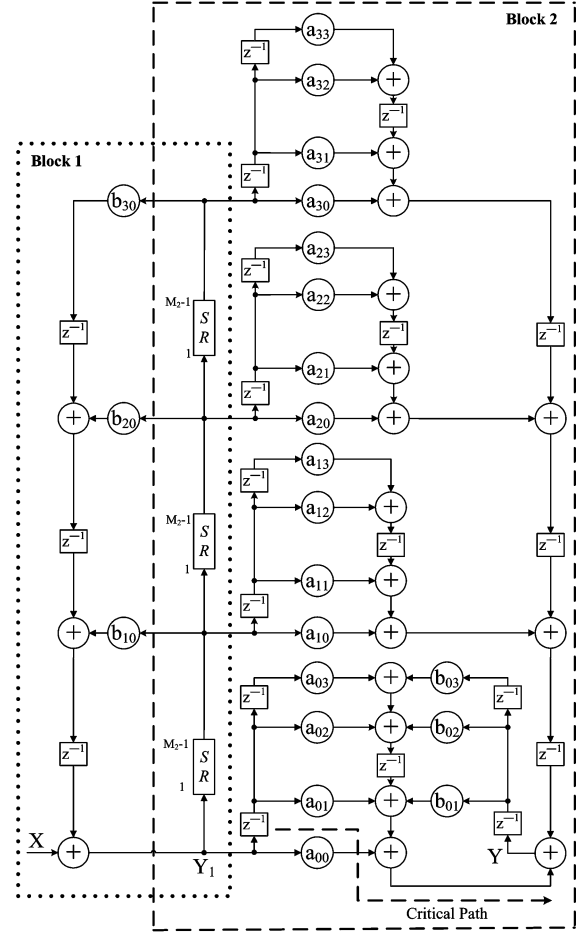


Fig. 1. Proposed Type-1 separable denominator 2-D IIR filter structure for $N = 3$ [13].

The proposed Type-2 3×3 2-D IIR filter with separable denominator is shown in Fig. 2 [13]. The structures of Block 3 and Block 4 in Fig. 2 satisfy (7) and (8), respectively, with $N = 3$. The reason for writing the transfer function in (2) in the form of (3) followed by (4) and (5) as well as (6) followed by (7) and (8) is to decompose the filter structure into the two blocks in Figs. 1 and 2. Also, note that the structure in Fig. 2 is obtained by taking the transpose of the structure in Fig. 1. Using the tree method mentioned in [12] to arrange the adders, the critical periods in Figs. 1 and 2 are analyzed as $T_m + 3T_a$ and $T_m + 2T_a$, respectively, where T_m and T_a denote the operation time required by the multiplier and adder, respectively.

III. COST-EFFECTIVE 2-D FILTER ARCHITECTURES WITH SPECIFIC SYMMETRY

The presence of symmetry in the 2-D frequency response can alleviate the design complexity of a 2-D digital filter. Symmetry in the frequency response induces certain relationship among the filter coefficients which can result in fewer multipliers in the implementation. In this section, we will design eight symmetry filter architectures with diagonal, fourfold rotational, quadrantal and octagonal symmetry property.

A. Diagonal Symmetry Filter Structure

A 2-D magnitude response possesses diagonal symmetry if $|H(z_1, z_2)| = |H(z_2, z_1)|$ with $z_1 = e^{j\theta_1}$ and $z_2 = e^{j\theta_2}$, $\forall (\theta_1, \theta_2)$ [5]–[7]. Assuming the separable denominator transfer function in (2) is adopted, it will have diagonal symmetry if

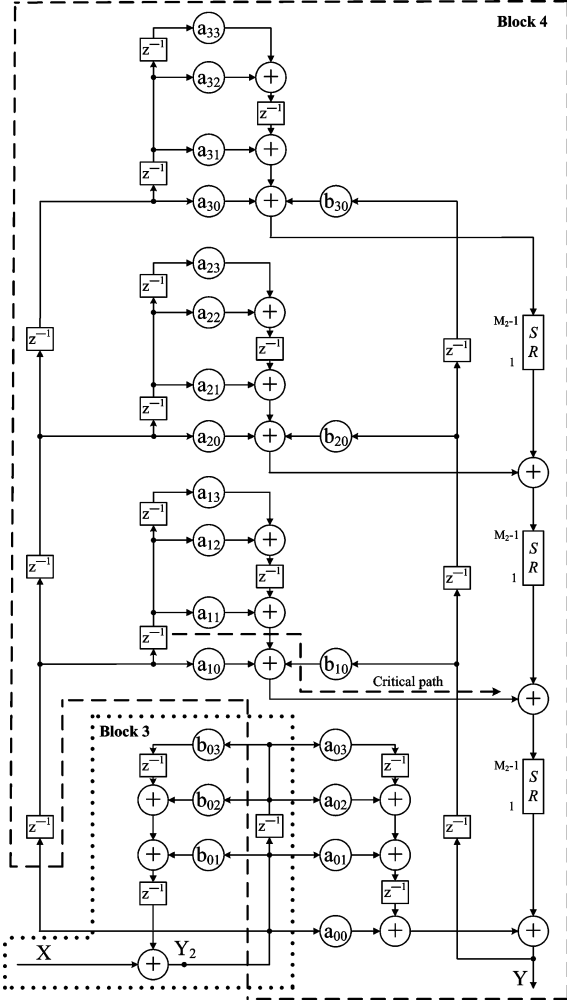


Fig. 2. Proposed Type-2 separable denominator 2-D IIR filter structure for $N = 3$ [13].

$a_{ij} = a_{ji}$ and $b_{k0} = b_{0k}$ for all i, j, k . Applying these constraints to the transfer function in (2), (4) and (5) can be recast in (9a) and (9b), respectively

$$Y_1 = X + \sum_{j=1}^N b_{0j} z_1^{-j} Y_1 \quad (9a)$$

$$Y = \sum_{j=1}^N b_{0j} z_2^{-j} Y + \sum_{i=0}^N a_{ii} z_1^{-i} z_2^{-i} Y_1 + \sum_{i=0}^{N-1} \sum_{j=i+1}^N a_{ij} (z_1^{-i} z_2^{-j} + z_1^{-j} z_2^{-i}) Y_1 \quad (9b)$$

and (7) and (8) can be recast in (10a) and (10b), respectively

$$Y_2 = X + \sum_{j=1}^N b_{0j} z_2^{-j} Y_2 \quad (10a)$$

$$Y = \sum_{j=1}^N b_{0j} z_1^{-j} Y + \sum_{i=0}^N a_{ii} z_1^{-i} z_2^{-i} Y_2 + \sum_{i=0}^{N-1} \sum_{j=i+1}^N a_{ij} (z_1^{-i} z_2^{-j} + z_1^{-j} z_2^{-i}) Y_2. \quad (10b)$$

According to (9a) and (9b) with $N = 3$, the Type-1 2-D diagonal symmetry filter structure with separable denominator is

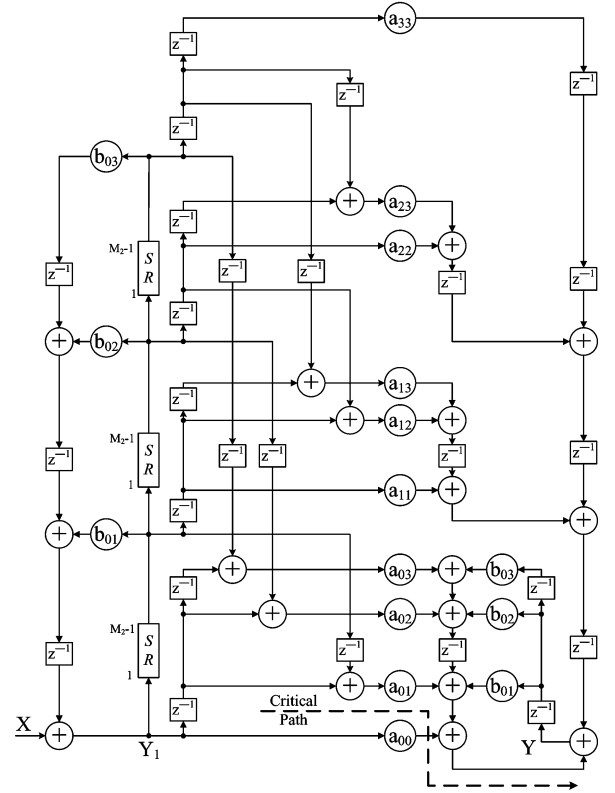


Fig. 3. Proposed Type-1 2-D diagonal symmetry filter structure with separable denominator for $N = 3$.

obtained and shown in Fig. 3. It can be shown that the structure satisfies (9a) as well as (9b) with $N = 3$. Similarly, in accordance with (10a) and (10b) with $N = 3$, the Type-2 2-D diagonal symmetry filter structure with separable denominator is obtained in Fig. 4. This structure satisfies (10a) as well as (10b) with $N = 3$. Using the tree method to arrange the adders, the critical paths are analyzed as $T_m + 3T_a$ and $T_m + 2T_a$ as shown in Figs. 3 and 4, respectively.

B. Fourfold Rotational Symmetry Filter Structure

For a 2-D magnitude response, if $|H(z_1, z_2)| = |H(z_2^{-1}, z_1)|$ with $z_1 = e^{j\theta_1}$ and $z_2 = e^{j\theta_2}$, $\forall (\theta_1, \theta_2)$, the filter possesses fourfold rotational symmetry [5]–[7]. With the separable denominator transfer function in (2), the following constraints on the coefficients will provide the required symmetry: $a_{ij} = a_{j(N-i)}$ and $b_{k0} = b_{0k}$ for all i, j, k . Applying these constraints to the transfer function in (2), (4) and (5) can be recast in (11a) and (11b), respectively

$$Y_1 = X + \sum_{j=1}^N b_{0j} z_1^{-j} Y_1 \quad (11a)$$

$$Y = \sum_{j=1}^N b_{0j} z_2^{-j} Y + v a_{uu} z_1^{-u} z_2^{-u} Y_1 + \sum_{i=0}^{u-v} \sum_{j=i}^{N-i-1} a_{ij} \times \left(z_1^{-i} z_2^{-j} + z_1^{-j} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-(N-j)} + z_1^{-(N-j)} z_2^{-i} \right) Y_1 \quad (11b)$$

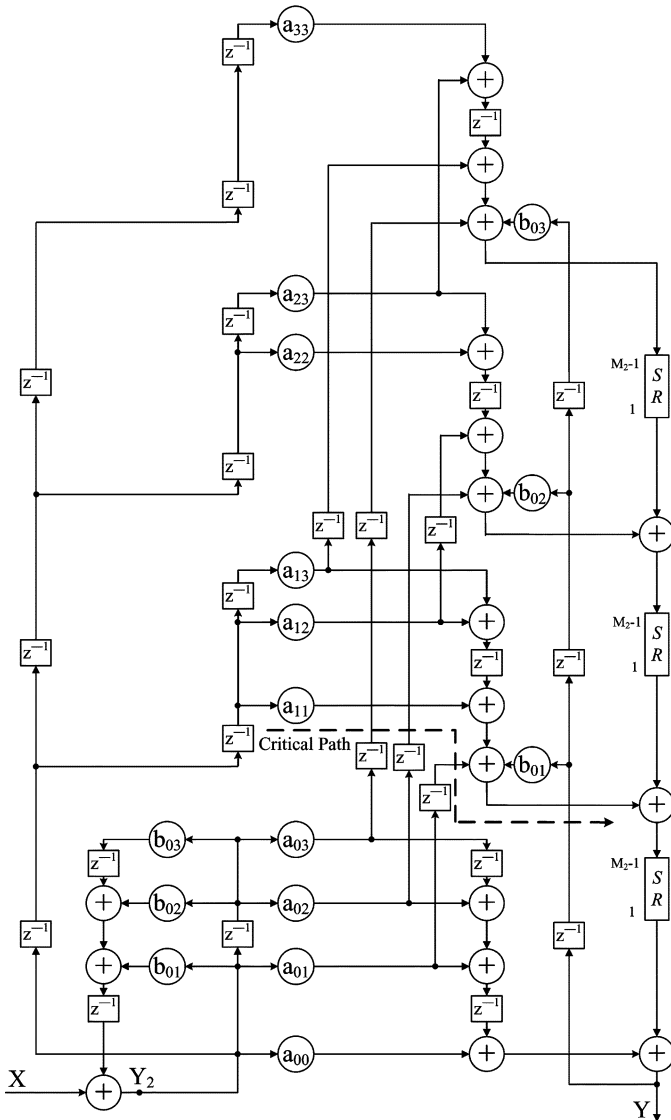


Fig. 4. Proposed Type-2 2-D diagonal symmetry filter structure with separable denominator for $N = 3$ [13].

and (7) and (8) can be recast in (12a) and (12b), respectively

$$Y_2 = X + \sum_{j=1}^N b_{0j} z_2^{-j} Y_2 \quad (12a)$$

$$Y = \sum_{j=1}^N b_{0j} z_1^{-j} Y + v a_{uu} z_1^{-u} z_2^{-u} Y_2 + \sum_{i=0}^{u-v} \sum_{j=i}^{N-i-1} a_{ij} \times \left(z_1^{-i} z_2^{-j} + z_1^{-j} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-(N-j)} + z_1^{-(N-j)} z_2^{-i} \right) Y_2 \quad (12b)$$

where $u = \lfloor N/2 \rfloor$ and $v = (N + 1) \bmod 2$. Note that $\lfloor \bullet \rfloor$ denotes the largest integer that is smaller than or equal to \bullet . In the case of $N = 3$, (11a)-(11b) and (12a)-(12b) can be realized by Type-1 and Type-2 2-D fourfold rotational symmetry filter structures with separable denominator given in Figs. 5 and 6,

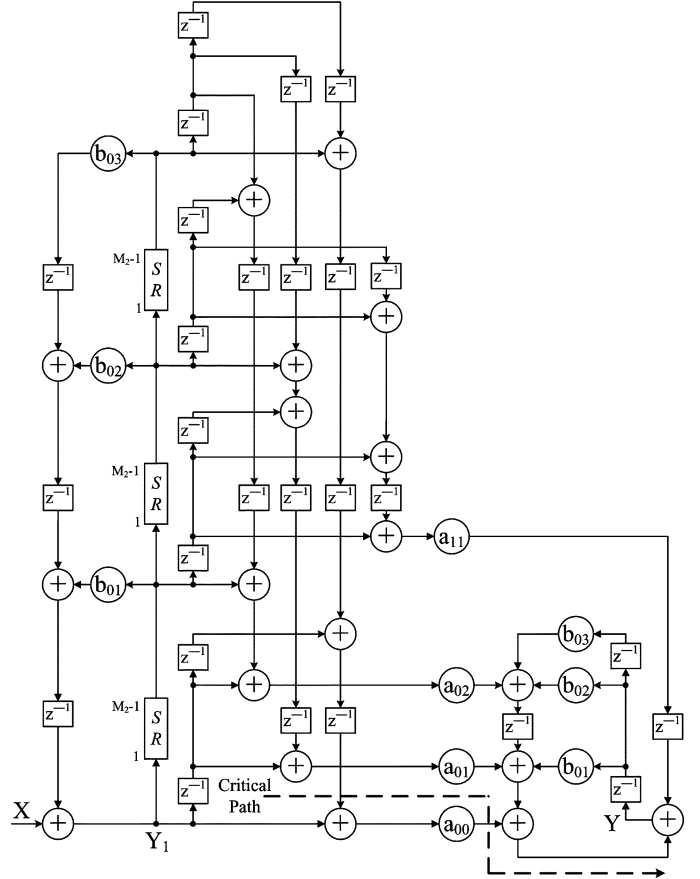


Fig. 5. Proposed Type-1 2-D fourfold rotational symmetry filter structure with separable denominator for $N = 3$.

respectively. It is easy to verify that the structure in Fig. 5 satisfies (11a) and (11b) with $N = 3$, and the filter structure in Fig. 6 satisfies (12a) and (12b). Using the tree method to arrange the adders, the critical paths are analyzed as $T_m + 3T_a$ and $T_m + 2T_a$ as shown in Figs. 5 and 6, respectively.

C. Quadrantal Symmetry Filter Structure

A 2-D magnitude response possesses quadrantal symmetry if $|H(z_1, z_2)| = |H(z_1^{-1}, z_2)|$ with $z_1 = e^{j\theta_1}$ and $z_2 = e^{j\theta_2}$, $\forall (\theta_1, \theta_2)$ [5]–[7]. Assuming the separable denominator transfer function in (2) is adopted, it will have quadrantal symmetry if $a_{ij} = a_{(N-i)j}$ and $b_{k0} = b_{0k}$ for all i, j, k . (Note that for quadrantal symmetry, b_{k0} need not be the same as b_{0k} ; but here they are assumed equal to ease the implementation of the multimode filter to be discussed later). Applying the constraints to the transfer function in (2), (4) and (5) can be recast in (13a) and (13b), respectively

$$Y_1 = X + \sum_{j=1}^N b_{0j} z_1^{-j} Y_1 \quad (13a)$$

$$Y = \sum_{j=1}^N b_{0j} z_2^{-j} Y + v \cdot \sum_{j=0}^N a_{uj} \left(z_1^{-u} z_2^{-j} \right) Y_1 + \sum_{i=0}^{u-v} \sum_{j=0}^N a_{ij} \left(z_1^{-i} z_2^{-j} + z_1^{-(N-i)} z_2^{-j} \right) Y_1 \quad (13b)$$

and (7) and (8) can be recast in (14a) and (14b), respectively

$$Y_2 = X + \sum_{j=1}^N b_{0j} z_2^{-j} Y_2 \quad (14a)$$

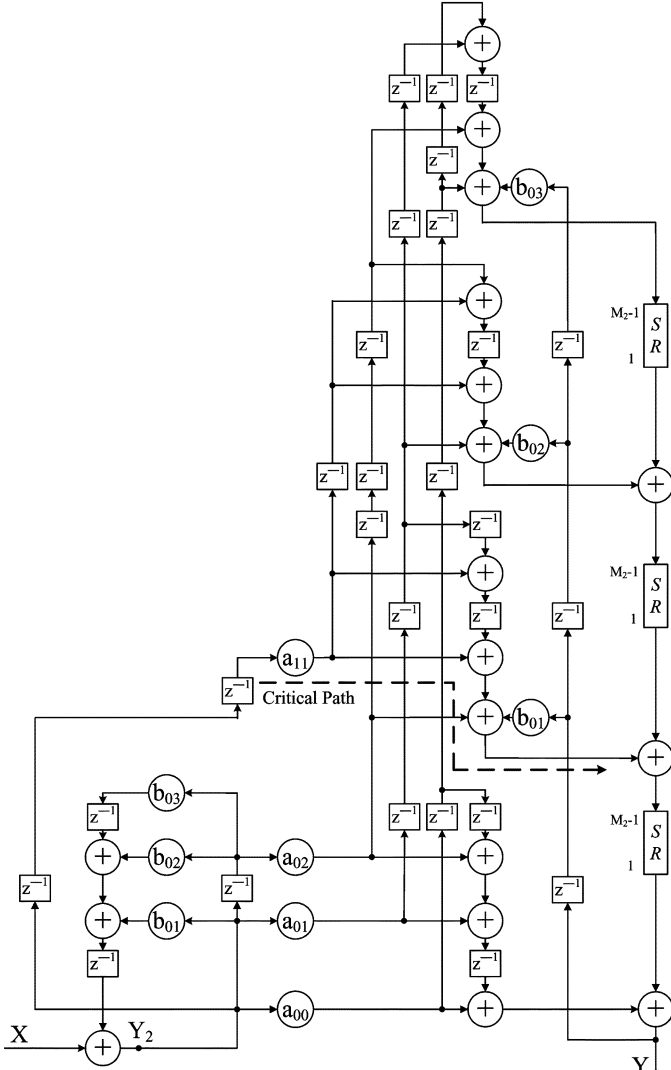


Fig. 6. Proposed Type-2 2-D fourfold rotational symmetry filter structure with separable denominator for $N = 3$.

$$Y = \sum_{j=1}^N b_{0j} z_1^{-j} Y + v \cdot \sum_{j=0}^N a_{uj} (z_1^{-u} z_2^{-j}) Y_2 + \sum_{i=0}^{u-v} \sum_{j=0}^N a_{ij} (z_1^{-i} z_2^{-j} + z_1^{-(N-i)} z_2^{-j}) Y_2. \quad (14b)$$

Taking into consideration (13a) and (13b) with $N = 3$, the Type-1 2-D quadrantal symmetry filter structure with separable denominator is realized as shown in Fig. 7. Similarly, in accordance with (14a) and (14b) with $N = 3$, the Type-2 2-D quadrantal symmetry filter structure with separable denominator is obtained in Fig. 8. Both architectures can be verified by Mason's Gain Formula. Using the tree method again to arrange the adders, the critical paths are analyzed as $T_m + 3T_a$ and $T_m + 2T_a$ as shown in Figs. 7 and 8, respectively.

D. Octagonal Symmetry Filter Structure

Octagonal symmetry is a combination of diagonal, fourfold rotational and quadrantal symmetries. Any two of the three symmetries are sufficient to guarantee that a 2-D magnitude response possesses octagonal symmetry [5]–[7]. Using the separable denominator transfer function in (2), the following constraints on the coefficients can be obtained as: $a_{ij} = a_{ji} =$

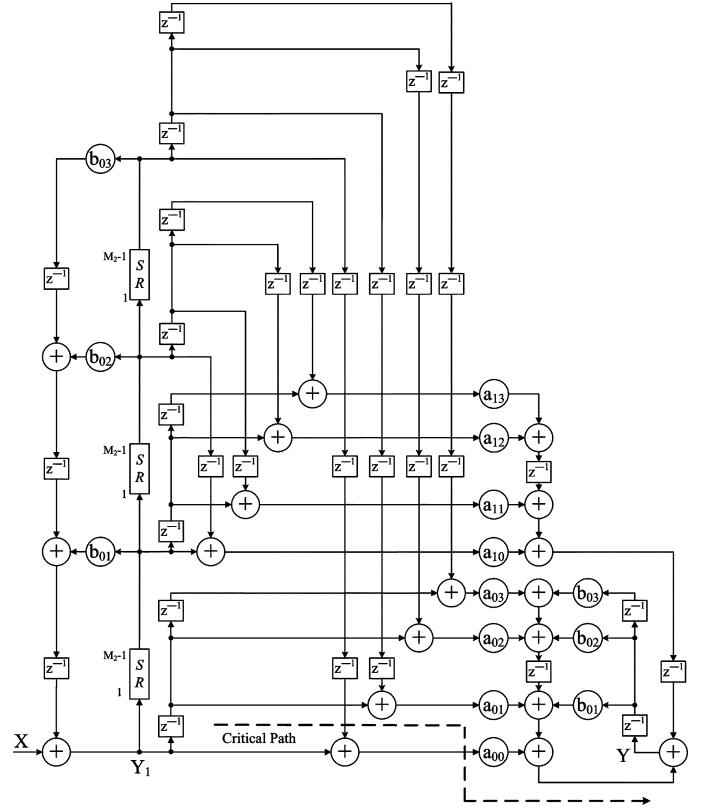


Fig. 7. Proposed Type-1 2-D quadrantal symmetry filter structure with separable denominator for $N = 3$.

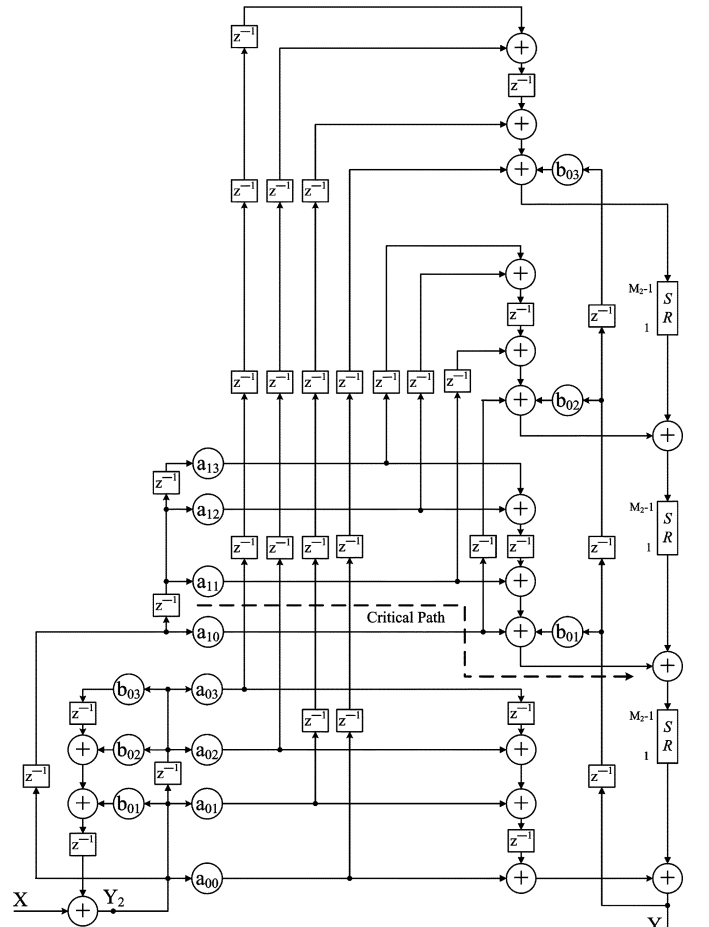


Fig. 8. Proposed Type-2 2-D quadrantal symmetry filter structure with separable denominator for $N = 3$.

$a_{(N-i)j}$ and $b_{k0} = b_{0k}$ for all i, j, k . Utilizing these constraints on the transfer function in (2), (4) and (5) can be recast in (15a) and (15b), respectively (see equation (15a)–(15b) at the bottom of the page) and (7) and (8) can be recast in (16a) and (16b), respectively (see equation (16a)–(16b) at the bottom of the next page). Considering the transfer function in (15a) and (15b) with $N = 3$, the Type-1 2-D octagonal symmetry filter structure with separable denominator is obtained in Fig. 9. Similarly, in accordance with (16a) and (16b) with $N = 3$, the Type-2 2-D octagonal symmetry filter structure with separable denominator is obtained in Fig. 10. Using the tree method to arrange the adders, the critical paths are analyzed as $T_m + 3T_a$ and $T_m + 2T_a$ as shown in Figs. 9 and 10, respectively. All eight cost-effective filter structures possess fewer multipliers, especially for the 2-D octagonal symmetry structures in Figs. 9 and 10 which have the lowest number of multipliers. The complete comparison is addressed in Section V.

Furthermore, concerning the symmetry filter structure for different order N , the generalized design procedure for the Type-1 symmetry filter is described as follows.

- Step 1: Determine the filter order N and symmetry property.
- Step 2: Determine the independent coefficients and transfer functions of Y_1/X and Y/Y_1 with specific value of N from the symmetry property.
- Step 3: Depict the structure of the Type-1 separable denominator 2-D IIR filter with specific value of N (e.g., Fig. 1 with $N = 3$) and replace the corresponding dependent coefficients using the independent coefficient.
- Step 4: According to the structure of the Type-1 separable denominator 2-D IIR filter and the transfer function of Y/Y_1 , the delay arrangement equation in terms of the sum of delays associated with one independent numerator coefficient can be obtained.
- Step 5: Based on the delay arrangement equation associated with the one independent numerator coefficient, the paths ahead of the replaced dependent coefficient multipliers in the Type-1 separable denominator 2-D IIR filter structure are cut and the cut signal paths

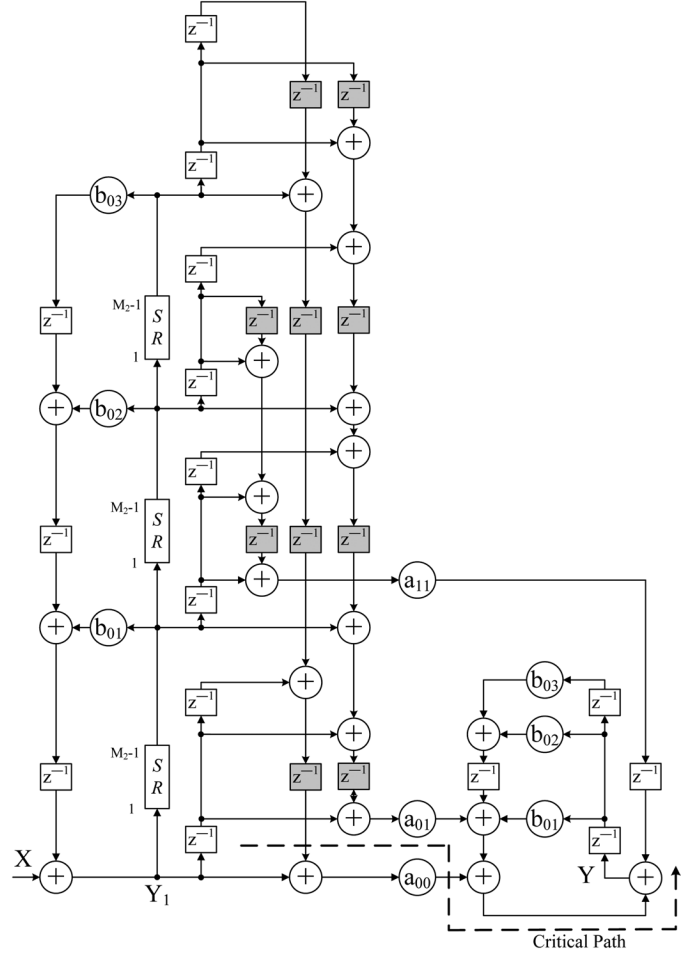


Fig. 9. Proposed Type-1 2-D octagonal symmetry filter structure with separable denominator for $N = 3$.

are added into the path before the independent numerator coefficient multiplier. Then, the replaced dependent numerator coefficient multipliers can be removed.

$$Y_1 = X + \sum_{j=1}^N b_{0j} z_1^{-j} Y_1 \quad (15a)$$

$$\begin{aligned}
Y &= \sum_{j=1}^N b_{0j} z_2^{-j} Y + v a_{uu} z_1^{-u} z_2^{-u} Y_1 \\
&+ v \cdot \sum_{i=0}^{u-v} a_{iu} \left(z_1^{-i} z_2^{-u} + z_1^{-u} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-(N-u)} + z_1^{-(N-u)} z_2^{-i} \right) Y_1 \\
&+ \sum_{i=0}^{u-v} a_{ii} \left(z_1^{-i} z_2^{-i} + z_1^{-i} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-i} \right) Y_1 \\
&+ \sum_{i=0}^{u-v-1} \sum_{j=i+1}^{u-v} a_{ij} \left(z_1^{-i} z_2^{-j} + z_1^{-i} z_2^{-(N-j)} + z_1^{-(N-i)} z_2^{-j} + z_1^{-(N-i)} z_2^{-(N-j)} + z_1^{-j} z_2^{-i} \right. \\
&\quad \left. + z_1^{-j} z_2^{-(N-i)} + z_1^{-(N-j)} z_2^{-i} + z_1^{-(N-j)} z_2^{-(N-i)} \right) Y_1 \quad (15b)
\end{aligned}$$

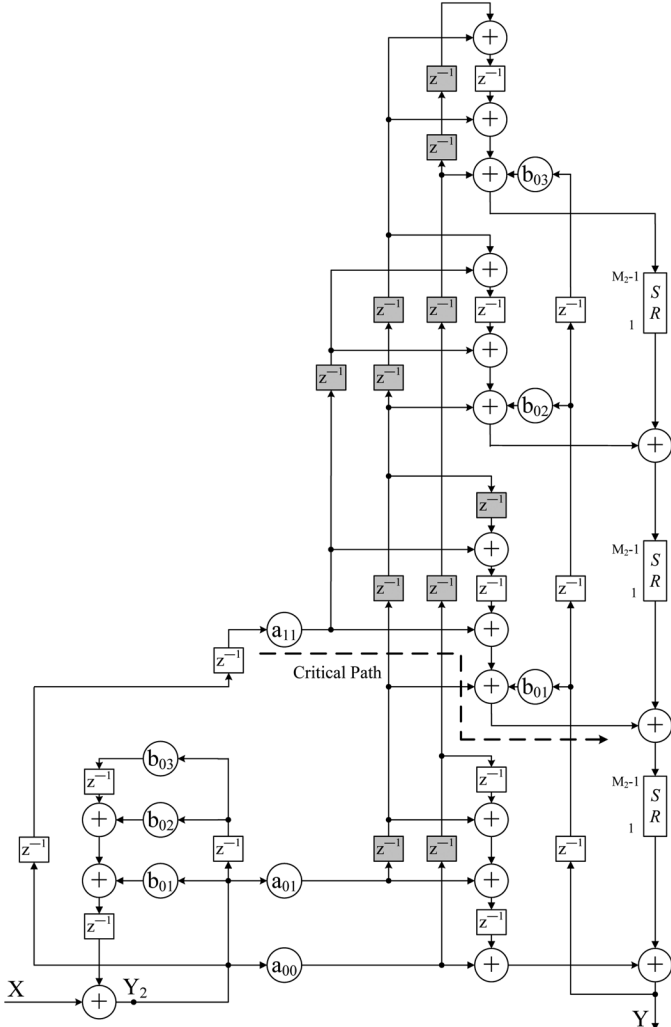


Fig. 10. Proposed Type-2 2-D octagonal symmetry filter structure with separable denominator for $N = 3$.

Step 6: Repeat Step 4 and Step 5 for the rest of the independent numerator coefficients.

Step 7: Remove the resulting unnecessary adders (i.e., the adder with single input or no input source) and the resulting unnecessary delay elements (i.e., the delay with no input source or output destination).

Similarly, the above generalized design procedure can be applied to the Type-2 symmetry filter with the modifications to Step 2, Step 3, Step 4, and Step 5 as described below.

Step 2: Determine the independent coefficients and transfer functions of Y_2/X and Y/Y_2 with specific value of N from the symmetry property.

Step 3: Depict the structure of the Type-2 separable denominator 2-D IIR filter with specific value of N (e.g., Fig. 2 with $N = 3$) and replace the corresponding dependent coefficients using the independent coefficient.

Step 4: According to the structure of the Type-2 separable denominator 2-D IIR filter and the transfer function of Y/Y_2 , the delay arrangement equation in terms of the sum of delays associated with one independent numerator coefficient can be obtained.

Step 5: Based on the delay arrangement equation associated with the one independent numerator coefficient, the paths after the independent coefficient multiplier in the Type-2 separable denominator 2-D IIR filter structure are branched and the branched signal paths are added into the path behind the replaced dependent numerator coefficient multipliers. Then, the replaced dependent numerator coefficient multipliers can be removed.

To illustrate, we will use the above procedure to obtain the Type-1 and Type-2 octagonal symmetry filter structures with $N = 3$ in Figs. 9 and 10, respectively. In the first example, the Type-1 octagonal symmetry filter structure with $N = 3$ is illustrated as follows. In Step 1, we select the Type-1 octagonal symmetry filter order to be $N = 3$. In Step 2, according to octagonal symmetry property, we can determine that a_{00} , a_{01} , a_{11} , b_{01} , b_{02} , b_{03} are independent coefficients and the others are dependent coefficients. Thus, the transfer functions of Y_1/X and Y/Y_1 with $N = 3$ can be obtained from (15a) and (15b), respectively. In Step 3, the structure of the Type-1 separable

$$Y_2 = X + \sum_{j=1}^N b_{0j} z_2^{-j} Y_2 \quad (16a)$$

$$\begin{aligned} Y = & \sum_{j=1}^N b_{0j} z_1^{-j} Y + v a_{uu} z_1^{-u} z_2^{-u} Y_2 \\ & + v \cdot \sum_{i=0}^{u-v} a_{iu} \left(z_1^{-i} z_2^{-u} + z_1^{-u} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-(N-u)} + z_1^{-(N-u)} z_2^{-i} \right) Y_2 \\ & + \sum_{i=0}^{u-v} a_{ii} \left(z_1^{-i} z_2^{-i} + z_1^{-i} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-(N-i)} + z_1^{-(N-i)} z_2^{-i} \right) Y_2 \\ & + \sum_{i=0}^{u-v-1} \sum_{j=i+1}^{u-v} a_{ij} \left(z_1^{-i} z_2^{-j} + z_1^{-i} z_2^{-(N-j)} + z_1^{-(N-i)} z_2^{-j} + z_1^{-(N-i)} z_2^{-(N-j)} \right. \\ & \left. + z_1^{-j} z_2^{-i} + z_1^{-j} z_2^{-(N-i)} + z_1^{-(N-j)} z_2^{-i} + z_1^{-(N-j)} z_2^{-(N-i)} \right) Y_2 \end{aligned} \quad (16b)$$

denominator 2-D IIR filter with order $N = 3$ can be easily obtained in Fig. 1. Then, the dependent coefficients are replaced by the corresponding independent coefficients. In Step 4, for the case of the a_{01} independent numerator coefficient, since $a_{01} = a_{02} = a_{10} = a_{13} = a_{20} = a_{23} = a_{31} = a_{32}$, the sum of delay terms associated with a_{01} in (15b) with $N = 3$ can be expressed in (17a)

$$S_{1,a_{01}} = a_{01} \left(z_2^{-1} + z_2^{-2} + z_1^{-1} + z_1^{-1} z_2^{-3} + z_1^{-2} + z_1^{-2} z_2^{-3} + z_1^{-3} z_2^{-1} + z_1^{-3} z_2^{-2} \right) Y_1 \quad (17a)$$

where $S_{1,a_{01}}$ denotes the sum of delay terms associated with a_{01} in the Type-1 octagonal symmetry filter. According to the structure of the Type-1 separable denominator 2-D IIR filter in Fig. 1, eight delay terms in the square brackets in (17b) denote the delays of the unchanged signal paths in the Type-1 octagonal symmetry filter. That means these eight delay terms in the square brackets are fixed for delay arrangement

$$S_{1,a_{01}} = a_{01} \left([z_2^{-1}] + z_2^{-1} [z_2^{-1}] + z_2^{-1} [z_1^{-1} z_2^1] + z_2^{-2} [z_1^{-1} z_2^{-1}] + z_2^{-2} [z_1^{-2} z_2^2] + z_2^{-3} [z_1^{-2}] + z_2^{-3} [z_1^{-3} z_2^2] + z_2^{-4} [z_1^{-3} z_2^2] \right) Y_1 \quad (17b)$$

The other delays before the square brackets in (17b), however, are adjustable for delay arrangement. After extracting the shared delay elements, (17b) can be recast in (17c) (shown at the bottom of the page). Here, (17c) is referred to as the delay arrangement equation for the a_{01} independent coefficient. In Step 5, according to (17c), seven cut signal paths ahead of the replaced dependent coefficient multipliers $\{a_{02}, a_{10}, a_{13}, a_{20}, a_{23}, a_{31}, a_{32}\}$ are rearranged and summed into the path before the a_{01} independent coefficient multiplier. The replaced dependent coefficient multipliers are then removed. In (17c), the signal paths are added ahead of the a_{01} independent coefficient multiplier and the delay elements before each parenthesis are shown as rightmost-column gray delay elements in Fig. 9. In Step 6, for the rest of the independent numerator coefficients a_{00} and a_{11} , repeat Step 4 and Step 5, the delay arrangement equations and gray delay elements can be obtained. Finally, the resulting unnecessary adders and delay elements are removed to obtain the 2-D octagonal symmetry filter structure in Fig. 9. Note that, in other independent

numerator coefficient cases, if no delay element can be shared in (17b), (17c) will be the same as (17b).

In the second example, the Type-2 octagonal symmetry filter structure with $N = 3$ is illustrated as follows. In Step 1, we select the Type-2 octagonal symmetry filter order to be $N = 3$. In Step 2, due to the same symmetry property as that in the previous example, we can determine that $a_{00}, a_{01}, a_{11}, b_{01}, b_{02}, b_{03}$ are independent coefficients and the others are dependent coefficients. Thus, the transfer functions of Y_2/X and Y/Y_2 with $N = 3$ can be obtained from (16a) and (16b), respectively. In Step 3, the structure of the Type-2 separable denominator 2-D IIR filter with order $N = 3$ can be easily obtained in Fig. 2. Then, the dependent coefficients are replaced by the corresponding independent coefficients. In Step 4, the sum of the delay terms associated with a_{01} can be expressed in (18a)

$$S_{2,a_{01}} = a_{01} (z_2^{-1} + z_2^{-2} + z_1^{-1} + z_1^{-1} z_2^{-3} + z_1^{-2} + z_1^{-2} z_2^{-3} + z_1^{-3} z_2^{-1} + z_1^{-3} z_2^{-2}) Y_2 \quad (18a)$$

where $S_{2,a_{01}}$ denotes the sum of delay terms associated with a_{01} in the Type-2 octagonal symmetry filter. According to the structure of the Type-2 separable denominator 2-D IIR filter in Fig. 2, eight delay terms in the square brackets in (18b) denote the delays of the unchanged signal paths in the Type-2 octagonal symmetry filter. That means these eight delay terms in the square brackets are fixed for delay arrangement

$$S_{2,a_{01}} = a_{01} \left([z_2^{-1}] + z_2^{-1} [z_2^{-1}] + z_2^{-1} [z_1^{-1} z_2^1] + z_2^{-3} [z_1^{-1}] + z_2^{-2} [z_1^{-2} z_2^2] + z_2^{-4} [z_1^{-2} z_2^1] + z_2^{-4} [z_1^{-3} z_2^3] + z_2^{-4} [z_1^{-3} z_2^2] \right) Y_2. \quad (18b)$$

The other delays before the square brackets in (18b), however, are adjustable for delay arrangement. After extracting the shared delay elements, (18b) can be recast in (18c) (shown at the bottom of the next page). Here, (18c) is referred to as the delay arrangement equation for the a_{01} independent coefficient. In Step 5, according to (18c), the signal paths are dispatched after the a_{01} independent coefficient multiplier and the delay elements before each parenthesis are shown as gray delay elements associated with a_{01} in Fig. 10. In the same manner, the delay arrangement equations and gray delay elements corresponding to independent numerator coefficients a_{00} and a_{11} can be obtained in Step 6. Finally, the resulting unnecessary adders and delay elements are removed to obtain the 2-D octagonal symmetry filter structure in Fig. 10.

$$S_{1,a_{01}} = a_{01} \left([z_2^{-1}] + z_2^{-1} \left([z_2^{-1}] + [z_1^{-1} z_2^1] + z_2^{-1} \left([z_1^{-1} z_2^{-1}] + [z_1^{-2} z_2^2] + z_2^{-1} ([z_1^{-2}] + [z_1^{-3} z_2^2] + z_2^{-1} ([z_1^{-3} z_2^2])) \right) \right) \right) Y_1 \quad (17c)$$

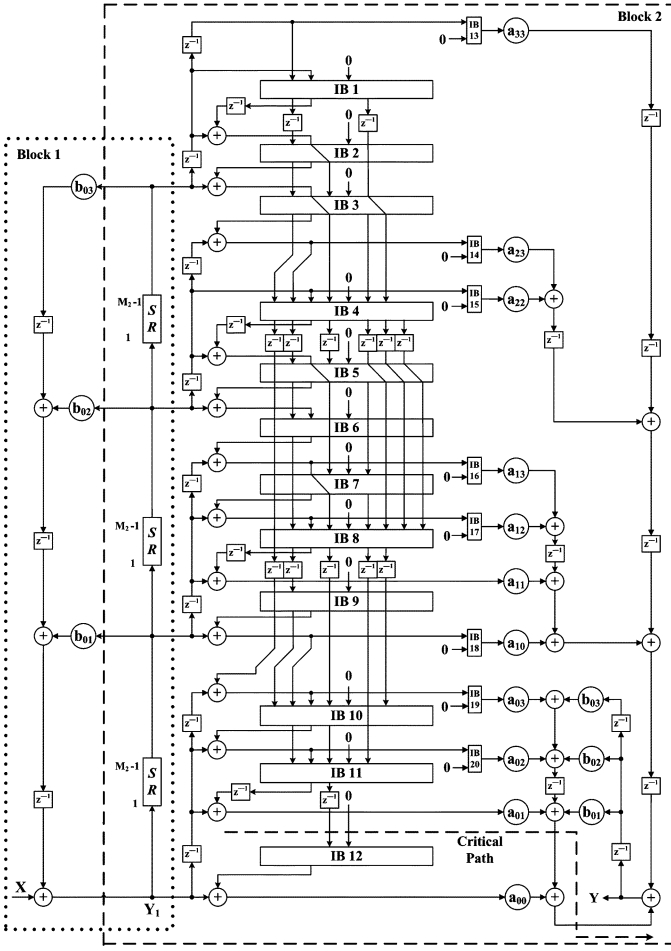


Fig. 11. Proposed multimode 2-D filter architecture with four symmetries for $N = 3$.

In Figs. 9 and 10, it can be observed that although the numbers of delays of the same independent numerator coefficient for the Type-1 and Type-2 octagonal symmetry filters are the same, the gray delay element arrangement of the Type-2 octagonal symmetry filter in Fig. 10 is more complicated than that of the Type-1 octagonal symmetry filter in Fig. 9 for $N = 3$. In the same way, the other six symmetry filters can be analyzed. It can be observed that the gray delay element arrangements of the Type-2 fourfold rotational and quadrantal symmetry filters are complicated compared with that of the Type-1 fourfold rotational and quadrantal symmetry filters for $N = 3$. The similar approach can be followed for any order N for all the symmetries.

$$\begin{aligned}
 & \begin{bmatrix} a_{00} & a_{01} & a_{02} & a_{03} \\ a_{10} & a_{11} & a_{12} & a_{13} \\ a_{20} & a_{21} & a_{22} & a_{23} \\ a_{30} & a_{31} & a_{32} & a_{33} \end{bmatrix} \quad \begin{bmatrix} a_{00} & a_{01} & a_{02} & a_{03} \\ a_{01} & a_{11} & a_{12} & a_{13} \\ a_{02} & a_{12} & a_{22} & a_{23} \\ a_{03} & a_{13} & a_{23} & a_{33} \end{bmatrix} \quad \begin{bmatrix} a_{00} & a_{01} & a_{02} & a_{00} \\ a_{02} & a_{11} & a_{11} & a_{01} \\ a_{01} & a_{11} & a_{11} & a_{02} \\ a_{00} & a_{02} & a_{01} & a_{00} \end{bmatrix} \\
 & \text{(a)} \qquad \qquad \qquad \text{(b)} \qquad \qquad \qquad \text{(c)} \\
 & \begin{bmatrix} a_{00} & a_{01} & a_{02} & a_{03} \\ a_{10} & a_{11} & a_{12} & a_{13} \\ a_{10} & a_{11} & a_{12} & a_{13} \\ a_{00} & a_{01} & a_{02} & a_{03} \end{bmatrix} \quad \begin{bmatrix} a_{00} & a_{01} & a_{01} & a_{00} \\ a_{01} & a_{11} & a_{11} & a_{01} \\ a_{01} & a_{11} & a_{11} & a_{01} \\ a_{00} & a_{01} & a_{01} & a_{00} \end{bmatrix} \\
 & \text{(d)} \qquad \qquad \qquad \text{(e)}
 \end{aligned}$$

Fig. 12. Coefficient distributions of the numerators in matrix form for: (a) general filter; (b) DSM mode; (c) FRSM mode; (d) QSM mode; (e) OSM mode.

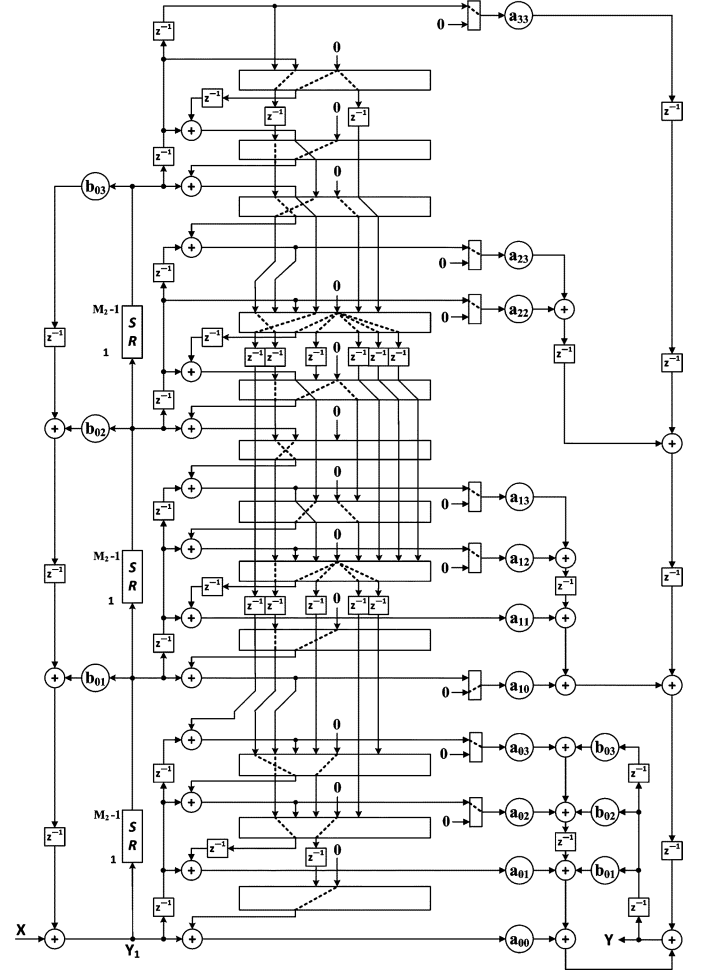
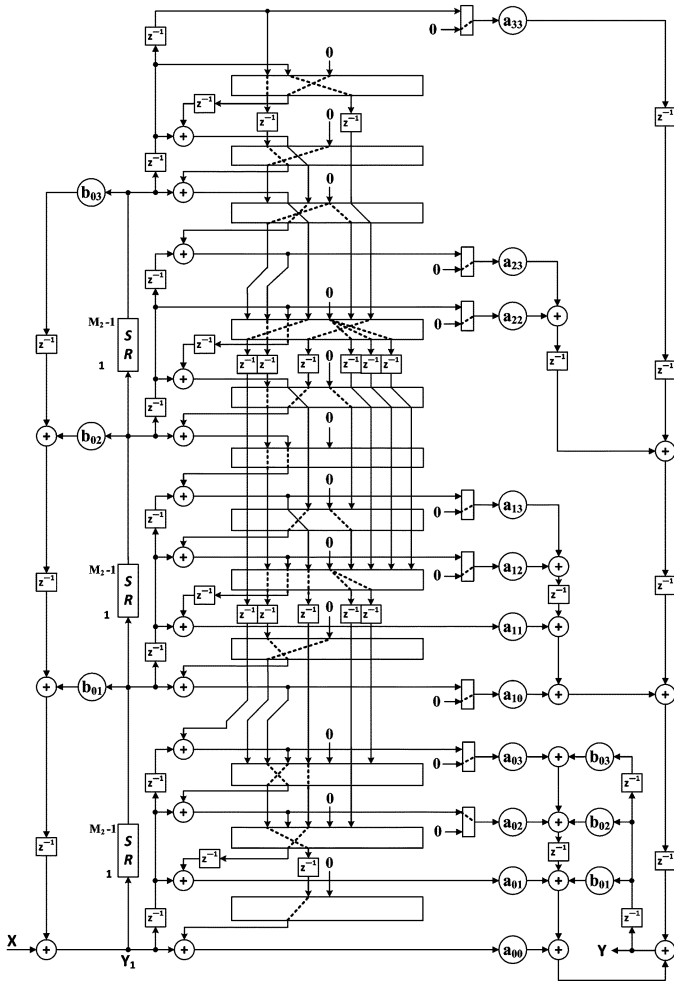
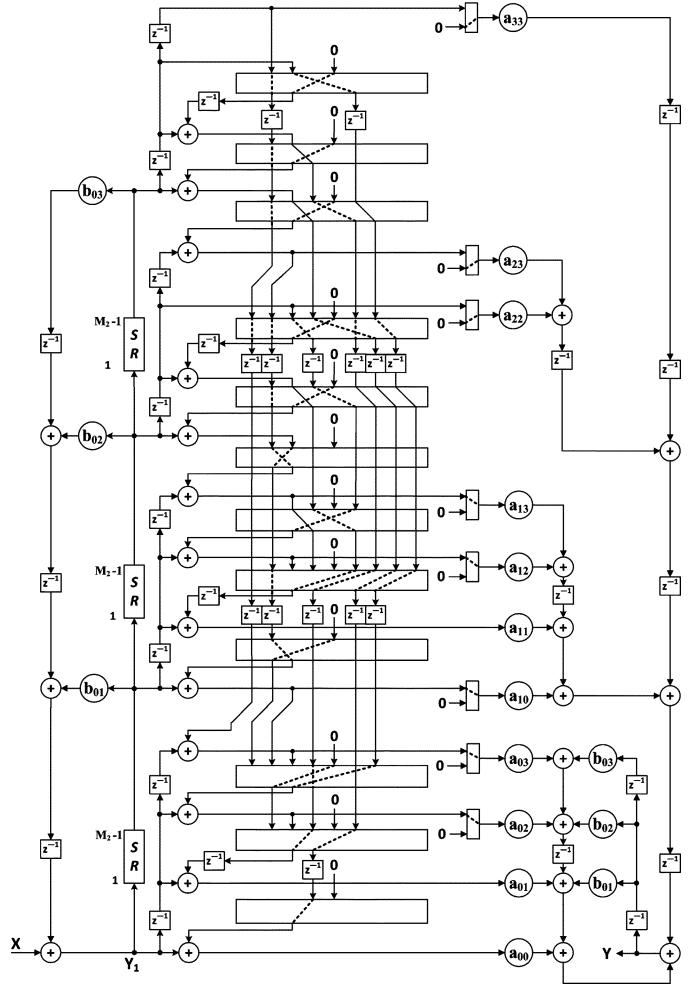


Fig. 13. Diagonal symmetry mode (DSM) operation of the proposed multimode filter for $N = 3$.

$$\begin{aligned}
 S_{2,a_{01}} = & a_{01} \left([z_2^{-1}] + z_2^{-1} \left([z_2^{-1}] + [z_1^{-1}z_2^1] + z_2^{-1} \left(z_2^{-1} ([z_1^{-1}]) + [z_1^{-2}z_2^2] \right. \right. \right. \\
 & \left. \left. \left. + z_2^{-2} ([z_1^{-2}z_2^1] + [z_1^{-3}z_2^3] + [z_1^{-3}z_2^2]) \right) \right) \right) Y_2 \quad (18c)
 \end{aligned}$$


 Fig. 14. Fourfold rotational symmetry mode (FRSM) operation of the proposed multimode filter for $N = 3$.

 Fig. 15. Quadrantal symmetry mode (QSM) operation of the proposed multimode filter for $N = 3$.

IV. COST-EFFECTIVE MULTIMODE 2-D FILTER ARCHITECTURE WITH FOUR SYMMETRIES

In order to support multiple symmetry functions, we propose one cost-effective multimode 2-D filter design with four symmetry modes: diagonal symmetry mode (DSM), fourfold rotational symmetry mode (FRSM), quadrantal symmetry mode (QSM), and octagonal symmetry mode (OSM). The cost-effective multimode 2-D symmetry filter architecture with $N = 3$ shown in Fig. 11 can be obtained based on the following three observations.

First, it is observed that signal paths are added before the a_{ij} independent coefficient multiplier for the Type-1 symmetry filters in Figs. 3, 5, 7, and 9, and signal paths are dispatched after the a_{ij} independent coefficient multiplier for the Type-2 symmetry filters in Figs. 4, 6, 8, and 10. From the delay arrangement analysis in Section III, the Type-2 fourfold rotational, quadrantal, and octagonal symmetry filters have more complicated delay arrangement for $N = 3$. Thus, the four Type-1 symmetry structures are selected for the proposed multimode 2-D filter as the basis for the four configuration modes.

Second, it can be observed in (3) that the Type-1 symmetry filter consists of two transfer functions: Y_1/X and Y/Y_1 , with the Y_1/X transfer function being the same for the four individual symmetry filters as shown in (9a), (11a), (13a), and (15a). The block diagram of Y_1/X is depicted as Block 1 on the left

hand side of Fig. 11. Block 1 requires 3 multipliers and 3 adders. Next, we consider the Y/Y_1 transfer function which is different for each of the four individual symmetry filters. To construct Block 2 of the multimode filter, we need 3 multipliers for the denominator $\{b_{01}, b_{02}, b_{03}\}$, and 11 multipliers for the numerator. To illustrate the requirements on the numerator multipliers, we use the matrix format to show the numerator coefficient distribution. The numerator coefficient distribution of the general filter is shown in Fig. 12(a). The four numerator coefficient distributions for the DSM, FRSM, QSM, and OSM modes are expressed in Fig. 12(b)–(e), respectively. It can be seen that due to symmetry, not all the coefficients are independent. The DSM and FRSM modes require 10 and 4 independent coefficient multipliers for their numerators respectively, while the QSM and OSM modes require 8 and 3 coefficient multipliers for their numerators. Thus, the union set of the independent coefficients is $\{a_{00}, a_{01}, a_{02}, a_{03}, a_{10}, a_{11}, a_{12}, a_{13}, a_{22}, a_{23}, a_{33}\}$. Therefore, $11 + 3 = 14$ coefficient multipliers are required in Block 2 of Fig. 11 to achieve the operations for four different transfer functions of Y/Y_1 . We next consider the number of adders. From the architecture viewpoint, for Y/Y_1 of the multimode 2-D symmetry filter, 13 adders and 11 adders are needed on the left hand side and right hand side of Block 2 in Fig. 11, respectively. The former number can be determined by the Type-1 octagonal symmetry filter structure in Fig. 9. The latter number can be determined by the Type-1 diagonal and quadrantal symmetry filters

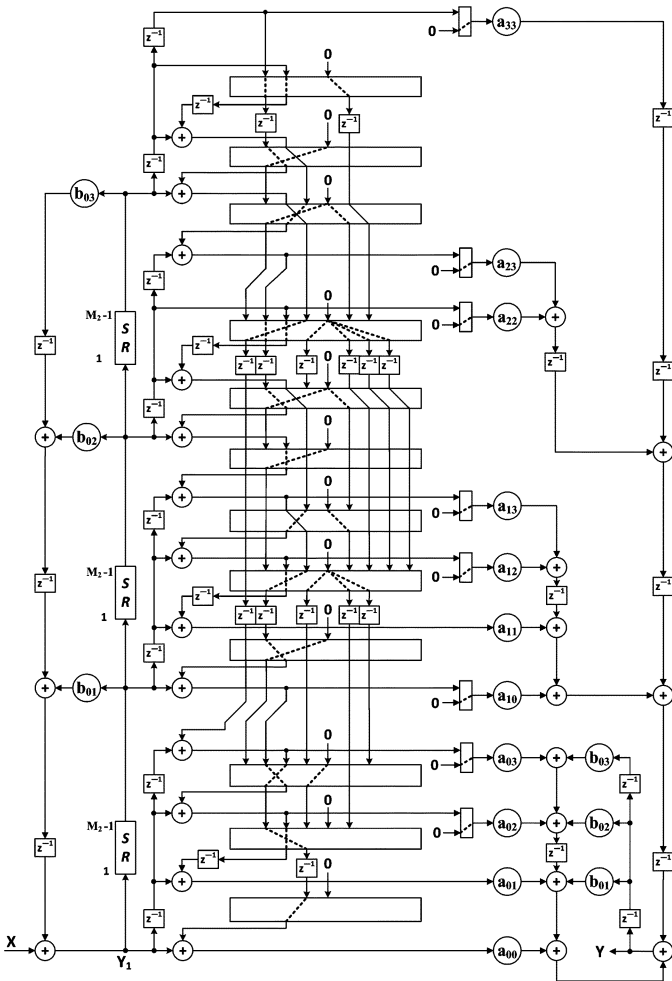


Fig. 16. Octagonal symmetry mode (OSM) operation of the proposed multimode filter for $N = 3$.

in Figs. 3 and 7, respectively. In summary, the proposed multimode 2-D symmetry filter requires altogether 17 coefficient multipliers and 27 adders as shown in Fig. 11.

Third, in Figs. 3, 5, 7, and 9, the interconnection control is only needed for the four Y/Y_1 transfer functions. The multiplication connections and internal connections are controlled by interconnection boxes (IBs) to accomplish the four-mode operations, where IB performs either connection or disconnection task for each signal path. According to the connections of the four individual symmetry filter structures, 12 IBs are needed for the internal connections in Block 2. Note that the solid line feeding through the IB means that this signal path is not controlled by four modes. On the other hand, for the multiplication connection control, only 8 IBs are needed for $N = 3$.

As a consequence, considering the three observations mentioned above, the multimode 2-D filter with four symmetry modes can be obtained in Fig. 11. The multimode filter architecture has a critical path of $T_m + 3T_a$ as shown in Fig. 11 by using the tree method. The corresponding signal path connections of DSM, FRSM, QSM, and OSM are presented in Figs. 13–16, respectively, where the dash lines denote the different connections within each IB for each mode. The difference in the interconnections for the four modes of the proposed multimode filter is highlighted in Fig. 17. Since we only use one hardware resource with a slight area overhead to support four different symmetry modes, the proposed structure achieves an area reduction of 63.25% compared with the sum

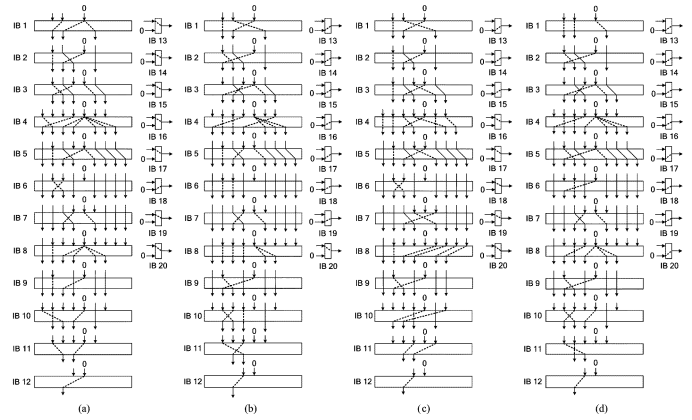


Fig. 17. Interconnections of: (a) DSM; (b) FRSM; (c) QSM; (d) OSM for $N = 3$.

of the areas of the four individual symmetry filter structures. Hence, the proposed structure is cost effective.

V. COMPARISON AND EVALUATION RESULTS

The architecture analysis results are shown in Table I in terms of the number of multipliers and critical path for $N = 3$. This work proposes eight novel individual 2-D symmetry filters and one multimode 2-D symmetry filter. The Type-1 symmetry filters possess simple delay arrangement and the Type-2 symmetry filters have shorter critical path. Among these filters, the proposed Type-1 and Type-2 octagonal symmetry filters have the lowest number of multipliers.

Most importantly, the power and core area evaluation results among the proposed four Type-1 2-D individual symmetry filter architectures, one multimode 2-D symmetry filter architecture, one Type-1 2-D separable denominator filter architecture, and other referenced filter architectures are presented in Table II. Here, all evaluated filter architectures with $N = 3$ and $M_2 = 8$ have been implemented in TSMC 0.18 μm general-purpose one-poly six-metal (1P6M) CMOS process with 1.8-V Artisan standard cell library. The wordlengths of the filter input, filter output, coefficients, and register outputs are 10, 10, 16, and 16 bits, respectively. The 16×16 -bit multiplier is adopted for the proposed 2-D symmetry filters, multimode filter, and separable denominator filter.

For the 2-D conventional filter [12], the 10×16 -bit and 16×16 -bit multipliers are used for the coefficient multiplications of a_{ij} and b_{ij} , respectively. Although the conventional filter has the largest number of multipliers, it is expected that the power and area of the filter can be reduced due to the use of 10×16 -bit multiplier. In order to save the number of coefficient inputs for the filter implementation, the coefficients are loaded sequentially through one 16-bit coefficient input and stored in the individual registers. After the coefficients of register are loaded into the corresponding multipliers in parallel, the filter begins to work. In this manner, the requirement of the number of pads can be significantly reduced.

The cell-based design flow is adopted for the chip implementation and addressed as follows. Synopsys Design Compiler is employed to synthesize the proposed and referenced 2-D filter designs in RTL level and Cadence SOC Encounter is adopted for placement and routing (P&R). The power dissipation is measured via Synopsys PrimePower using 100 000 combinations of random vectors after RC extraction of the placed and routed netlists at 100 MHz. The 100 000 combinations is composed of 100-set stable coefficients by 1000 random inputs per each

TABLE I
COMPARISON RESULTS AMONG THE 2-D IIR DIGITAL FILTER ARCHITECTURES

2-D Filter Architecture		No. of Multipliers	Critical Path for N=3
Ahmed [10]		$2(N+1)^2 - 1$	$T_m + (2 + \lceil \log_2(N+1) \rceil)T_a$
Van [12]		$2(N+1)^2 - 1$	$T_m + 3T_a$
Separable denominator filter [13]	Type-1	$(N+1)^2 + 2N$	$T_m + 3T_a$
	Type-2	$(N+1)^2 + 2N$	$T_m + 2T_a$
Non-separable denominator filter [14, 15]	Diagonal symmetry	$(N+1)^2 + N$	$T_m + 2T_a$
	Four-fold rotational symmetry	$\frac{3}{4}(N+1)^2 + \frac{1}{2}(N+1) - 1$	$T_m + 3T_a$
Proposed diagonal symmetry filter	Type-1	$\frac{1}{2}(N+1)^2 + \frac{5}{2}N + \frac{1}{2}$	$T_m + 3T_a$
	Type-2 [13]	$\frac{1}{2}(N+1)^2 + \frac{5}{2}N + \frac{1}{2}$	$T_m + 2T_a$
Proposed four-fold rotational symmetry filter	Type-1	$\frac{1}{4}(N+1)^2 + \frac{3}{4}v + 2N$	$T_m + 3T_a$
	Type-2	$\frac{1}{4}(N+1)^2 + \frac{3}{4}v + 2N$	$T_m + 2T_a$
Proposed quadrantal symmetry filter	Type-1	$\frac{1}{2}(N+1)^2 + \frac{v}{2}(N+1) + 2N$	$T_m + 3T_a$
	Type-2	$\frac{1}{2}(N+1)^2 + \frac{v}{2}(N+1) + 2N$	$T_m + 2T_a$
Proposed octagonal symmetry filter	Type-1	$\frac{1}{8}(N+1+v)^2 + \frac{1}{4}(N+1+v) + 2N$	$T_m + 3T_a$
	Type-2	$\frac{1}{8}(N+1+v)^2 + \frac{1}{4}(N+1+v) + 2N$	$T_m + 2T_a$
Proposed multimode symmetry filter	Type-1	$\frac{1}{2}(N+1)^2 + \frac{1}{2}(N+1) + \frac{1}{8}(N+1+v)^2 - \frac{1}{4}(N+1+v) + 2N$	$T_m + 3T_a$

TABLE II
EVALUATION RESULTS OF 2-D IIR DIGITAL FILTER ARCHITECTURES

2-D Filter Architecture		Power Consumption		Core Area	
Conventional filter [12]		38.51 mW	100%	608,703 μm^2	100%
Proposed Type-1 separable denominator filter [13]		34.62 mW	89.90%	528,099 μm^2	86.76%
Proposed Type-1 diagonal symmetry filter		32.05 mW	83.23%	418,608 μm^2	68.77%
Proposed Type-1 four-fold rotational symmetry filter		24.53 mW	63.70%	291,381 μm^2	47.87%
Proposed Type-1 quadrantal symmetry filter		29.69 mW	77.10%	393,384 μm^2	64.63%
Proposed Type-1 octagonal symmetry filter		23.98 mW	62.27%	287,592 μm^2	47.25%
Proposed multimode symmetry filter architecture	DSM	34.27 mW	88.99%	511,209 μm^2	83.98%
	FRSM	26.41 mW	68.58%		
	QSM	31.76 mW	82.47%		
	OSM	24.93 mW	64.74%		
	Average	29.34 mW	76.19%		

set stable coefficient. From Table II, it can be seen that the presented four individual symmetry filter structures are capable of providing low power and low area consumption.

In terms of power consumption, the diagonal, fourfold rotational, quadrantal, and octagonal symmetry filter structures can attain power savings of 16.77%, 36.30%, 22.90%, and 37.73% with respect to that of the conventional filter architecture [12], and power savings of 7.42%, 29.15%, 14.24%, and 30.73% with respect to that of the Type-1 separable denominator filter architecture [13]. On the other hand, the layout of the proposed multimode 2-D filter for $N = 3$ in Fig. 11 is shown in Fig. 18 with the area size of $718.95 \mu\text{m} \times 711.05 \mu\text{m}$. The corresponding power consumption of the proposed multimode 2-D filter is 29.34 mW on average. In terms of power comparison, the DSM, FRSM,

QSM, and OSM modes can attain power reductions of 11.01%, 31.42%, 17.53%, and 35.26% with respect to that of the conventional filter architecture [12], and power reductions of 1.01%, 23.71%, 8.26%, and 27.99% with respect to that of the Type-1 separable denominator filter architecture [13]. Compared with the four individual symmetry filter designs, the corresponding modes of the multimode architecture increase the power consumption by 6.93%, 7.66%, 6.97%, and 3.96%, respectively. Although each individual symmetry filter structure has smaller area and lower power consumption than the proposed multimode filter architecture does, these four individual symmetry filter structures are single-mode such that each of them cannot be applied to the demand of a multiple-symmetry system. So the multimode filter architecture can save more chip area when the

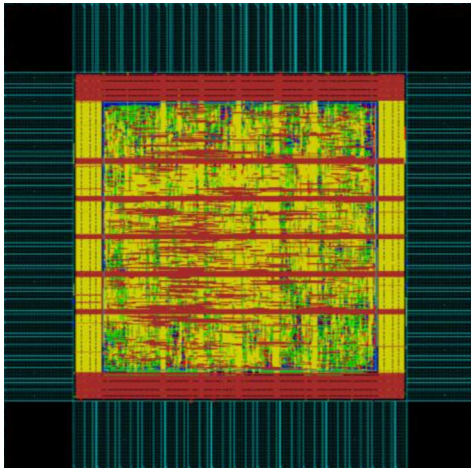


Fig. 18. Layout of the proposed multimode symmetry filter for $N = 3$.

four individual symmetry filter structures are needed in a multiple-symmetry system. Compared with the sum of the areas of the four individual symmetry filters, the area saving could be up to 63.25%. Hence, the proposed multimode filter architecture is power efficient and cost effective.

VI. CONCLUSION

In this paper, eight new power-efficient and cost-effective individual 2-D symmetry filter structures and one multimode filter with diagonal, fourfold rotational, quadrantal and octagonal symmetry modes are presented for a 2-D filter transfer function of order 3×3 . By using the developed generalized design procedure, the individual symmetry filter structure for different order could be obtained. Further, it is to be noted that the symmetry conditions imposed are the sufficient conditions for the existence of those symmetries in a given transfer function. The novel aspect of the work is taking into account the presence of symmetry in the 2-D VLSI filter implementation and thereby reducing the power and the cost of the design. From the implementation results, the proposed four symmetry structures can attain power savings of 16.77%, 36.30%, 22.90%, and 37.73% with respect to that of the conventional filter architecture [12], and the power savings of 7.42%, 29.15%, 14.24%, and 30.73% with respect to that of the Type-1 separable denominator filter architecture [13]. On the other hand, the proposed multimode filter architecture can attain the power reduction on average by 15.25% with respect to that of the Type-1 separable denominator filter architecture. It will be of interest to study and compare various 2-D digital filter structures possessing different magnitude symmetries. In [17], the work on the generalized formulation of 2-D filter structures with symmetry is initiated.

REFERENCES

- [1] M. Petrou and P. Bosdogianni, *Image Processing*. New York: Wiley, 2000.
- [2] A. M. Tekalp, *Digital Video Processing*. Englewood Cliffs, NJ: Prentice-Hall, 1995, ch. 14.
- [3] M. A. Sid-Ahmed, *Image Processing: Theory, Algorithms, and Architectures*. New York: McGraw-Hill, 1995.
- [4] D. E. Dudgeon and R. M. Mersereau, *Multidimensional Digital Signal Processing*. Englewood Cliffs, NJ: Prentice-Hall, 1984.
- [5] M. N. S. Swamy and P. K. Rajan, "Symmetry in 2-D filters and its application," in *Multidimensional Systems: Techniques and Applications*, S. Tzafestas, Ed. New York: Marcel Dekkar, 1986, ch. 9.

- [6] H. C. Reddy, I. H. Khoo, and P. K. Rajan, "Application of symmetry: 2-D polynomials, fourier transform, and filter design," in *The Circuits and Filters Handbook*, W. K. Chen, Ed., 3rd ed. Boca Raton, FL: CRC, 2009.
- [7] H. C. Reddy, I. H. Khoo, and P. K. Rajan, "2-D symmetry: Theory and filter design applications," *IEEE Circuits Syst. Mag.*, vol. 3, no. 3, pp. 4–33, 3rd Q., 2003.
- [8] H. L. P. A. Madanayake and L. T. Bruton, "A speed-optimized systolic array processor architecture for spatio-temporal 2-D IIR broadband beam filter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 7, pp. 1953–1966, Aug. 2008.
- [9] H. L. P. A. Madanayake, S. V. Hum, and L. T. Bruton, "A systolic array 2-D IIR broadband RF beamformer," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 55, no. 12, pp. 1244–1248, Dec. 2008.
- [10] M. A. Sid-Ahmed, "A systolic realization for 2-D digital filters," *IEEE Trans. Acoust., Speech, Signal Process.*, vol. 37, no. 4, pp. 560–565, Apr. 1989.
- [11] N. R. Shanbhag, "An improved systolic architecture for 2-D digital filters," *IEEE Trans. Signal Process.*, vol. 39, no. 5, pp. 1195–1202, May 1991.
- [12] L. D. Van, "A new 2-D systolic digital filter architecture without global broadcast," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 4, pp. 477–486, Aug. 2002.
- [13] I. H. Khoo, H. C. Reddy, L. D. Van, and C. T. Lin, "2-D digital filter architectures without global broadcast and some symmetry applications," in *Proc. IEEE ISCAS*, May 2009, pp. 952–955.
- [14] P. Y. Chen, L. D. Van, H. C. Reddy, and C. T. Lin, "A new VLSI 2-D diagonal-symmetry filter architecture design," in *Proc. IEEE APCCAS*, Macao, China, Nov. 2008, pp. 320–323.
- [15] P. Y. Chen, L. D. Van, H. C. Reddy, and C. T. Lin, "A new VLSI 2-D fourfold-rotational-symmetry filter architecture design," in *Proc. IEEE ISCAS*, May 2009, pp. 93–96.
- [16] P. P. Vaidyanathan, *Multirate Systems and Filter Banks*. Englewood Cliffs, NJ: Prentice-Hall, 1993, pp. 859–863.
- [17] I. H. Khoo, H. C. Reddy, L. D. Van, and C. T. Lin, "Generalized formulation of 2-D filter structures without global broadcast for VLSI implementation," presented at the IEEE MWSCAS, Seattle, WA, Aug. 2010.



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