A 38/114 GHz Switched-Mode and Synchronous Lock Standing Wave Oscillator

Tai-You Lu and Wei-Zen Chen

***Abstract*—This letter presents a 38/114 GHz switched-mode standing wave oscillator (SWO) capable of synchronous locking. Triple output frequency can be excited by digital control of different mode operations. The experimental prototype was fabricated using a low leakage 65 nm 1P9M triple-well CMOS technology. Incorporating a synchronous lock scheme, the measured phase noise from a 38 GHz carrier before and after the phase locked at 1 MHz offset are −102 dBc/Hz and −120 dBc/Hz, respectively. For the mode 1 operation at 38 GHz and mode 3 operation at 114 GHz, the experimental prototype consumes 4 and 20 mA, respectively, under a 1.2 V biasing voltage and with a chip size of $720 \times 880\ \mu\mathrm{m}^2$.**

***Index Terms*—Standing wave oscillator (SWO), synchronous lock.**

I. Introduction

MILLIMETER wave applications in sensing, advanced imaging, and bio-agent chemical detection have been the focus of considerable research in the past few years. However, to achieve widespread usage, a compact and cost-effective signal source is necessary. Recently, CMOS oscillators in nanometer technology have demonstrated a strong potential for application in the sub-Tera Hz frequency range (0.1–1 THz) [1]–[3]. These designs are based on LC-tank architecture and they attempt to multiply their output frequency through the application of multiphase edge combining [2] or push-push techniques [3]. As the operating frequency increases to hundreds in the GHz range, matching, crosscoupling, and insertion loss of transmission lines between the oscillators and edge combiner become very critical to the realization of a successful design. In addition, the edge combiner itself may become an obstacle to the achievement of the desired frequency range. From the perspective of power efficiency, an edge combiner seeks to eliminate lower order harmonics through vector cancellation. However, it turns out to consume a considerable amount of dc power wastefully since its output signal becomes quite small as the multiplication factor increases.

In contrast to LC-tank oscillators, wave-based oscillators are capable of pushing their output frequency close to the cutoff frequency of a device $(\mathrm{f_T})$ by distributing parasitic capacitance along the transmission line [4]–[8]. The output frequency can be varied by switching the capacitor and varactor tuning [6]. Under the ultimate frequency limitation, the oscillation speed is primarily determined by the characteristics of the transmission line. A conventional standing wave or traveling wave oscillator or distributed oscillator is operated at its fundamental mode [5]–[8], and it is difficult to generate double or triple output frequency in a single oscillator, unlike its multi-band LC oscillator based counterparts [9]. In order to facilitate multi-band operations, this letter proposes a switched-mode standing wave oscillator capable of generating fundamental and triple output frequencies in the sub-THz range. Different excitation modes are enabled using digital control without the need to resort to other high speed circuits or to an edge combiner. Additionally, through the incorporation of mode enabling and sub-harmonic injection locking techniques, the proposed SWO can be synchronized to an external reference source in order to further improve phase noise performance. The close-in phase noise is improved by about 18 dB with the proposed scheme when the SWO incorporates a synchronous lock.

II. Architecture and Implementation

Fig. 1 shows the architecture of the proposed standing wave oscillator. As an experimental prototype, it is composed of circular differential transmission lines (TL) and three negative impedance converters equally-spaced along the TL to compensate for power loss and to sustain oscillation. Under the boundary conditions of ac ground at both ends of the TL, odd mode excitations are preserved and the resonant frequency can be derived as follows:

$$\omega_{osc} = \frac{\omega_{phase\_velocity}}{\lambda} = \frac{1/\sqrt{LC}}{2l/(2n+1)} = \frac{2n+1}{2l\sqrt{LC}}\ n = 0, 1, 2, \ldots$$

where L and C represent the equivalent inductance and capacitance per unit length of the TL, respectively; l denotes the TL length; λ is the wavelength under resonant frequency; and n stands for the different excitation modes. While on the one hand, it confirms that the resonant frequency of a given TL can be increased by n-fold if a higher order mode is excited; on the other, it also establishes the fact that the output frequency can be fine-tuned by adjusting its wave velocity. However, in a typical SWO, a large portion of oscillation energy is concentrated naturally on its fundamental mode, while other modes co-exist and manifest themselves as high order harmonics. In order to improve its power efficiency when experiencing different mode excitations, the fundamental mode should be suppressed to boost energy at higher order modes by imposing other constraints. As the SWO reaches a steady state, the TL poses zero or maximum power at fixed points, where the locations are varied under different mode operations. It stands to reason that a different operation mode can be excited if the power recovery stations, that is, negative impedance converters, are located right at the nodes where the maximum power is gener-

Manuscript received August 19, 2010; revised September 17, 2010; accepted October 10, 2010. Date of publication December 10, 2010; date of current version January 07, 2011. This work was supported in part by National Nano Device Laboratories (NDL), Ansoft Corporation, TSMC University Shuttle Program, and the National Science Council (NSC), Taiwan by Grant NSC99-2220-E-009-063.

The authors are with the Department of Electronics Engineering and the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan (e-mail: wzchen@alab.ee.nctu.edu.tw).

Digital Object Identifier 10.1109/LMWC.2010.2089975

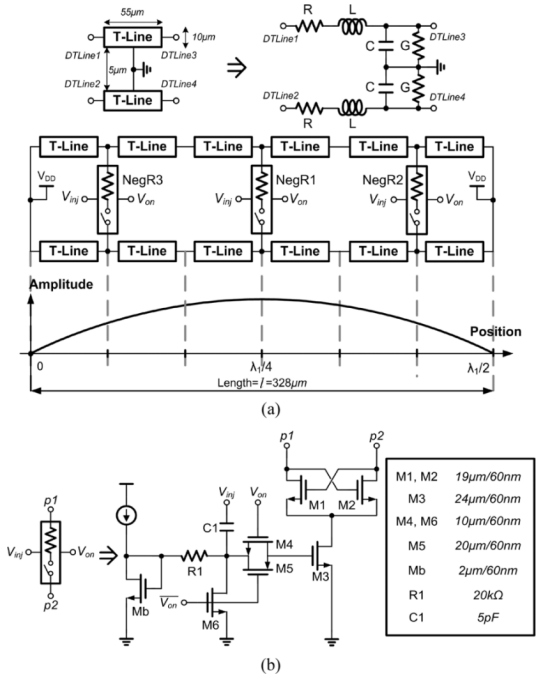

Fig. 1. (a) Proposed switched-mode standing wave oscillator architecture and (b) detailed circuit schematic.

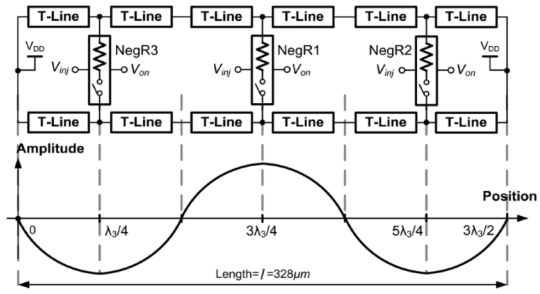

Fig. 2. Standing wave oscillator for mode 3 operation.

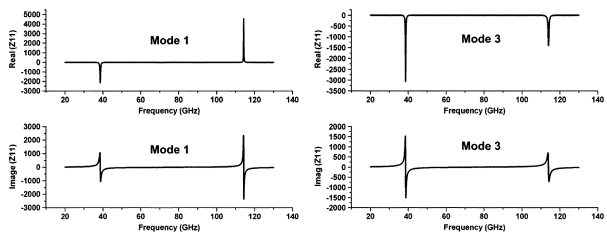

Fig. 3. Simulated Z11 at node $l/2$ with different excited mode.

ated. Fig. 1 shows the architecture of the multi-mode SWO and its position-dependant amplitude necessary for fundamental mode operation. Here only the negative impedance converter NegR1 at $l/2 = \lambda_1/4$ is enabled by setting the digital control signal to $(V_{on}, \overline{V_{on}}) = (1, 0)$, thus the transmission gate (M4, M5) is turned on. Similarly, the negative impedance converters NegR2 and NegR3 at $l/6(\lambda_1/12)$ and $5l/6(5\lambda_1/12)$ are disabled by setting $(V_{on}, \overline{V_{on}}) = (0, 1)$ to turn on M6. Contrarily, for the mode 3 operation in Fig. 2, all the negative impedance converters are activated by setting the digital control signal to $(V_{on}, \overline{V_{on}}) = (1, 0)$. In this scenario, operating points at $l = 1, 3, 5\lambda_3/4$ are also forced to pose the maximum power as well, thus the constraints oblige the SWO to operate at mode 3.

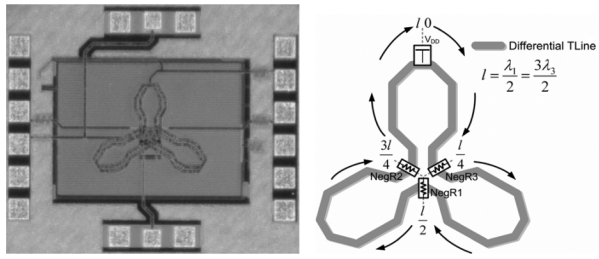

Fig. 4. SWO (a) chip micrograph and (b) physical layout.

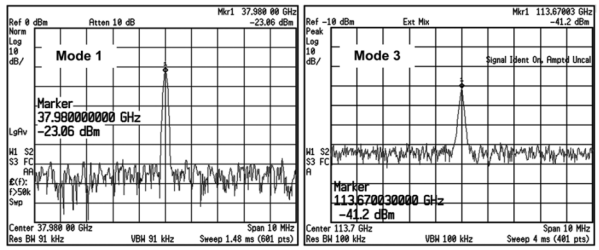

Fig. 5. Measured output spectrum at mode 1 (38 GHz) and mode 3 (114 GHz).

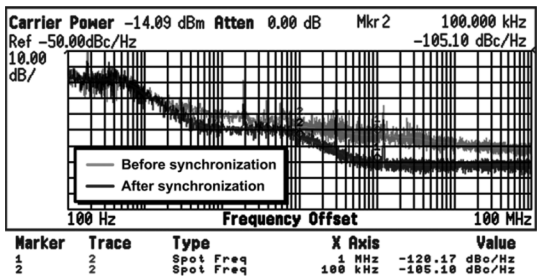

Fig. 6. Measured phase noise before (grey) and after (dark) synchronous lock.

TABLE I
PERFORMANCE BENCHMARK

	This work	[9]	[5]	[8]	[7]	[6]
Tech.	65nm CMOS	90nm CMOS	180nm CMOS	180nm CMOS	120nm SOI	130nm CMOS
Supply	1.2	N/A	1.5	1.8	1.5	1.2
Power dissipation	4.8mW 24mW(1)	14mW	27mW	4.7mW	7.5mW	30mW
Max. freq. (GHz)	38 114(1)	21 55(4)	40	14	44	12
PN@1MHz (dBc/Hz)	-102(2) -120(3)	-101 -87	-100	-110	-101	-105
P_{out} (dBm)	-15(3) -41(1)	N/A	-13.6	-15.3	-6	N/A
FoM	187(2) 205(3)	176 170(4)	178	188	185	172
Topology	standing wave	LC -resonator	standing wave	standing wave	traveling wave	traveling wave
Mode	Mode1 Mode3	Mode1 Mode3	Mode1	Mode1	Mode1	Mode1

(1) Mode 3 operation for $f_{osc} = (2n + 1) \times f_{fundamental}$, where $n = 1$
(2) Mode 1 operation without synchronous lock
(3) Mode 1 operation with synchronous lock
(4) Mode 3 operation (by switched resonator) with $f_{osc} = (n/2 + 1) \times f_{fundamental}$, where $n = 3$

As one way to validate this concept, the equivalent negative impedance looking at the centre of the TL $(l/2)$ under different modes is summarized in Fig. 3. For a mode 1 operation, the impedance (Z_{11}) at 114 GHz is positive while that at 38 GHz is negative, indicating that the SWO tends to concentrate more

power on the fundamental mode. In contrast to mode 1, the negative impedance ratio for its fundamental and 3rd order harmonic becomes the following:

$$\left| \frac{\mathrm{Re}\,[Z_{11}(f_1)]|_{@38\ \mathrm{GHz}}}{\mathrm{Re}\,[Z_{11}(3f_1)]|_{@114\ \mathrm{GHz}}} \right| = 2.3.$$

It reveals that most of the energy being pumped into the SWO is pushed to the triple frequency. In the simulation, the power ratio for the triple to fundamental frequency is about 47 dB in mode 3 operation. Fig. 4 shows the chip photo and layout of the SWO prototype. The differential TL is laid out in three arcs (leaves) of 328 μm in length. Based on the EM simulation, the quality factor of the differential transmission line is approximately 10 and 12 at 38 GHz and 114 GHz, respectively. To maintain the symmetry of the layout and to facilitate an increase in power, all the negative impedance converters are centralized in the middle to eliminate potential transmission line mismatches, while the output signal is picked up at $(l/2)$ to generate the largest output power at any odd-mode. Moreover, dummy buffers are added at the transmission line to compensate for asymmetry when experiencing different mode excitation. The digital control scheme of the SWO can be applied in conjunction with the phase synchronization technique [10]. In this prototype, the sub-harmonics (f_{ref}) of the SWO are injected by applying V_{inj} to enable and disable periodically all the negative impedance converters, as shown in Fig. 1, which lead to a synchronous lock/injection locked SWO. If we let $f_{swo}/f_{ref} = N$, where N is a positive integer, the frequency locking range is proportional to the power ratio between the reference signal and SWO output, and inversely proportional to N. With the incorporation of the phase synchronization technique, the in- band noise can be suppressed significantly.

III. Experimental Results

The experimental prototype was fabricated using a low leakage 65 nm triple-well CMOS technology whose f_T is approximately 150 GHz. The circuit is measured using on-chip probing. Due to the limited bandwidth of the in-house instruments available, the fundamental mode was designed to operate at approximately 38 GHz, and its corresponding mode 3 to operate at 114 GHz. Fig. 5 shows the measured output spectrum at 37.98 GHz (mode 1) and 113.67 GHz (mode 3), respectively. A frequency deviation of 270 MHz in mode 3 was observed due to the parasitic variations during mode switching, which can be overcome by a fine tuning scheme. By taking instrument signal loss into account (including the loss of probes, cables and adapters) the output power at 38 GHz (for mode 1) is about -15 dBm. The measured output power at 114 GHz (for mode 3) is -41.2 dBm, which is underestimated due to insufficient equipment bandwidth. The measured free running phase noise from a 38 GHz carrier is -102 dBc/Hz at 1 MHz offset, and the simulated phase noise at 38 and 114 GHz are approximately -105 dBc/Hz and -94 dBc/Hz at 1 MHz offset, respectively. With the injection of a sub-harmonic reference f_{swo}/N ($N = 1, 2, 3$), whose phase noise at 1 MHz offset are -127 dBc/Hz, -133 dBc/Hz and -135 dBc/Hz, the improvement to the SWO phase noise is approximately 18 dB thanks to the clean reference source. Thus, the opportunity arises to realize an ultra low noise signal source in the sub-THz range. Fig. 6 shows the phase noise profile before (grey) and after (dark) a synchronous lock condition. With a minimum power of -30 dBm (38 GHz), -12 dBm (19 GHz) and -3 dBm (12.7 GHz) sub-harmonic injection, the frequency locking ranges are 1500 MHz, 40 MHz, and 6 MHz, respectively, without a need to resort to other frequency tuning schemes. The locking range can be extended with the aid of varactors or a frequency tracking loop. For mode 1 and mode 3 operations, this chip, which has an area of $720 \times 880\ \mu\mathrm{m}^2$, consumes 4 and 20 mA, respectively, under a 1.2 V power supply.

IV. Conclusion

This letter proposes a novel concept to triple SWO output frequency by exciting different mode operations without the need to reconfigure the transmission line, switched resonator, or other high-speed circuits such as an edge combiner. Furthermore, through the incorporation of mode enabling and sub-harmonic injection locking, the proposed SWO can be synchronized to an external reference to further improve phase noise performance. The measured close-in phase noise is improved significantly using the proposed scheme when the SWO incorporates a synchronous lock. Table I shows the performance benchmark with the prior art using a standing wave [5], [8], traveling wave [6], [7], and LC-tank topologies [9]. Based on the figure of merit (FoM) in terms of noise performance and power consumption

$$FoM = -PN + 20\log\left(\frac{f_o}{\Delta f}\right) - 10\log\left(\frac{P_{diss}}{1\ \mathrm{mW}}\right)$$

the proposed SWO manifests superior phase noise performance and FoM (187 and 205 without and with synchronous lock, respectively) compared to a traveling wave or LC-tank based architectures, and is the only SWO that is capable of switched mode operation.

References

[1] S. Sankaran, C. Mao, E. Seok, D. Shim, C. Cao, R. Han, D. J. Arenas, D. B. Tanner, S. Hill, C.-M. Hung, and K. K. O., "Towards terahertz operation of CMOS," in *ISSCC Tech. Dig.*, Feb. 2009, pp. 202–203, 203a.

[2] D. Huang, T. R. LaRocca, M. C. F. Chang, L. Samoska, A. Fung, R. L. Campbell, and M. Andrews, "Terahertz CMOS frequency generator using linear superposition technique," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2730–2738, Dec. 2008.

[3] E. Seok, C. Cao, D. Shim, D. J. Arenas, D. B. Tanner, C.-M. Hung, and K. K. O., "A 410 GHz CMOS push-push oscillator with an on-chip patch antenna," in *ISSCC Tech. Dig.*, Feb. 2008, pp. 472–629.

[4] W. F. Andress and D. Ham, "Standing wave oscillators utilizing wave-adaptive tapered transmission lines," *IEEE J. Solid-State Circuits*, vol. 40, no. 3, pp. 638–651, Mar. 2005.

[5] J.-C. Chien and L.-H. Lu, "Design of wide-tunning-range millimeter-wave CMOS VCO with a standing-wave architecture," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1942–1952, Sep. 2007.

[6] F. B. Abdeljelil, W. Tatinian, L. Carpineto, and G. Jacquemod, "Desigin of a CMOS 12 GHz rotary travelling wave oscillator with switched capacitor tuning," in *RFIC Tech. Dig.*, Jun. 2009, pp. 579–582.

[7] J. Kim, J.-O. Plouchart, N. Zamdmer, R. Trzcinski, K. Wu, B. J. Gross, and M. Kim, "A 44 GHz differentially tuned VCO with 4 GHz tuning range in 0.12 μm SOI CMOS," in *ISSCC Tech. Dig.*, Feb. 2005, pp. 416–417.

[8] D. Ham and W. F. Andress, "Standing wave oscillators utilizing wave-adaptive tapered transmission lines," in *ISSCC Tech. Dig.*, Feb. 2004, pp. 380–553.

[9] S.-W. Tam, H.-T. Yu, Y. Kim, E. Socher, M. C. F. Chang, and T. Itoh, "A dual band mm-wave CMOS oscillator with left-handed resonator," in *RFIC Tech. Dig.*, Jun. 2009, pp. 477–480.

[10] J. Lee, H. Wang, W.-T. Chen, and Y.-P. Lee, "Subharmonically injection-locked PLLs for ultra-low-noise clock generation," in *ISSCC Tech. Dig.*, Feb. 2009, pp. 92–93, 93a.