A CMOS 8-Bit 1.6-GS/s DAC With Digital Random Return-to-Zero

Wei-Hsin Tseng, Jieh-Tsorng Wu, *Senior Member, IEEE*, and Yung-Cheng Chu

***Abstract*—A digital random return-to-zero technique is presented to improve the dynamic performance of current-steering digital-to-analog converters (DACs). To demonstrate the proposed technique, a CMOS 8-bit 1.6-GS/s DAC was fabricated in a 90-nm CMOS technology. The DAC achieves a spurious-free dynamic range better than 60 dB for a sine-wave input up to 460 MHz and better than 55 dB up to 800 MHz. The DAC consumes 90 mW of power.**

***Index Terms*—Current steering, digital-to-analog converter (DAC), digital random return-to-zero (DRRZ), return-to-zero (RZ).**

I. Introduction

THE current-steering digital-to-analog converters (DACs) can achieve a high sampling rate and, thus, are commonly used in generating high-frequency signals [1]–[5]. Fig. 1 shows a generic current-steering DAC. It consists of M equally weighted current cells. Each current cell contains a current source of I_u output current, a p-channel MOSFET pair functioning as a current switch, and a digital latch controlled by the clock CK. The complementary outputs of the latch control the current switch, directing the I_u current to either the R_L load at V_{o1} or the one at V_{o2}. A decoder converts the DAC digital input $D_i[k]$ into M thermometer-code signals $B_j[k]$, where $1 \leq j \leq M$, such that $D_i[k] = \sum_{j=1}^{M} B_j[k]$. The $B_j[k]$ signal has a binary value of either $+1$ or -1. Fig. 2 illustrates the DAC differential nonreturn-to-zero (NRZ) output waveform $V_o = V_{o1} - V_{o2}$. V_o has a voltage range between $+MI_uR_L$ and $-MI_uR_L$ and a step size of $2I_uR_L$.

DAC static linearity, which is specified as differential nonlinearity (DNL) and integral nonlinearity (INL), is mainly determined by the matching of I_u among different current cells and the output resistances of the I_u current sources. There are techniques to improve static linearity, which will not be covered in this brief. However, even with ideal I_u current sources, dynamic nonlinearity still occurs. It is manifested as spurious-free dynamic range (SFDR) degradation shown in the V_o output spectrum when the $D_i[k]$ input is a single-tone sine wave. The SFDR decreases rapidly with increasing input frequency. The sources of dynamic nonlinearity are numerous and complex, including code-dependent switching transients [6], [7] and the capacitive output impedance of the current cells [5], [12], [13].

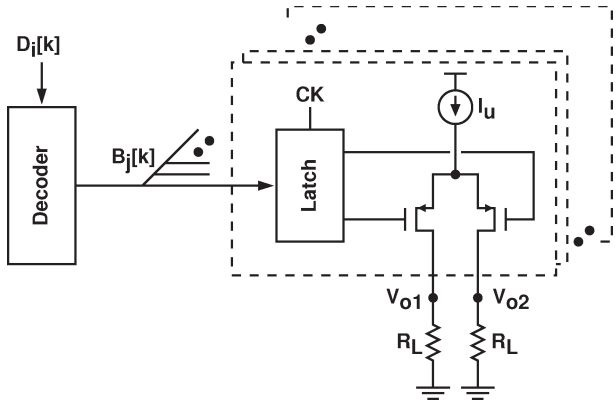

Fig. 1. Current-steering DAC.

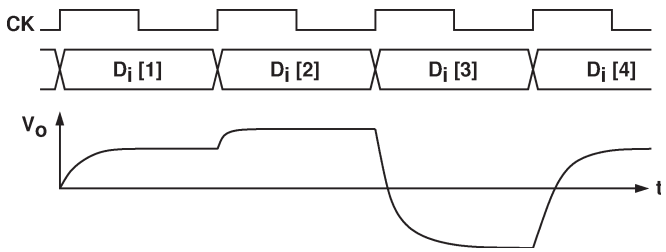

Fig. 2. NRZ output waveform of a current-steering DAC.

The return-to-zero (RZ) technique has been proposed to improve the DAC dynamic performance [6], [8], [9]. The technique adds an output buffer to isolate the output loads from the current switches and executes current-switching operation during the zero phase. The DAC dynamic performance can also be improved by modifying the current-switching operation to make the switching transients uncorrelated with the input sequence [2], [10], [11].

In this brief, we propose a digital random RZ (DRRZ) technique to mitigate the effect of switching transients on the DAC dynamic performance. An 8-bit 1.6-GS/s current-steering DAC chip was designed to demonstrate the proposed technique. The rest of this brief is organized as follows. Section II introduces the DRRZ technique. Section III describes the circuit implementation of the DAC chip. Section IV shows the experimental results. Section V draws conclusions.

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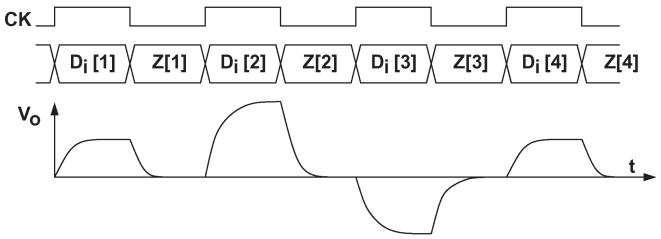

Fig. 3. Waveforms of an RZ DAC.

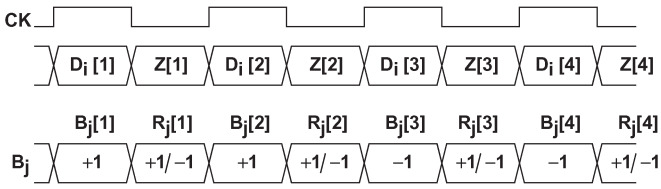

Fig. 4. Switching behavior of a current cell in a DRZ DAC or a DRRZ DAC.

II. DRRZ

Consider the jth current cell of the DAC shown in Fig. 1. Its current switch is driven by $B_j[k] \in \{-1, +1\}$. When CK changes from low to high, the current switch may remain unchanged or undergo a (-1)-to-$(+1)$ or a $(+1)$-to-(-1) switching. When the current switch makes a switching, the DAC output V_o experiences a transient disturbance called switching transient. The (-1)-to-$(+1)$ and $(+1)$-to-(-1) switching transients have opposite polarities. For the NRZ DAC, the switching of the current cells is determined by the input $D_i[k]$. Thus, the switching transients are input dependent and will result in DAC dynamic distortion.

Analog RZ (ARZ) has been used to hide the switching transients from the output [6], [8], [9]. The CK and V_o waveforms of Fig. 3 show the ARZ operation. When CK is high, the DAC is in the data phase. It decodes the digital input $D_i[k]$, sets up its internal current switches, and generates the analog output V_o corresponding to $D_i[k]$. When CK is low, the DAC is in the zero phase. The DAC output V_o is forced to zero by analog switches added at output nodes V_{o1} and V_{o2}. The current switches in the DAC are switched to reflect the next input $D_i[k+1]$ during the zero phase. Thus, the switching transients do not appear in V_o to contribute dynamic distortion. The analog switches at the output nodes must be large enough to eliminate switching transients.

We can generate the RZ V_o waveform without using the analog switches at the output nodes. As shown in Fig. 3, when CK is low, the DAC is in the zero phase $Z[k]$, in which the DAC arranges its internal current switches in such a way that the output $V_o = 0$. In the $Z[k]$ state, the switch controls $B_j[k]$ are reset to predefined values such that $\sum_{j=1}^{M} B_j[k] = 0$, assuming that M is an even number. However, in this digital RZ (DRZ) setup, switching transients appear in V_o. Consider the jth current cell. The sequence of its switching control B_j is shown in Fig. 4. When CK is high, $B_j = B_j[k]$ is determined by the input $D_i[k]$. When CK is low, $B_j = R_j[k]$ is a fixed value of either $+1$ or -1. In Fig. 4, $B_j[1] = +1$ and $B_j[2] = +1$ have the same value. If $R_j[1] = +1$, there will be no switching during the $Z[1]$ period. If $R_j[1] = -1$, there will be $(+1)$-to-(-1) and (-1)-to-$(+1)$ transients on both edges of the $Z[1]$ period. Fig. 4 also shows that $B_j[2] = +1$ and $B_j[2] = -1$ have different values. If $R_j[2] = +1$, a $(+1)$-to-(-1) transient occurs at the right edge of the $Z[2]$ period. If $R_j[2] = -1$, a $(+1)$-to-(-1) transient occurs at the left edge of the $Z[2]$ period. In summary, DRZ assigns a constant to $R_j[k]$, i.e., $R_j[k] = +1$ for all k or $R_j[k] = -1$ for all k. The current switch transitions are determined by the $B_j[k]$ sequence alone. Their strong correlation with the input $D_i[k]$ yields distortion in V_o. DRZ, in fact, introduces more input-dependent switching transients than NRZ.

We propose the DRRZ technique to randomize the switching transients appearing in DRZ. In this scheme, the switch controls $B_j[k]$ in the $Z[k]$ phase are dictated by a pseudorandom number generator (PRNG), such that $\sum_{j=1}^{M} B_j[k] = 0$. Consider the jth current cell and the operation sequence shown in Fig. 4. When CK is high, $B_j = B_j[k]$ is determined by the input $D_i[k]$. When CK is low, $B_j = R_j[k]$ becomes a binary random variable, which has a value of either $+1$ or -1. In Fig. 4, $B_j[1] = +1$ and $B_j[2] = +1$ have the same value. Switch transitions occur only if $R_j[1] = -1$. Fig. 4 also shows that $B_j[2] = +1$ and $B_j[2] = -1$ have different values. A switch transition occurs at the right edge of the $Z[2]$ period if $R_j[2] = +1$. On the other hand, a switch transition occurs at the left edge of the $Z[2]$ period if $R_j[2] = -1$. In summary, DRRZ makes $R_j[k]$ a random sequence, which randomizes the current switch transitions. When the switching transients are not correlated with the input $D_i[k]$, they appear as noises in V_o and will not cause distortion.

III. Circuit Descriptions

Fig. 5 shows the block diagram of the 8-bit DAC. It is segmented into a 5-bit equally weighted most significant bit (MSB) DAC (M-DAC) and a 3-bit binary-weighted least significant bit (LSB) DAC (L-DAC). The M-DAC comprises 31 identical current cells. Each current cell can output a current of $8I$, where I is the DAC unit current. The L-DAC comprises four current cells, which output currents of $1I$, $1I$, $2I$, and $4I$, respectively. There are two $1I$ current cells in the L-DAC so that a differential output of zero can be realized. The nodes I_{o1} and I_{o2} of all current cells are tied together to form two differential DAC output terminals. The two output terminals are connected to two R_L resistors to generate the differential V_o, as illustrated in Fig. 1. When CK is high, the decoder controls both the M-DAC and the L-DAC. The current of the extra $1I$ current cell in the L-DAC is always directed to the I_{o1} node. The DAC output is expressed as $V_o[k] = (D_i[k] - 127) \times 2IR_L$, where $D_i[k]$ is an integer from 0 to 255. In our design, $I = 80\ \mu$A and $R_L = 25\ \Omega$ yield V_o with a differential signal range of 1 V_{pp}.

As shown in Fig. 5, each current cell contains a multiplexing (MUX) latch. When CK is high, the latch selects the $B_j[k]$ control from the $D_i[k]$ decoder for a normal DAC output. When CK is low, the latch selects the $R_j[k]$ control from a PRNG. The PRNG is a 16-bit linear feedback shift register. Its 16 outputs and their complements form the 32 $R_j[k]$ zero-phase controls. This arrangement ensures that $\sum_{j=1}^{32} R_j[k] = 0$. During the

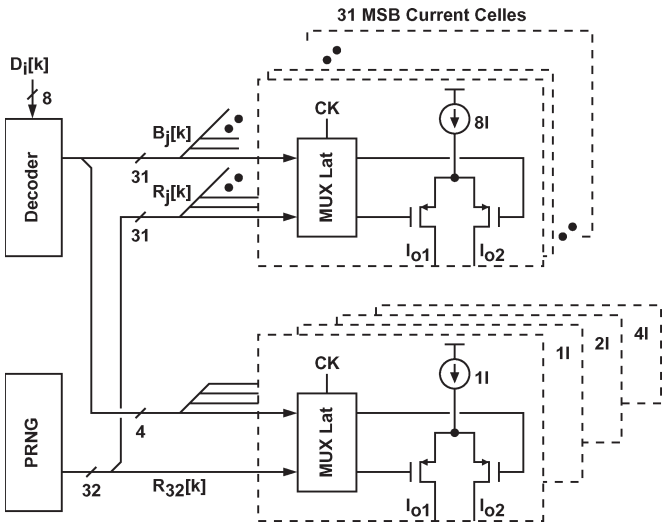

Fig. 5. DAC block.

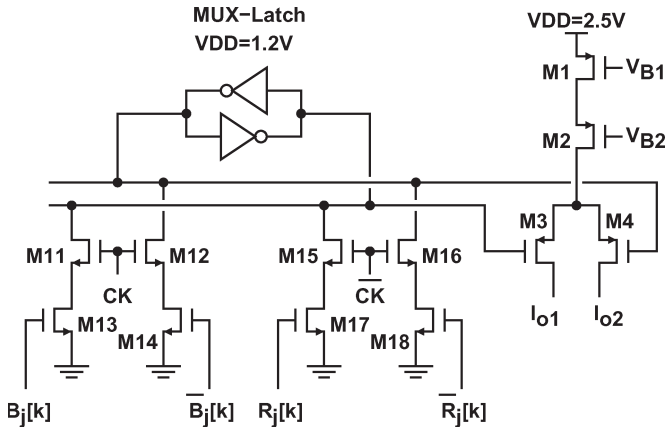

Fig. 6. Current cell schematic.

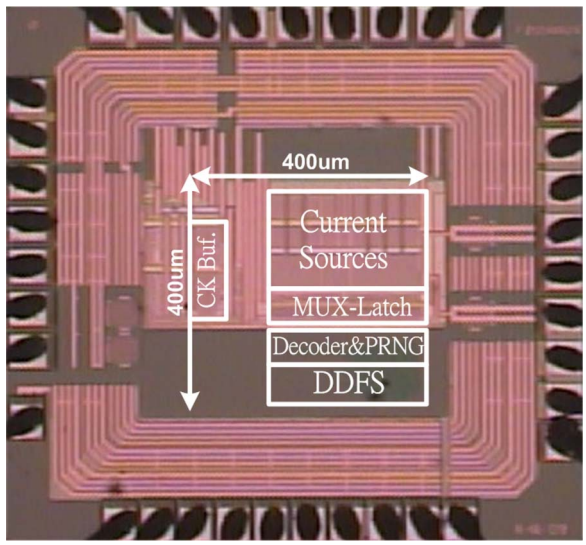

Fig. 7. Microphotograph of the DRRZ DAC.

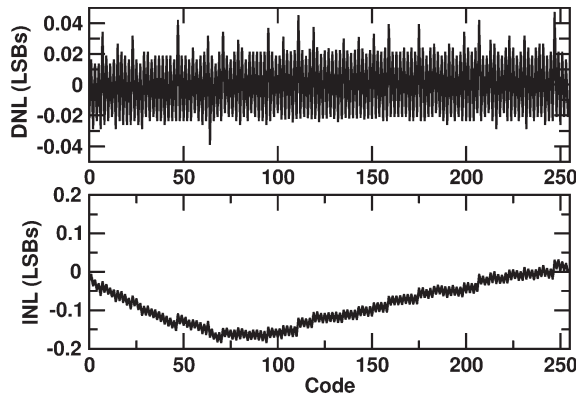

Fig. 8. Measured DNL and INL.

zero phase, the entire L-DAC is treated as a single MSB current cell controlled by a single $R_{32}[k]$ signal.

Fig. 6 shows the circuit schematic of a current cell. MOSFETs M1 and M2 form a cascode current source. M3 and M4 together function as a current switch. The current source is operated under a 2.5-V supply. M1–M4 are MOSFETs with thick gate oxide. MOSFETs M11–M18 and the two inverters form a level-sensitive MUX latch. When CK is high, the $B_j[k]$ signal is loaded into the latch. When CK is low, the $R_j[k]$ signal is loaded into the latch. The MUX latch is operated under a 1.2-V supply.

IV. Experimental Results

The DAC was fabricated in a standard 90-nm CMOS technology. Fig. 7 shows the chip photograph. The DAC core area is 400×400 μm^2. The chip also includes a direct digital frequency synthesizer (DDFS) to generate digital inputs for DAC testing. Fig. 8 shows the measured DNL and INL of the DAC. The DNL is $+0.04/-0.03$ LSB, and the INL is $+0/-0.2$ LSB.

Figs. 9 and 10 show the output spectra of the DAC operating at a 1.6-GS/s sampling rate, and the input frequency is 107 MHz. In Fig. 9, the DRRZ function is turned off, and the DAC output waveform is similar to NRZ V_o waveform shown in Fig. 2. In Fig. 10, the DRRZ function is turned on, and the DAC output waveform is similar to the RZ V_o waveform shown in Fig. 3. There are no significant harmonic tones in both figures. The measured SFDR is 65.4 dB for the NRZ DAC and 66 dB for the DRRZ DAC. When the input frequency of the DAC is low, the total number of current switches forced to switch is low in each clock cycle. The overall switching transients have little effect on the harmonic distortion of the DAC. Thus, the DRRZ function shows little improvement in the SFDR.

Figs. 11 and 12 are the DAC output spectra under similar conditions, except that the input frequency is raised to 731 MHz. When the input frequency of the DAC is high, the total number of current switches forced to switch is high in each clock cycle. The effect of switching transients becomes large and is revealed as the harmonic tones in Fig. 11. The SFDR is 43 dB and is dominated by the third harmonic. The harmonic tones are suppressed by the DRRZ operation, as illustrated in Fig. 12. The SFDR is improved to 56.5 dB.

Fig. 13 shows the measured SFDR of the DAC operated at a 1.6-GS/s sampling rate and with different input frequencies. The DAC has three different configurations, which are NRZ, DRZ, and DRRZ. For the NRZ DAC, the measured SFDR is

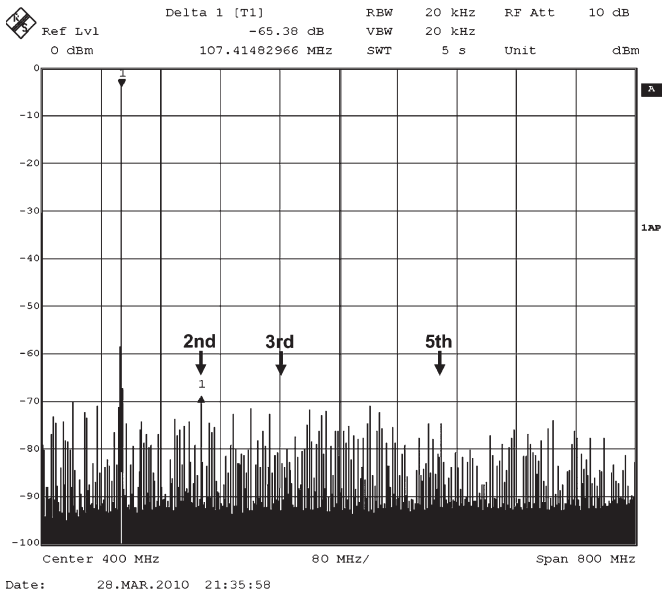

Fig. 9. Output spectrum of the DAC with NRZ. Sampling rate is 1.6 GS/s, and input frequency is 107 MHz.

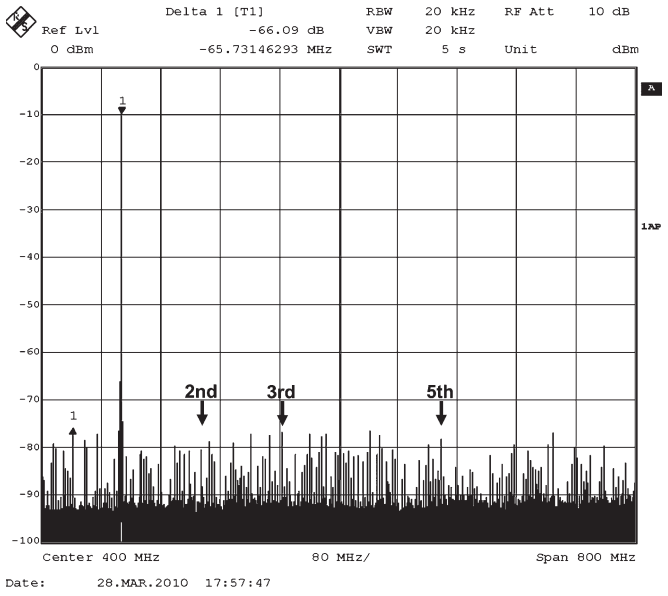

Fig. 10. Output spectrum of the DAC with DRRZ. The sampling rate is 1.6 GS/s, and the input frequency is 107 MHz.

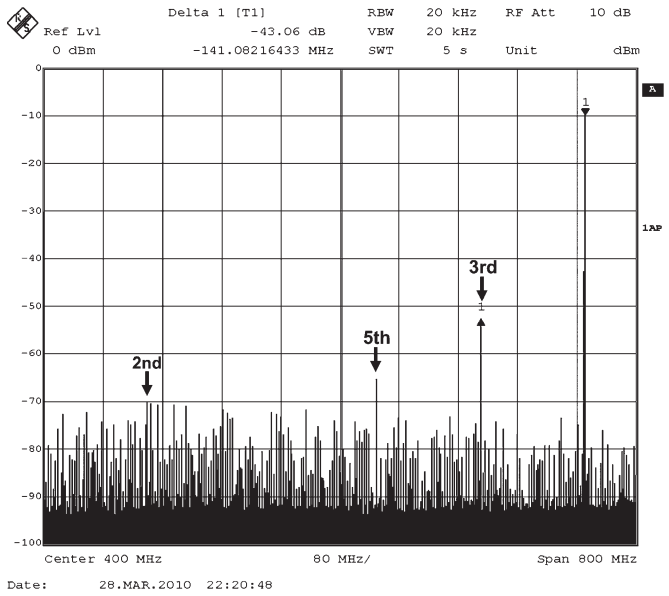

Fig. 11. Output spectrum of the DAC with NRZ. The sampling rate is 1.6 GS/s, and the input frequency is 731 MHz.

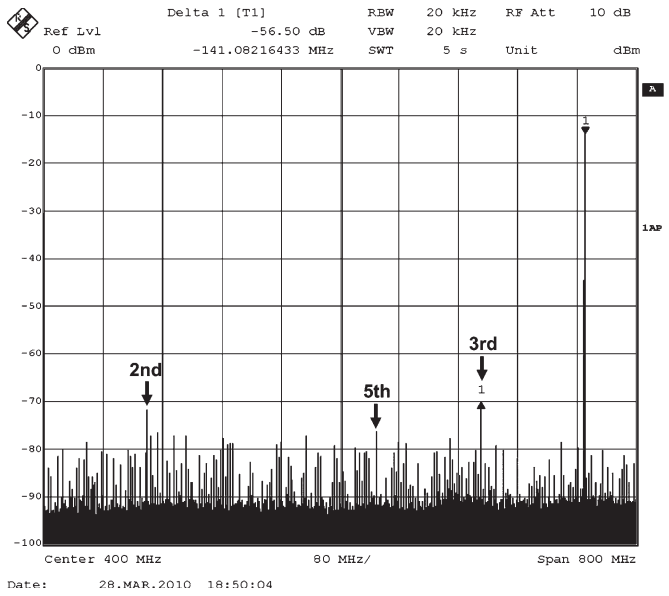

Fig. 12. Output spectrum of the DAC with DRRZ. The sampling rate is 1.6 GS/s, and the input frequency is 731 MHz.

degraded from 65 to 42 dB as the input frequency increases toward 800 MHz. Employing the DRRZ operation, the DAC can maintain an SFDR larger than 60 dB up to 460 MHz and an SFDR larger than 55 dB up to 800 MHz. Fig. 13 also shows the measured SFDR of the DRZ DAC. The DRZ setup cannot improve the SFDR at all. At low frequencies, the DRZ DAC exhibits an SFDR even worse than the NRZ DAC. This is because, at low frequencies, DRZ introduces more switching transients than NRZ.

Fig. 13 also shows a theoretical third-order harmonic distortion (HD3) calculation by considering only the output impedance of current cells [5], [12], [13]. It is expressed as

$$\text{HD3} = \left[\frac{M}{4} \cdot \frac{R_{L,d}}{|Z_o|}\right]^2 \tag{1}$$

where $R_{L,d} = 50\ \Omega$ is the differential resistance of the DAC output loads, $M = 32$ is the total number of M-DAC current cells, and Z_o is the output impedance of an M-DAC current cell. The L-DAC is treated as a single M-DAC current cell. Referring to Fig. 6, Z_o is the output impedance looking into the I_{o1} terminal when M3 is turned on and M4 is off. Z_o in our design can be modeled as a resistor $R_o = 1.9\ \text{M}\Omega$ in parallel with a capacitor $C_o = 10.8$ fF. Fig. 13 indicates that the HD3 of (1) is the major distortion source for the DRRZ DAC with input frequencies higher than 300 MHz. This type of distortion cannot be removed by DRRZ.

The DAC specifications are summarized in Table I. Fig. 14 compares the dynamic performance of this DAC against other published DAC works. In order to compare DACs of different

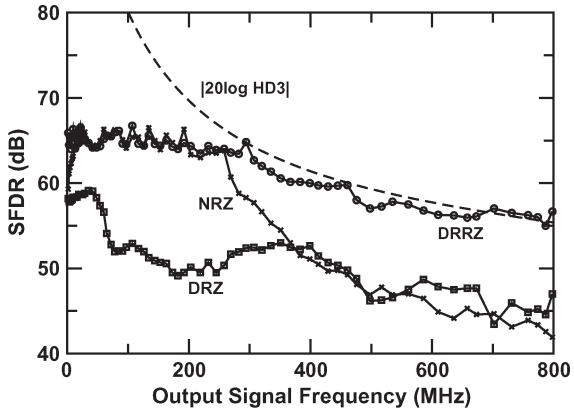

Fig. 13. Measured SFDR at different signal frequencies.

TABLE I
DAC PERFORMANCE SUMMARY

Technology	CMOS 90 nm
Resolution	8 Bits
Sampling Rate f_s	1.6 GS/s
DNL	+0.04 / −0.03 LSB
INL	+0.0 / −0.2 LSB
SFDR @f_{in} = 100 MHz	64.5 dB
SFDR @f_{in} = 700 MHz	57.0 dB
Load Current	20 mA
Output Swing	1 V_{pp}
Supply Voltage (Analog/Digital)	2.5 V / 1.2 V
Power Consumption	90 mW
Core Area	0.16 mm^2

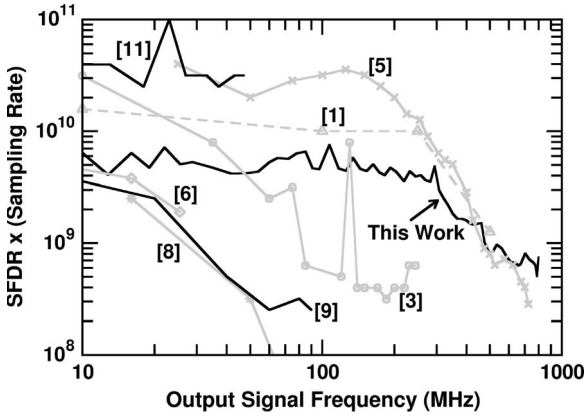

Fig. 14. Dynamic performance comparison of published DACs.

sampling rates, the dynamic performance is defined as SFDR $\times$ f_s, where SFDR is expressed in power ratio, and f_s is the sampling rate (in hertz). Note that the reported DAC is only an 8-bit design, but its dynamic performance is competitive at high signal frequencies.

V. CONCLUSION

A CMOS 8-bit 1.6-GS/s current-steering DAC has been presented to demonstrate the proposed DRRZ technique. The technique requires only a small overhead in digital circuits. The improvement in the SFDR of the DAC is 14 dB when the input frequency is 800 MHz.

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