Solid-State Electronics 55 (2011) 64–67

Contents lists available at ScienceDirect

Solid-State Electronics

journal homepage: www.elsevier.com/locate/sse

High-field mobility metal-gate/high-κ Ge n-MOSFETs with small equivalent-oxide-thickness

W.B. Chen [a], C.H. Cheng [a,b], C.W. Lin [c], P.C. Chen [c], Albert Chin [a,*]

[a] Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan, ROC
[b] Department of Electronics Engineering and Institute of Electronics, National Tsing Hua University, Hsinchu, Taiwan, ROC
[c] Department of Electronics Engineering, Chung Hua University, Hsinchu, Taiwan, ROC

ARTICLE INFO

Article history:
Received 8 July 2010
Received in revised form 5 September 2010
Accepted 6 September 2010
Available online 8 October 2010

The review of this paper was arranged by Prof. A. Zaslavsky

Keywords:
High-κ dielectric
Ge
EOT
Mobility

ABSTRACT

We fabricated high performance *gate-last* $TaN/La_2O_3/SiO_2$ on Ge n-MOSFET. Small equivalent-oxide-thickness (EOT) of 1.9-nm and high-field mobility of 258 $cm^2/V\,s$ at 0.75 MV/cm were obtained, which were attributed to the thin SiO_2-like barrier layer and low process temperature to prevent interfacial reaction during post-deposition annealing (PDA).

1. Introduction

Recently, the high performance metal–oxide–semiconductor field effect transistors (MOSFETs) with using high-κ materials such as La_2O_3 [2], Al_2O_3 [3], [19], HfO_2 [5] and mixed metal oxides have been proposed to replace the conventional SiO_2 MOSFETs for equivalent-oxide thickness (EOT) scaling. However, the scalable performance enhancement depends on channel length scaling, gate dielectric scaling and optimized strain engineering like SiGe source–drain and compressive contact etch stop layer (CESL). Ge channel is expected to additionally boost the mobility at thin EOT. Thus, much attention has been focused on Ge channel complementary metal oxide semiconductor field effect transistors (CMOSFETs) [1–22], which is due to 2–4 times higher electron and hole mobility than those of Si devices. Besides, the densities of states are ~50 times larger than III–V InGaAs substrate for higher drive current. However, the challenging issues of the small-bandgap-induced high leakage current, sensitive to process temperature and poor interface quality due to Ge out-diffusion are the major challenges.

To address these issues, the defect-free Ge-on-insulator (GOI or GeOI) [3] and thin body Ge-on-Si [17,18] are proposed. Nevertheless, the low electron mobility at high effective electronic field (E_{eff}) and poor equivalent-oxide thickness EOT scaling are still the unsettled issues. The lower peak mobility could be attributed to the coulomb scattering in the high-κ dielectric that was also found in high-κ/Si [27,29]. Such challenges become worst at gate-first process, where the high thermal budget degrades the mobility originated from interface reaction and Ge out-diffusion. Although several surface passivation approaches such as NH_3 surface treatment and Si-capping on Ge channel [8,10,12,21,22] were proposed, high-field mobility at small EOT still needs to be developed.

In this study, we reported the high-field mobility of Ge n-MOSFETs using $TaN/La_2O_3/SiO_2$ gate stack. The La_2O_3 dielectric [2,23,24] with high-κ value and negative flat band voltage (V_{fb}) are important for n-MOSFET. The metal-gate/device show high-field mobility of 258 $cm^2/V\,s$ at 0.75 MV/cm with a small 1.9-nm EOT. The results are ascribed to the SiO_2 barrier layer and low thermal budget process to suppress the Ge out-diffusion into high-κ dielectric.

2. Experimental procedure

We used a 2-in p-type Ge (1 0 0) wafers with a doping concentration of $5 \times 10^{14}\,cm^{-3}$ in these experiments. After standard clean, 500 nm isolation oxides were deposited by plasma-enhanced chemical vapor deposition (PECVD). Then active areas were defined by lithography and wet etching. After that As^+ was implanted at source and drain region at 25 keV and a dosage of $5 \times 10^{15}\,cm^{-2}$ and followed by a 550 °C rapid thermal annealing

* Corresponding author. Tel./fax: +886 3 5731841.
E-mail address: albert_achin@hotmail.com (A. Chin).

0038-1101/$ - see front matter © 2010 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2010.09.006

(RTA) for dopant activation. A 0.8 nm thick SiO_2 and 6 nm La_2O_3 were deposited by dual E-Gun evaporation system at a pressure of 2×10^{-6} torr and followed by a 400 °C post-deposition anneal (PDA) in an oxygen ambient for 5 min to densify the gate dielectric quality. A 150-nm-thick TaN metal was deposited and patterned to form the gate electrode by a sputter system at a pressure of 9×10^{-7} torr. Finally, the Ge *n*-MOSFET was formed by adding 300-nm-thick Al metal contacts to source–drain by thermal evaporation coater and annealed at 400 °C for 25 min in an N_2 ambient. Fig. 1a and b shows the schematic image and process flow. The fabricated devices were characterized by *C–V* and *I–V* measurements by HP4284A precision LCR meter and HP4156C semiconductor parameter analyzer, respectively. The devices were also analyzed by secondary ion mass spectroscopy (SIMS), and cross-sectional transmission electron microscopy (TEM).

3. Results and discussion

Fig. 2a and b shows the *C–V* and *J–V* characteristics of TaN/La_2O_3/SiO_2/Ge devices. The increasing PDA temperature from 350 to 450 °C improves the gate leakage current for several times, with only slight V_{fb} shift. The slight EOT increase with increasing PDA temperature is related to interfacial layer formation. At 400 °C PDA temperature, a capacitance density of 1.54 μF/cm^2 was measured that gave an EOT of 1.9 nm from quantum–mechanical *C–V* (*QM*–CV) simulation using Ge material parameters. Besides, a low leakage current of 8×10^5 A/cm^2 was reached at 1 V above V_{fb}. The *C–V* curves spreading with different PDA were mainly attributed to interface reaction. Compared to 350 °C and 450 °C, the capacitor with an optimized 400 °C PDA shows a corresponding thinner EOT of 1.9 nm and lowest leakage current at 1 V above V_{fb} shift. The large leakage and small capacitance density caused by serious interface oxidation for over high-temperature 450 °C explain the importance of thermal budget control during dielectric activation. The combined effect of thicker interfacial layer and poor interface state may lead to the performance degradation on capacitance density and leakage current. Thus, an appropriate PDA temperature not only can effectively activate the defect-rich dielectric but also suppress the serious interface oxidation, especially for Ge substrate.

We further analyzed the gate stack on Ge substrate by SIMS and TEM. Fig. 3a and b shows the SIMS depth profile and cross-sectional TEM image, respectively. No apparent Ge out-diffusion was found by SIMS that is important to reach mobility and low gate leakage for Ge MOSFET [22]. This is further confirmed by the sharp interface between La_2O_3/SiO_2 and Ge as observed by cross-sectional TEM. The sharp SiO_2-like layer formation may result from intermixing effect near Si interface which can reduce the Ge out-diffusion into high-κ La_2O_3 dielectric during optimized 400 °C PDA. Such SiO_2-like interface layer is also related to the low leakage current and *C–V* characteristics in Fig. 2.

Fig. 4a and b presents the I_d–V_d and I_d–V_g characteristics of TaN/La_2O_3/SiO_2/Ge *n*-MOSFET respectively, fabricated at a PDA low-temperature of 400 °C. Well-behaved transistor characteristics were reached, where a low threshold voltage (V_t) of −0.22 V was measured. The negative threshold voltage results from the negative V_{fb} shown in Fig. 1, which is important for Ge *n*-MOSFETs. Further V_t adjustment to positive can be obtained using higher work-function gate electrode in the future work. From the following

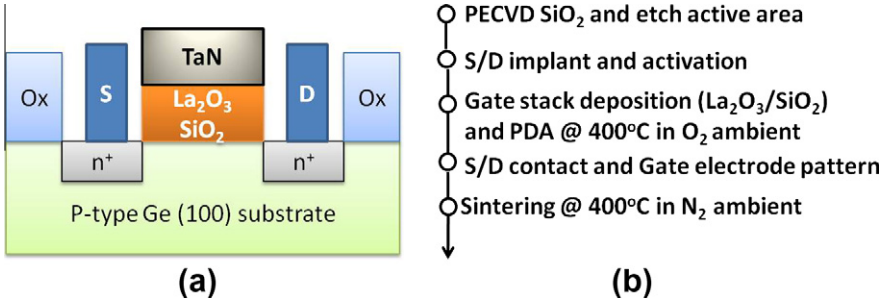

Fig. 1. (a) Schematic image of TaN/La_2O_3/SiO_2/Ge *n*-MOSFET and (b) process flow of *gate-last* Ge *n*-MOSFET.

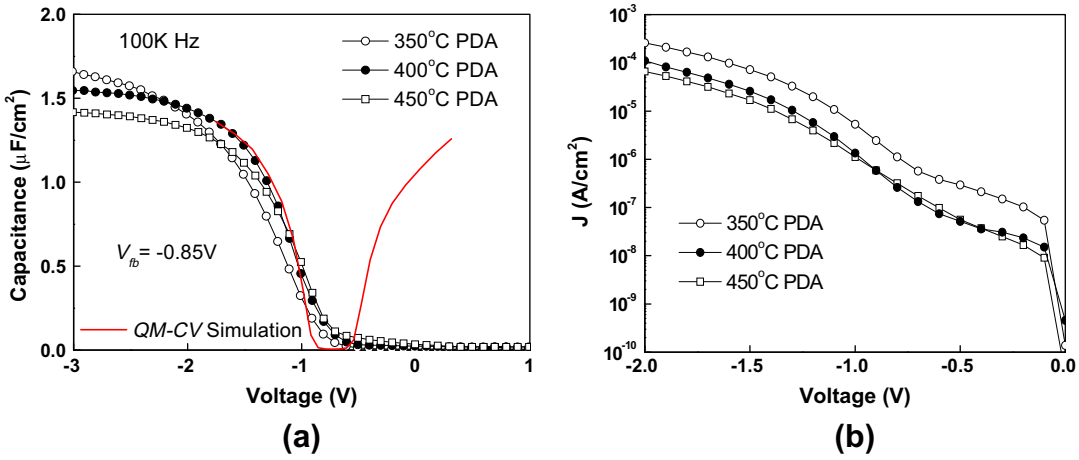

Fig. 2. (a) *C–V* and (b) *J–V* characteristics of TaN/La_2O_3/SiO_2/Ge *n*-MOS capacitors with different PDA temperatures.

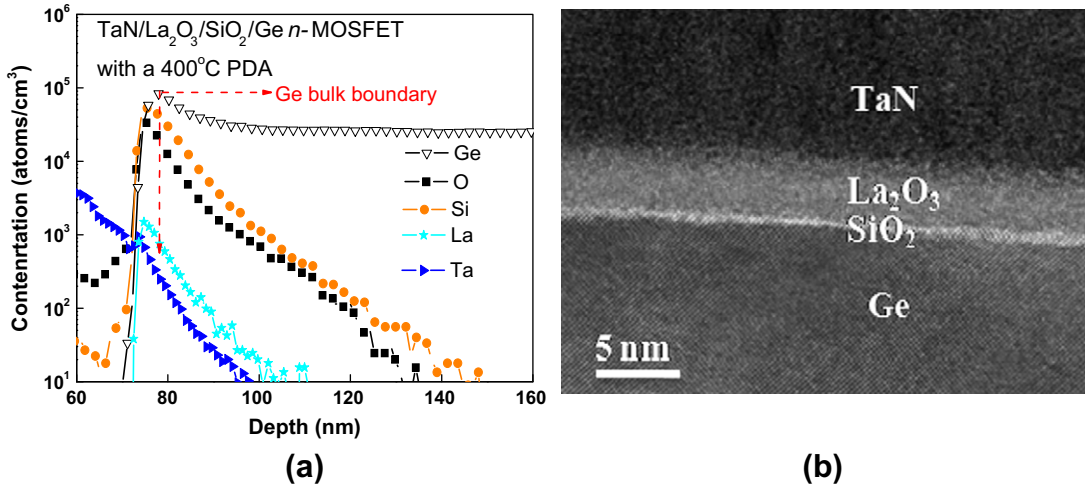

Fig. 3. (a) SIMS depth profile of TaN/La_2O_3/SiO_2/Ge at a 400 °C PDA. (b) Cross-sectional TEM of TaN/La_2O_3/SiO_2/Ge after a 400 °C PDA.

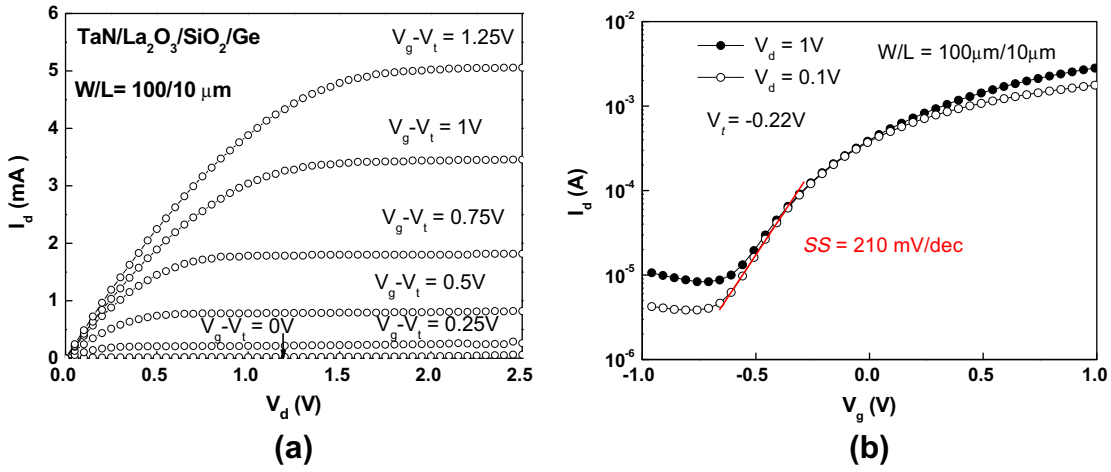

Fig. 4. (a) I_d–V_d and (b) I_d–V_g plots of TaN/La_2O_3/SiO_2/Ge *n*-MOSFET.

sub-threshold swing (*SS*) equation, it gives an interface trap density (D_{it}) of $9.5 \times 10^{12}\ eV^{-1}\ cm^{-2}$ [25]. The *SS* is degraded with the relative high D_{it} and the further improvement is required in the future.

$$SS = kT/q \times ln10 \times [1 + (C_{dep} + C_{it})/C_i]$$

where C_{dep}, C_{it} and C_i are the depletion capacitance density, capacitance density of charged interface traps, and gate capacitance density, respectively.

Fig. 5 shows the mobility as a function of E_{eff} over a wide range for the TaN/La_2O_3/SiO_2/Ge *n*-MOSFET. High peak mobility of 486 cm^2/V s and 0.75 MV/cm mobility of 258 cm^2/V s were measured at a small EOT of 1.9 nm. The mobility was directly calculated from the I_d–V_g curves and the equations are shown as the following [26]:

$$\mu_{eff} = I_d/(W_{eff}/L)C_{ox}(V_{gs} - V_t)V_{ds} \quad (a)$$

The effective normal field can be expressed as:

$$E_{eff} = (Q_{inv}/2 + Q_B)/\varepsilon_{Ge} \quad (b)$$

where Q_{inv} is the inversion layer charge, Q_B is the bulk depletion-layer charge and ε_{Ge} is the permittivity of Ge. Here the I_d versus V_g is extrapolated to zero drain current ($I_d = 0$) and the threshold voltage (V_{th}) is determined from intercept gate voltage (V_g).

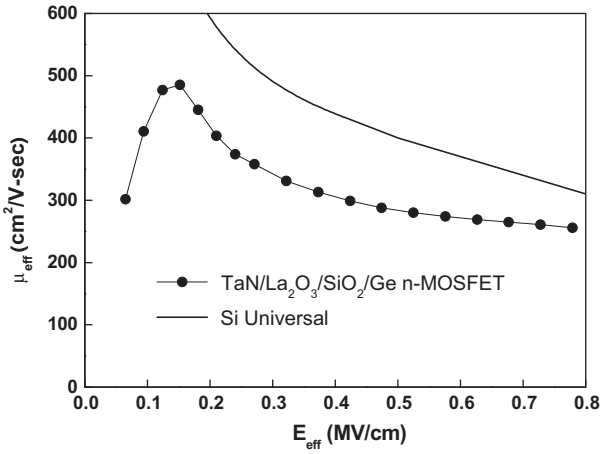

Fig. 5. The electron mobility as a function of effective electric field of TaN/La_2O_3/SiO_2/Ge *n*-MOSFETs.

Table 1
Comparison of device integrity data for various metal-gate/high-κ Ge *n*-MOSFETs.

Gate stack	Junction	EOT (nm)	Peak mobility (cm^2/V s)	Mobility @ 0.75 MV/cm (cm^2/V s)
Al/Al_2O_3/GeO_2/Ge [17]	P^+-implant, 350 °C RTA	–	488	258
Al/GeO_2(70-atm)/Ge [18]	P^+-implant, 580 °C RTA	–	790	366
Al/Al_2O_3/GeO_2/Ge [19]	600 °C gas phase doping	–	804	~210
Al/SiO_2/GeO_2/Ge/Si [20]	600 °C *in situ* doping	–	540	~134
TaN/La_2O_3/SiO_2/Ge (this work)	As^+-implant, 550 °C RTA	**1.9**	**486**	**258**

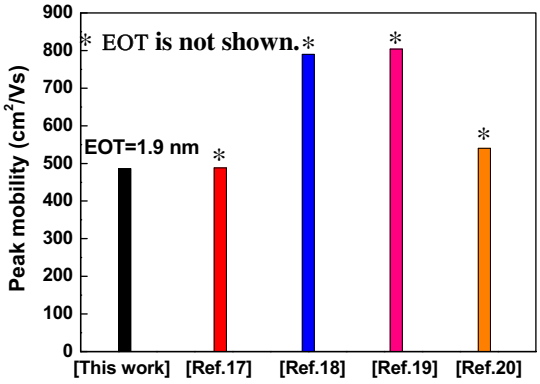

Fig. 6. The comparison of electron peak mobility of Ge *n*-MOSFETs.

Although many studies have been proposed for high performance and high peak mobility, the scaling down is also the issue for large EOT. High transistor current (I_d) due to the following relation:

$$I_d = WC_{inv}V_{eff}(V_g - V_t)$$

Here the v_{eff} is effective source velocity and related to high-field effective mobility [28], since the MOSFET is biased at $V_g = V_{d,sat}$ for higher I_d rather than at a low V_g with good peak mobility. Such high field operation is inevitable for MOSFET at highly scaled EOT used for advanced Ge CMOSFETs technology node.

Table 1 summarizes the important device parameters of metal-gate/high-κ Ge *n*-MOSFETs [17–20]. Fig. 6 shows the peak mobility comparisons of references in Table 1. Our TaN/La_2O_3/SiO_2/Ge *n*-MOSFET has high-field mobility of 258 cm^2/V s at 0.75 MV/cm at the smallest 1.9-nm EOT.

4. Conclusion

We have demonstrated a high performance Ge *n*-MOSFET using high-κ La_2O_3/SiO_2 stack dielectric, suitable for future EOT scaling. Device performance of high 258 cm^2/V s at 0.75 MV/cm and small EOT of 1.9-nm are reached simultaneously, which is due to the smooth interface observed by TEM.

Acknowledgment

This work was supported in part by National Nano Project, National Science Council of Taiwan.

References

[1] Chui C, Kim H, Chi D, Triplett BB, McIntyre PC, Saraswat KC. IEDM Technol Dig 2002:437–40.
[2] Huang CH, Chen SB, Chin A. IEEE Electron Dev Lett 2002;23:710–2.
[3] Huang CH, Yang MY, Chin A, Chen WJ, Zhu CX, Cho BJ et al. In: VLSI Symp Technol Dig; 2003. p. 119–20.
[4] Low T, Hou YT, Lin MF, Chunxiang Zhu, Kwong D.-L, Albert Chin. In: VLSI Symp Technol Dig; 2003. p. 117–8.
[5] Bai WP, Lu N, Liu J, Ramirez A, Kwong DL, Wristers D et al. In: VLSI Symp Technol Dig; 2003. p. 121–2.
[6] Huang CH, Yu DS, Chin A, Chen WJ, Zhu CX, Li M-F, et al. IEDM Technol Dig 2003:319–20.
[7] Low T, Hou YT, Li MF, Zhu C, Chin A, Samudra1 G, et al. IEDM Technol Dig 2003:691–4.
[8] Wu N, Zhang Q, Zhu C, Chan DSH, Du A, Balasubramanian N, et al. IEEE Electron Dev Lett 2004;25:631–3.
[9] Chin A, Kao HL, Tseng YY, Yu DS, Chen CC, McAlister SP et al. In: Eur Solid State Dev Res Conf, (ESSDERC) Technol Dig; 2005. p. 285–8.
[10] Yeo CC, Cho BJ, Gao F, Lee SJ, Zhu CX, Lee MH, et al. IEEE Electron Dev Lett 2005;26:761–3.
[11] Bai WP, Lu N, Kwong D-L. IEEE Electron Dev Lett 2005;26:378–80.
[12] Takahashi T, Nishimura T, Chen L, Sakata S, Kita K, Toriumi A. IEDM Technol Dig 2007:697–700.
[13] Kobayashi M, Irisawa T, Kope BM, Sun Y, Saraswat K, Wong H. -SP. In: VLSI Symp Technol Dig; 2009. p. 76–7.
[14] Park JH, Tada M, Kuzum D, Kapur P, Yu HY, Wong H-SP, et al. IEDM Technol Dig 2008:389–92.
[15] Nakakita Y, Nakane R, Sasada T, Matsubara H, Takenaka M, Takagi S. IEDM Technol Dig 2008:877–80.
[16] Houssa M, Pourtois G, Caymax M, Meuris M, Heyns MM. Appl Phys Lett 2008;92:242101.
[17] Kuzum Duygu, Krishnamohan Tejas, Nainani Aneesh, Sun Yun, Pianetta Piero A, Wong H S-P, et al. IEDM Technol Dig 2009:453–6.
[18] Lee CH, Nishimura T, Saido N, Nagashio K, Kita K, Toriumi A. IEDM Technol Dig 2009:457–60.
[19] Morii K, Iwasaki T, Nakane R, Takenaka M, Takagi S. IEDM Technol Dig 2009:681–4.
[20] Yu H-Y, Kobayashi M, Jung WS, Okyay AK, Nishi Y, Saraswat KC. IEDM Technol Dig 2009:685–8.
[21] Chen WB, Chin Albert. Appl Phys Lett 2009;95:212105.
[22] Chen WB, Albert Chin. IEEE Electron Dev Lett 2010;30:80–2.
[23] Wu YH, Yang MY, Chin A, Chen WJ. IEEE Electron Dev Lett 2000;21:341–3.
[24] Yang MY, Yu DS, Albert Chin. J Electrochem Soc 2004;151:162.
[25] Chang MF, Lee PT, McAlister SP, Albert Chin. IEEE Electron Dev Lett 2008;29:215–7.
[26] Sun SC, Plummer JD. IEEE Trans Electron Dev 1980;27:1497–8.
[27] Heh D, Bersuker G, Huang J, Kirsch PD, Tseng H.-H., Jammy R. Eur Solid State Dev Res Conf, (ESSDERC) Technol Dig; 2009. p. 257–60.
[28] Kobabyashi M, Mitard1 J, Irisawa T, Hoffmann T.–Y, Meuris M, Saraswat K et al. In: VLSI Symp Technol Dig; 2010. p. 215–6.
[29] Zhang Z, Song SC, Quevedo-Lopez MA, Choi K. IEEE Electron Dev Lett 2006;27:185–7.