Acknowledgment: This work was supported in part by Tektronix and by the National Science Foundation under grant No. MIP 91-21360.

© IEE 1994 6 December 1993
Electronics Letters Online No: 19940185

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References

1 PENNOCK, J.L.: 'CMOS triode transconductor for continuous-time active integrated filters', *Electron. Lett.*, 1985, **21**, pp. 817–818
2 GATTI, U., MALOBERTI, F., and TORELLI, G.: 'A novel CMOS linear transconductance cell for continuous-time filters'. Proc. IEEE Int. Symp. Circ. Syst., 1990, pp. 1173–1176
3 CASTELLO, R., MONTECCHI, F., ALINI, R., and BASCHIROTTO, A.: 'A very linear BiCMOS transconductor for high-frequency filtering applications'. Proc. IEEE Int. Symp. Circ. Syst., 1990, pp. 1364–1367
4 STEFANELLI, B., and KAISER, A.: 'CMOS triode transconductor with high dynamic range', *Electron. Lett.*, 1990, **26**, pp. 880–881
5 NAUTA, B., KLUMPERINK, E., and KRUISKAMP, W.: 'A CMOS triode transconductor'. Proc. IEEE Int. Symp. Circ. Syst., 1991, pp. 2232–2235
6 SACKINGER, E., and GUGGENBUHL, W.: 'A high-swing, high-impendance MOS cascode circuit', *IEEE J. Solid-State Circuits*, 1990, **SC-25**, pp. 289–298
7 BULT, K., and GEELEN, G.J.: 'A fast-settling CMOS op amp for CS circuits with 90-dB DC gain', *IEEE J. Solid-State Circuits*, 1990, **SC-22**, pp. 1366–1384
8 WYSZYNSKI, A., and SCHAUMANN, R.: 'Frequency and phase tuning of continuous-time integrated filters using common-mode signals'. Submitted to IEEE Int. Symp. Circ. Syst., October 1993

New observation of charge injection in MOS analogue switches

M.-J. Chen, Y.-B. Gu, T. Wu, P.-C. Hsu and T.-H. Liu

Indexing terms: Integrated circuits, Switched capacitor networks

Based on experimental analogue MOS switches, the Letter reports a new observation of the charge injection component due to channel charges in weak inversion. As identified by the mixed-mode circuit and device simulations, this new component can contribute comparably to the switch-induced error voltage on a switched capacitor.

Introduction: Charge injection in analogue MOS switches has recently been studied extensively [1–4]. Suppression of the charge injection-induced error voltage on a switched holding capacitor is very important for switched-capacitor circuits. In this Letter we report a new observation of the charge injection component due to channel charges in weak inversion, which has not previously been observed experimentally or predicted theoretically.

Experimental observations: The on-chip test circuitry consists of one *n*-channel MOSFET, a holding capacitor C_H, and a unity-gain operational amplifier, as shown in Fig. 1. This test circuitry has been fabricated by a 1.2 μm double-metal double-polysilicon CMOS process. The gate voltage waveform $V_G(t)$ is given a pulse width t_w ranging from 1μs to 100μs and a fall time t_f from 6ns to 5μs. Because the unity-gain operational amplifier is used as a buffer, the waveform $V_H(t)$ on the holding capacitor can be represented by the measured waveform at the output. We have found that the new role of the channel charges in weak inversion is reproducible for a variety of the design parameters and measurement conditions. The case $W = 25$μm, $L = 4$μm, and $C_H = 1.0$PF, at the measurement condition of $V_{in} = 2$V, $t_w = 10$μs, and $t_f = 0.6$μs, is presented here. The corresponding observed waveforms at the gate and the output are shown in Fig. 1. Also shown in Fig. 1 is the waveform of the drain current $I_D(t)$. According to [1], the turn off of an MOS switch consists of two distinct phases: $t_1 < t < t_2$ and $t_2 < t < t_1 + t_f$ as labelled in Fig. 1. Here t_2 represents the

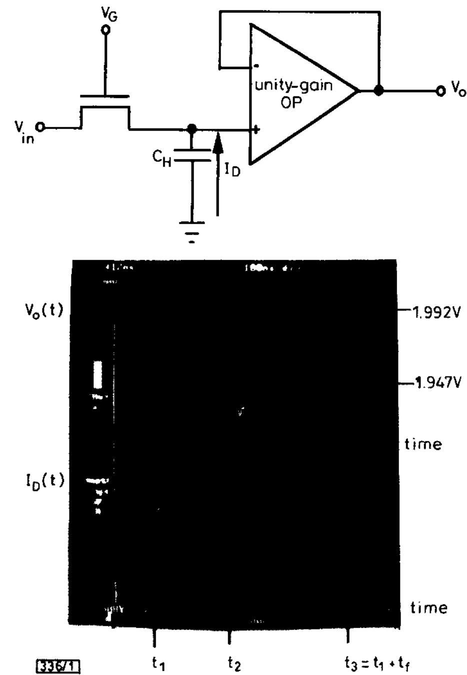

Fig. 1 *Schematic on-chip test circuity and measured voltage waveforms at gate and output*

Waveform $I_D(t)$ created by Tektronix 11402A is shown together. The horizontal scale is 100ns/division. The vertical scales for $V_G(t)$, $V_o(t)$, and ID(t) are 1V/division, 20mV/division, and 20nA/division, respectively. $t_1 = -300$ns, $t_2 = -40$ns, and $t_3 = 300$ns. The offset of the unity-gain opamp is ~8mv

time for the gate voltage $V_G(t)$ reaching the sum of the input voltage V_{in} and threshold voltage V_{th}. During the first phase, i.e. $t_1 < t < t_2$, some of the channel mobile charges are injected into the switched capacitor. At $t_1 = t_2$, the conduction channel disappears and the transistor enters the second phase of turn-off [1]. Therefore according to [1], the $I_D(t)$ curve for $t_2 < t < t_1 + t_f$ would be a constant because the $V_G(t)$ is a ramp voltage in this period. However, this is inconsistent with the $I_D(t)$ curve observed in Fig. 1 for $t_2 < t < t_1 + t_f$, where the drain current continuously decays with time until a constant one appears. Therefore during the second phase of the turn-off, in addition to the clock feedthrough through the gate-to-drain overlap capacitance [1], the channel charges in weak inversion should be taken into account.

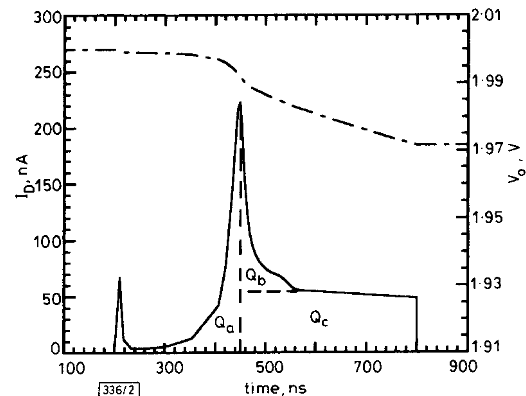

Fig. 2 *Simulated $V_o(t)$ and ID(t) waveforms under same conditions as Fig. 1*

$L = 4$μm, $W = 25$μm, $C_H = 1$pF, $t_f = 600$ns, $V_{in} = 2$V
——— I_D
— — — V_o

Computer simulations: The mixed-mode circuit and device simulations by using the program MEDICI [5] have been performed on the MOS switch. The simulated waveforms under the same conditions as those in Fig. 1 are presented in Fig. 2. Surprisingly, the simulated $I_D(t)$ waveform in Fig. 2 matches quite closely the measured waveform in Fig. 1. In Fig. 2 the area under the $I_D(t)$ curve has been separated into three components Q_a, Q_b, and Q_c, where Q_a represents part of the channel charges in strong inversion for $t_1 < t < t_2$, Q_b represents the channel charges in weak inversion for $t_2 < t < t_1 + t_f$, and Q_c represents the charges coupled through the gate-to-drain overlap capacitance for $t_2 < t < t_1 + t_f$. From the simulated current vectors (not shown here), we have found that for $t_2 < t < t_1 + t_f$ not only do the channel charges flow laterally to the drain but also the charges coupled through the gate-to-drain overlap capacitance flow vertically to the drain. Note that for $t_2 < t < t_1 + t_f$ the MOSFET is operated in weak inversion where $V_G(t) < V_{in} + V_{th}$.

The impact: Based on the work of Sheu and Hu [1], the Q_a can be modelled analytically as

$$Q_a = \sqrt{\frac{\pi U C_H}{2\beta}}\,\frac{(2C_{ol} + C_{ox})}{2}\,\mathrm{erf}\left(\sqrt{\frac{\beta}{2UC_H}}V_{HT}\right) \quad (1)$$

where $U(= (V_H - V_L/t_f)$ is the falling rate, C_{ox} is the gate oxide capacitance, C_{ol} is the gate-to-drain overlap capacitance, $V_{HT} = V_H - V_{in} - V_{th}$, and $\beta = \mu C_{ox}W/L$. Moreover, Q_c can be expressed as [1]

$$Q_c = C_{ol}(V_{in} + V_{th} - V_L) \quad (2)$$

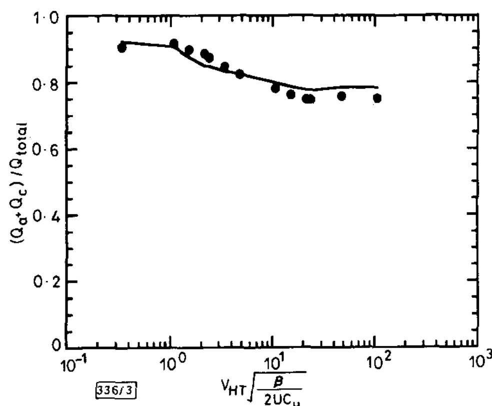

Fig. 3 *Simulated and calculated charge percentage $(Q_a+Q_c)/Q_{total}$ against parameter $V_{TH}\sqrt{\beta/2UC_H}$*

Value of total charge Q_{total} (= $Q_a + Q_b + Q_c$) comes from mixed-mode simulations

● mixed-mode simulations
—— eqns. 1 and 2

The validity of eqns. 1 and 2 has been identified by the mixed-mode circuit and device simulations, as demonstrated in Fig. 3 where the charge percentage against the dimensionless parameter $V_{HT}\sqrt{(\beta/2UC_H)}$ is shown. Fig. 3 reveals that neglecting Q_b can cause a considerably significant deviation. It has been found that as the channel length decreases and if the gate-to-drain overlap capacitance can be further reduced, both Q_a and Q_c decrease quickly. Under this condition, neglecting Q_b will underestimate seriously the error voltage.

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2 December 1993
Electronics Letters Online No: 19940177

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References

1 SHEU, B.J., and HU, C.: 'Switch-induced error voltage on a switched capacitor', *IEEE J. Solid-State Circuits*, 1984, **SC-19**, pp. 519–525

2 WILSON, W.B., MASSOUD, H.Z., SWANSON, E.J., GEORGE, R.T., and FAIR, R.B.: 'Measurement and modeling of charge feedthrough in n-channel MOS analog switches', *IEEE J. Solid-State Circuits*, 1985, **SC-20**, pp. 1206–1213

3 SHIEH, J.H., PATIL, M., and SHEU, B.J.: 'Measurement and analysis of charge injection in MOS analog switches', *IEEE J. Solid-State Circuits*, 1987, **SC-22**, pp. 277–281

4 WEGMANN, G., VITTOZ, E.A., and RAHALI, F.: 'Charge injection in analog MOS switches', *IEEE J. Solid-State Circuits*, 1987, **SC-22**, pp. 1091–1097

5 TMA MEDICI: 'Two - dimensional device simulation program'. Technology Modeling Associates, Inc., 1993

Testing analogue circuits by power supply voltage control

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Indexing terms: Analogue circuits, Testing, Integrated circuits

By varying the power supply voltages of an analogue integrated circuit as a testing technique it is possible to expose faults within the circuits which are difficult to detect by conventional input voltage stimulation. This technique is simple to implement and does not incur any area overhead penalty.

Introduction: Testing analogue integrated circuitry is a challenging task because many aspects of circuit performance need to be monitored such as functionality, transient response, bandwidth etc. An operational amplifier (opamp) is one of the most important analogue circuits and has received much attention from the testing community as a result [1–4].

In this Letter we have used a two stage opamp as a test vehicle because the technique we propose is well illustrated by such a circuit, but it is by no means constrained to this example in its application. This circuit is shown in Fig. 1. Of the possible faults which can occur in this circuit is a short circuit between the gate and the drain of transistor N4 which is difficult to detect by input voltage stimulation because the gate and the drain of this transistor often have similar potentials. This fault will become more difficult to expose if the short is a resistive short.

In this work faults were introduced singly, a short circuit was represented by a 1Ω resistor connected between two nodes and an open-circuit was modelled by a 10MΩ resistor between the open circuit nodes. Open-circuit gate faults have not been included because these are difficult to model or simulate with any degree of confidence.

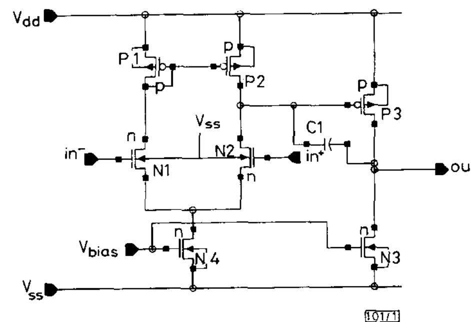

Fig. 1 *Operational amplifier*

Circuit under test: Fig. 1 shows a schematic diagram of the two stage opamp used as the circuit under test (CUT) in this work. The opamp was connected in inverting mode with two external