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Transient Effect Assisted NBTI Degradation in p-Channel LTPS TFTs under Dynamic Stress

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This work investigates dynamic negative bias temperature instability (NBTI) in p-channel low-temperature polycrystalline silicon thin-film transistors (LTPS TFTs) with different rise and fall times. Experimental results reveal identical increases in the interface state density (N_{it}) induced by different dynamic NBTI stress conditions. Nevertheless, the degradation of the grain boundary trap (N_{trap}) becomes more significant as rise time decreases to 1 μs. Because the surface inversion layer cannot form during the short rise time, transient bulk voltage will cause excess holes to diffuse into the poly-Si bulk. Therefore, the significant N_{trap} increase is assisted by this transient effect.
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Low-temperature polycrystalline-silicon thin-film transistors (LTPS TFTs) have been widely investigated for flat-panel applications, such as for active matrix liquid crystal displays and active-matrix organic light-emitting diodes.[1-3] Compared to amorphous silicon thin-film transistors (a-Si TFTs), LTPS TFTs have a higher electron mobility and driving current. Since the maximum process temperature is lower than 600°C, LPTS TFTs can be fabricated on relatively cheap glass. Consequently, the LTPS TFTs can integrate both the pixel array and peripheral circuits on the same glass substrate to realize a system-on-panel display.[4,5] Because drive circuits are designed using a CMOS inverter and therefore must suffer dynamic voltage pulses, negative bias temperature instability (NBTI) in p-channel LTPS TFTs under dynamic stress has been reported to be an important problem.[6-9] However, most studies have emphasized the recovery effect for threshold voltage during the dynamic voltage stress and have discussed the relationship between NBTI degradation and stress-frequency. The dependence of NBTI degradation on the period of transient variation of stress bias has not been analyzed in detail.

This work studies the NBTI effect in p-channel LTPS TFTs under various rise and fall times by extracting the interface state density (N_{it}) and the grain boundary trap density (N_{trap}) after NBTI stresses. In addition, the waveform and transient current were monitored by digital oscilloscope during dynamic stress to investigate the mechanism of device degradation. This analysis observed an increase in the bulk voltage in the transient region of the poly-Si bulk, which causes a diffusion of excess holes into the bulk when rise time is very short. This transient effect, therefore, is responsible for further degradation of grain boundary trap density (N_{trap}).

Experimental

In this work, the commercial standard p-channel LTPS TFTs fabricated on a Corning 1737 glass substrate with top-gate structures were prepared. First, a 500 nm thick buffer-oxide was deposited on the glass. Next, a 50 nm amorphous-Si (a-Si) film was deposited by plasma enhanced chemical vapor deposition (PECVD) at 380°C on the buffer-oxide, followed by dehydrogenation via furnace annealing process at 450°C. Then the a-Si films were crystallized by a 308 nm XeCl excimer laser with a line-shaped beam power of 350 mJ/cm^2. After patterning the films of polysilicon, 80 nm thick gate insulator was deposited by tetraethyl orthosilicate base oxide and 300 nm Mo was deposited as a gate metal by sputtering. After the gate metal definition process, the overlap between the gate and the source/drain regions are defined 0.75 μm and self-aligned boron implantation with a dose of 2×10^{15} cm^{-2} to form the P$^+$ regions at source/drain regions. The rapid thermal anneal irradiation process was performed to activate the dopant impurities after the source/drain regions implantation. The NH_3 plasma treatment was performed at 300°C to passivate the dangling bonds at the poly-Si/SiO_2 interface and at the grain boundaries. A 500 nm SiN_x layer was deposited by the PECVD as the interlayer dielectric. Finally, the contact holes were patterned by dry etching and Al metallization was performed. The cross-sectional view of the p-channel LTPS TFT is shown in Fig. 1. The thin-film transistors (TFTs) studied in this work are 6 μm in length and 10 μm in width.

The *I–V* curves and pulse waveform were measured by a Keithley 4200 semiconductor parameter analyzer and an Agilent DSO8104A digital oscilloscope, respectively. The measurements subsequent to the stress condition were performed with gate voltage sweeping from 5 to − 10 V, and the drain voltage was set to −0.1 V.

Results and Discussion

The dynamic NBTI stress waveform is shown in Fig. 2. A pulse with amplitude between 0 and −20 V was applied to the gate while source/drain were grounded. During the dynamic stress operation, times of high and low levels in the pulse period were fixed at 0.4 s and represented by T_{vg_high} and T_{vg_low}, respectively. The transient times of the gate pulse when switched from 0 to − 20 V and −20 to 0 V were defined as rise time (T_r) and fall time (T_f). In order to investigate the relationship between transient effect and

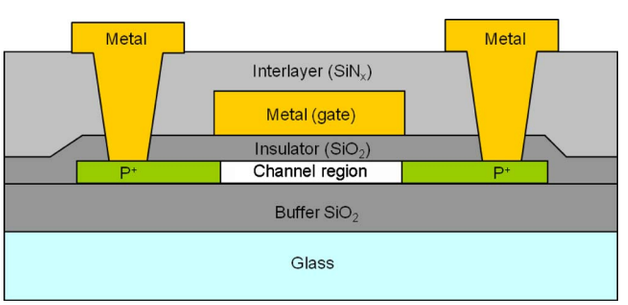

Figure 1. (Color online) Cross-sectional views of p-channel LTPS TFTs.

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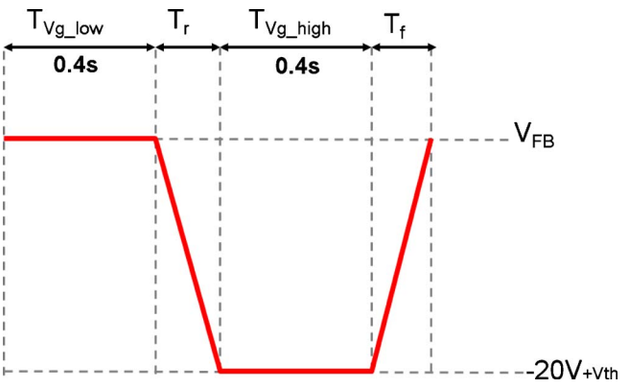

Figure 2. (Color online) Waveform of stress pulse applied to the gate.

dynamic NBTI induced degradation during the T_f and T_r, three stress conditions were performed. First, rise time and fall time were fixed to 0.1 s for standard NBTI stress. Either the rise time or fall time alone was reduced to 0.1 μs for the other two conditions. In all three stress conditions, the number of gate pulses was set at 2000 and the temperature was set at 125°C.

Figure 3 shows the linear I_d–V_g transfer characteristics of LTPS TFTs at the initial status and after standard NBTI stress. Subthreshold swing (S.S), transconductance (g_m), and on-current (I_{on}) were clearly degraded after the standard NBTI stress. In addition, the threshold voltage (V_{th}) after standard NBTI stress shifted in the negative direction. In general, V_{th} shift of TFT is caused by charge trapping or defect creation in the gate oxide. However, since charge trapping requires a high electric field across the gate oxide (above 6 MV/cm),[10] the electric field across this gate dielectric (about 3 MV/cm) is not high enough to cause hole injection. Therefore, the disorder-induced model could be eliminated.[11,12] Consequently, in this work, the degradation observed in S.S, g_m, and I_{on} can be considered to be mainly caused by conventional NBTI degradation.[10,13]

Figure 4 shows the negative shift of the threshold voltage ($-\Delta V_{th}$) as a function of stress pulse number under the different NBTI stress conditions. The V_{th} was defined as the gate voltage at which the drain current equals 10 nA in the subthreshold region. It can be seen from Fig. 4 that these $-\Delta V_{th}$ increase with an increase in stress pulse number, showing power law dependence. The exponent factor n can be extracted from the power law relationship, $V_{th} = At^n$,[14] where n is approximately 0.34 in this experiment. This value indicates that the diffusion-controlled electrochemical reaction

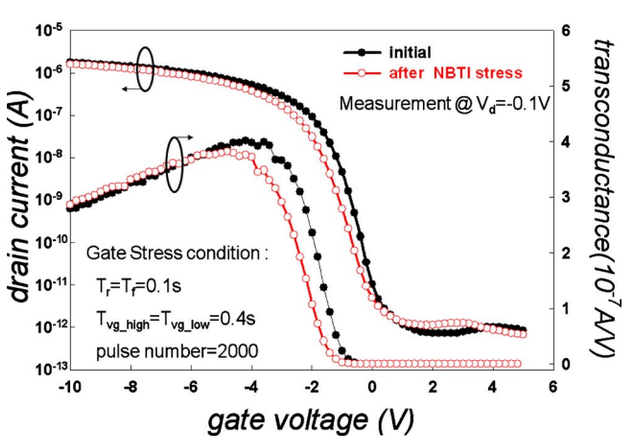

Figure 3. (Color online) I_d–V_g transfer characteristics when the device operates in the linear region for the LTPS TFT at the initial condition and standard NBTI stress condition.

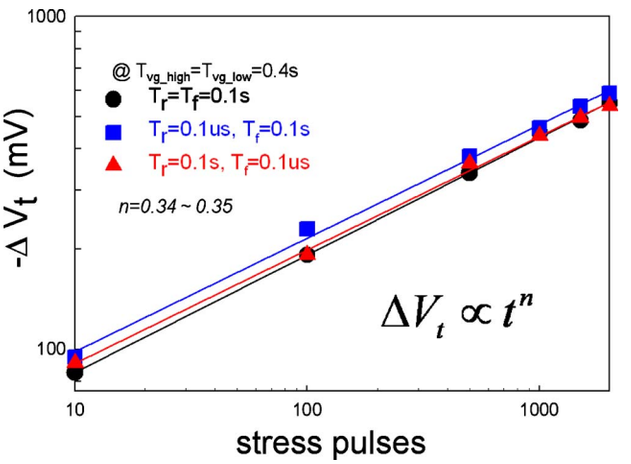

Figure 4. (Color online) Relationship between negative threshold voltage shift and number of stress pulses.

is the principal degradation mechanism for all the NBTI stresses.[15] These results are similar to those of our previous study,[16] which found that NBTI degradation originated from the interface state (N_{it}) increase and grain boundary trap (N_{trap}) increase. In order to understand the influences of rise and fall times on NBTI stress more clearly, the N_{it} and the N_{trap} increase for all stress conditions will be analyzed.

The N_{it} can be extracted from the S.S by ignoring the depletion capacitance in the active layer according to the following equation,[17] with N_{it} trap increase occurring not only at the SiO_2/poly-Si interface but also in the grain boundary in the weak inversion region. Here, the subthreshold swing is defined as half the gate voltage necessary to increase the drain current by 2 orders of magnitude (from 10^{-11} to 10^{-9} A) in the subthreshold region

$$N_{it} = \left[\left(\frac{S}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1\right]\left(\frac{C_{ox}}{q}\right) \quad [1]$$

Figure 5a shows the correlation between the N_{it} increase and the number of stress pulses for the three different rise and fall times. It is apparent that the N_{it} increase is independent of rise and fall times. The nearly identical N_{it} increase for these different stresses is due to the same T_{vg_high} and T_{vg_low}. The degradation was mainly due to the H dissociation caused by inversion holes during T_{vg_high} and the dissociated H recovery during T_{vg_low}.

The N_{trap} increase can be estimated by the Levinson and Proano method,[4,18] such that it includes the N_{it}. The relationship between the N_{trap} increase and the number of stress pulses is shown in Fig. 5b, where it is clear that the N_{trap} increase is more serious under stress with a shorter rise time but was independent of fall time. In n-channel TFTs, the main degradation mechanism was by the drain-avalanched hot-carrier induced impact ionization as a result of carriers being emitted from trap states when fall time is less than 1 ms.[19] However, in our experiment, the turn-off voltage was only 0 V and the ionization rate of the hole was lower than the ionization rate of the electron.[20] Therefore, the degradation of the grain boundary near the source/drain caused by the emitted carriers did not occur in this experiment. In order to understand the dominant mechanism in the N_{trap} increase for the short rise time, both the input gate voltage and the corresponding bulk voltage (V_{bulk}) were monitored by a digital oscilloscope, as shown in Fig. 6. The source was grounded, and the drain was connected to the 2-channel of the digital oscilloscope while the temperature was 125°C. The pulse voltage was applied to gate from the pulse generator and was connected to the 1-channel.

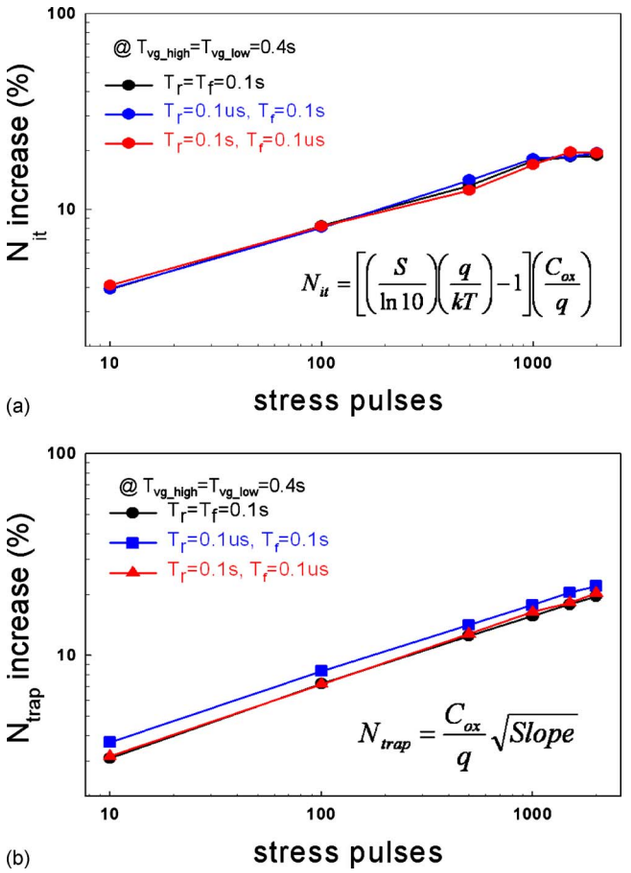

Figure 5. (Color online) Relationship between (a) N_{it} increase and (b) N_{trap} increase under different number of stress pulses.

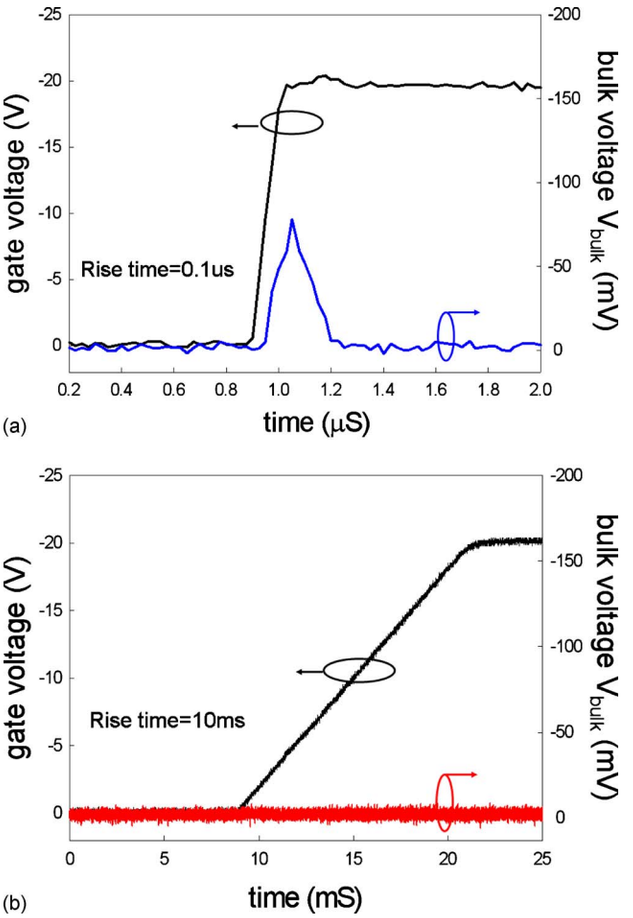

Figure 7. (Color online) Relationship between bulk voltage and gate voltage for rise times of (a) 0.1 μs and (b) 10 ms.

The relationship between the bulk voltage (V_{bulk}) and the gate voltage (V_g) is shown in Fig. 7a and b for T_r of 0.1 μs and 1 ms, respectively. It can be seen from Fig. 7a that there was a transient increase in the voltage of poly-Si bulk when the gate voltage was switched from 0 to − 20 V in a very short rise time (T_r = 0.1 μs). As the rise time is short, the inversion layer is not immediately formed at the interface between the SiO_2 and poly-Si, and the applied gate voltage is partially dropped at the bulk region, causing the transient bulk voltage increase. The typical turn-on time of the c-Si FETs is a few tens of nanoseconds.[21] This experimental result suggests that the switching delay in LTPS TFTs can be attributed to the high trap density. Figure 7b shows the gate voltage switched from 0 to − 20 V over a long rise time (T_r = 10 ms). Clearly, the V_{bulk} remains at 0 V, even during the transient time, because the inversion charges move along the channel as the gate pulse varies, finally electrically connecting the source and the drain. Therefore, the V_{bulk} is the same as the source voltage. Based on these results, we further analyzed the transient effect on drain current using a transient measurement system, as shown in Fig. 8. The gate terminal was connected to the 1-channel of the pulse generator and the digital oscilloscope, and the gate bias was changed from 0 to − 20 V. The drain was connected to the 2-channel of the pulse generator, which was switched from 0 to − 0.1 V. The source was connected to the input of a current-to-voltage converter (Keithley 428) such that the output voltage signal and the corresponding drain current could be

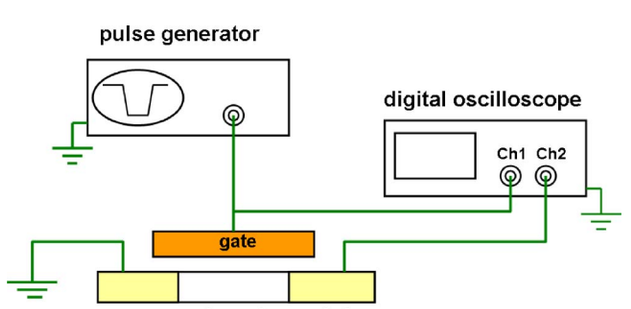

Figure 6. (Color online) Schematic view of an installation used to monitor V_{bulk}. The source was grounded, and the drain was connected to the 2-channel of the digital oscilloscope.

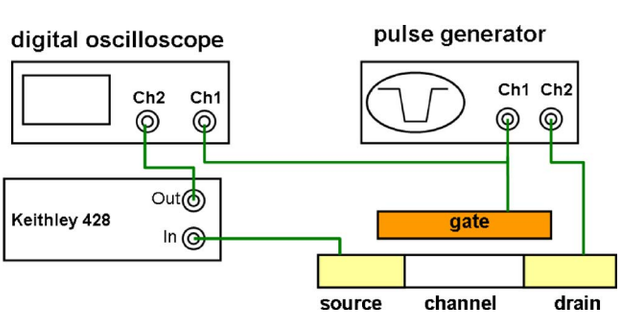

Figure 8. (Color online) Schematic of the transient measurement system.

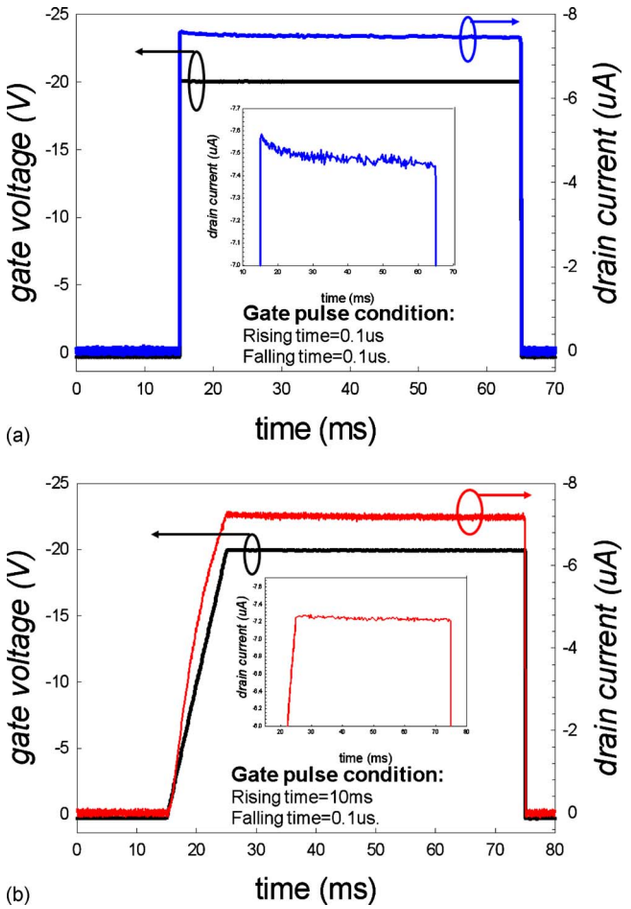

Figure 9. (Color online) Relationship between the transient drain current and the gate voltage for rise time of (a) 0.1 μs and (b) 10 ms, insets show the transient drain current under turn-on region.

displayed by the 2-channel of the digital oscilloscope. The measurement temperature was set to 125°C. The result of the transient current measurement was shown in Fig. 9.

Figures 9a and b show the relationship between the gate voltage and the transient drain currents under rise times of 0.1 μs and 0.1 ms, and the insets show only the transient drain current during the turn-on region. It can be seen from Fig. 9a, that the measured drain current exhibits the peak current at the beginning of the turn-on region and slowly returns to a steady current with the increasing measurement time. This phenomenon can be explained by recalling that, in Fig. 7a, the inversion layer is not immediately formed at the SiO_2/poly-Si interface, causing the transient bulk voltage in poly-Si bulk. When the negative voltage drops in the poly-Si bulk, holes will diffuse from the p-type source/drain into the Si bulk due to the forward bias. Therefore, excess holes cause the peak transient current to occur at the beginning of the turn-on region.[22] The corresponding energy band diagram is shown in Fig. 10. On the contrary, for a long rise time of 10 ms, the transient current is fixed to the steady value (steady-state current) during the turn-on time because the holes (inversion charges) can respond to the variation in the gate voltage.

Figure 10 shows the schematic energy band diagram of LTPS TFTs during different rise times. In the short rise time because the inversion layer is not formed immediately during such a short rise time, surface band bending is not apparent and part of V_g becomes dropped into the poly-Si bulk, resulting in excess holes diffusing from the source/drain. This phenomenon is also consistent with the result shown in Fig. 7a and 9a. Because there are many passivated

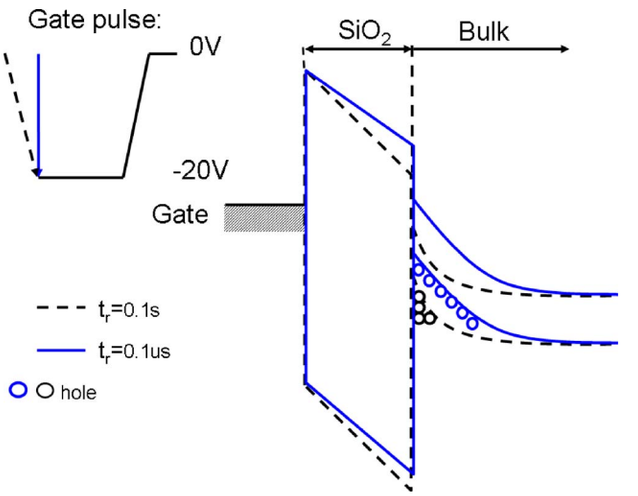

Figure 10. (Color online) Energy band diagram of LTPS TFT under different rise times.

Si–H bonds in grain boundaries in the poly-Si bulk region, the reaction between the transient-effect-induced excess holes and the Si–H bonds will cause a more serious N_{trap} increase in the poly-Si bulk during the NBTI stress. In addition, in the long rise time condition, the inversion layer forms immediately. Consequently, the main influence of the N_{trap} increase was the steady-state current.

Conclusion

In this work, dynamic NBTI stress in p-channel LTPS TFTs under different rise and fall times is investigated. Degradation occurred to the threshold voltage, subthreshold swing, and on-current in all kinds of dynamic NBTI stresses. For shorter and longer pulse rise time, the N_{it} increase is similar due to the dissociation of inversion holes and H at the interface at T_{vg_high}. Nevertheless, for a very short rise time, a pronounced N_{trap} increase is observed. This is because the inversion layer is not formed immediately and part of the gate voltage V_g is dropped into the poly-Si bulk, inducing excess holes. Therefore, the transient-effect-induced excess holes are the main reason for the more serious N_{trap} increase in the poly-Si bulk.

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