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Nickel Silicide Formation using Pulsed Laser Annealing for nMOSFET Performance Improvement

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The formation of a uniform, high tensile stress and low silicide/Si interfacial resistance nickel silicide in nMOSFET by introducing pulsed laser annealing (PLA) is reported. This annealing approach facilitated the phase transformation of nickel silicide to Si-rich $NiSi_x$ compounds using a low-thermal-budget process, improves the silicide/Si interface regularity and avoids familiar (111) $NiSi_2$ facet formation at a laser energy of 1.5 J cm^{-2}. By increasing laser energy density up to 2.3 J cm^{-2}, the device performance and statistics junction leakage distribution were degraded due to the increased sheet resistance of silicide layer and the destroyed silicide/Si interface morphology. When the PLA with a laser energy density of 1.5 J cm^{-2} was employed for nickel silicidation on the p-type Schottky diodes, a 0.16 eV hole Schottky barrier height (SBH) increase from 0.52 to 0.68 eV was observed. In addition, the application of PLA for source/drain silicidation of nMOSFETs demonstrated an 8% enhancement in $I_{on}-I_{off}$ characteristic relative to that obtained through the conventional two-step rapid thermal annealing (RTA). This PLA method holds promise as a potential replacement for current nickel silicide annealing approaches toward extremely scaled-down transistors.
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Although nickel silicide is a common silicide material used in advanced complementary metal-oxide-semiconductor (CMOS) transistors, Fermi-level pinning at the NiSi/n-Si interface sets the NiSi work function to a mid-gap value of 4.7 eV, causing high source/drain resistance of MOSFET. For this reason, techniques that can potentially reduce the NiSi Schottky barrier height (SBH) are of interest to expand the use of these materials in future transistors.[1–4] Among the various nickel silicide phases, single-crystalline and uniform $NiSi_2$ was previously reported to effectively reduce the electron SBH on n-type Si substrates.[5] Besides, $NiSi_2$ also provides higher tensile stresses than those of NiSi due to differences in material properties, which is favorable for carrier mobility enhancement in MOSFET.[6,7] These features make $NiSi_2$ an attractive replacement for NiSi as a silicide material. Nevertheless, the formation of the $NiSi_2$ at high temperatures usually favors the appearance of the more stable (111) facet on the (100) Si plane and causes rough morphology at silicide/Si interface.[8] A rough silicide/Si interface creates the possibility of junction spiking and limits the thickness to which the silicide layer can be grown, all of which adversely affect semiconductor performance. Although various approaches toward obtaining uniform silicide/Si interface were reported, there are were only a few reports of MOSFET device applications.[9–11] Herein, we present an annealing sequence that combines conventional rapid thermal annealing (RTA) with pulsed laser annealing (PLA) for silicidation. Introducing PLA provides sufficient energy to form $NiSi_2$, while minimizing the thermal budget relative to those of conventional furnace annealing approaches. Using this method for nickel silicidation on p-type Schottky diodes, we obtain smooth silicide/Si morphologies on (100) silicon interfaces while avoiding the problems of $NiSi_2$ (111) facet–induced junction leakage, leading to the silicide SBH modification for resistance reduction. After fundamental investigations on material and Schottky diode characteristics, we evaluate the performance of nMOSFET devices by introducing the PLA method during the source/drain nickel silicidation process. Furthermore, we performed TCAD device simulations to demonstrate explicitly the advantages of $NiSi_2$ formation through PLA annealing.

Experimental

A 6-inch (100) p-type wafers (resistivity: 15–25 Ω cm) were cleaned in hydrofluoric acid for 3 min and then rinsed with de-ionized water prior to nickel deposition. An inductively coupled plasma (ICP) pre-sputter was applied (10 s) to remove the native oxide from the surface. Ni (15 nm) and Ti (10 nm) were deposited sequentially using a physical vapor deposition (PVD) system. This Ti was used as a capping layer to avoid oxygen contamination during silicidation.[12] For silicidation through thermal annealing, RTA was performed using an AG Heat Pulse 610 and PLA was performed using a 355 nm wavelength Quanta-Ray Pulsed Nd:YAG laser. Blank wafer strain was measured using a Tencor FLX-2320 strain measurement instrument. The two-step silicide annealing process employed in this work commenced with a RTA first annealing process, followed by removal of unreacted nickel and titanium metal by immersion in H_2SO_4 and H_2O_2 solution (4:1), and then performed the second annealing process. After performing silicidation, the sheet resistances of the samples were measured using a four-point probe; a blank wafer strain was determined by measuring changes in the substrate curvature radius. All electrical data were measured using an HP4156 precision semiconductor parameter analysis probe.

Schottky diode fabrication.— After defining the active area of diode, a 550 nm-thick SiO_2 layer was grown using wet oxidation at 980°C for local oxidation of silicon (LOCOS) isolation. A 925°C, 35-nm thermal oxide was grown as sacrificial layer. Next, a field implantation with BF_2 at 90 keV and a dose of 1×10^{13} cm^{-2} was followed to ensured an acceptable field threshold for the p-type substrate. All samples were then annealed in a furnace (1100°C, 10 min) to activate the dopant and recover lattice damage and then subjected to pad oxide removal through an HF dip. Finally, the various nickel silicide annealing processes were employed to investigate the effect of PLA silicidation on the characteristics of the Schottky diode.

nMOSFET device fabrication.— After the LOCOS isolation was performed and followed by threshold voltage (V_{th}) implantation using BF_2 at 90 keV and a dose of 1×10^{13} cm^{-2}, The 800°C, 3-nm pure thermal oxide layer was grown in furnace as gate dielectric. The 620°C, 120-nm poly-Si layer was deposited sequentially in a low-pressure chemical vapor-deposition (LPCVD) system as gate material. A 700°C, 50-nm tetraethyl orthosilicate (TEOS) capping oxide layer was deposited as a etching hard mask for following gate electrode patterning. The poly-Si gate was patterned using an I-line stepper and trimmed to 130 nm using a photoresister and the "ashing and etching" approach, followed by 5-nm poly-Si re-oxidation as an offset spacer in a furnace. BF_2 was used for 30° tilted-angle halo implantation at 50 keV and a dose of 3×10^{13} cm^{-2}. Arsenic implantation was carried out at an energy of 7 keV and at a dose of 1×10^{15} cm^{-2} for the lightly doped drain (LDD). The

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deposition of 100-nm-thick SiN using SiH_2Cl_2 and NH_3 at 780°C in a LPCVD was performed and then followed by the anisotropic etching for spacer formation. The TEOS etching hard mask was then removed through HF dipping to ensure that the SiN spacer height was not less than the poly-Si gate height to protect the poly-Si from melting during the PLA process. The wafers then underwent deep source/drain implantation using arsenic at an energy of 20 keV and a dose of 5×10^{15} cm^{-2}. After exposing the wafers to RTA (1000°C, 10 s) to activate the dopant, the two different silicidation processes were compared for their effects on performance. Plasma-enhanced chemical vapor deposition (PECVD) was used to deposite a 400-nm TEOS layer for inter-metal layer. Finally, the contact hole etching process and physical vapor deposition (PVD) of Al were sequentially performed for contact and electrode pad formation.

Results and Discussion

$NiSi_x$ film and Schottky diode characterization.— Figure 1 shows the two silicide annealing processes. In the flow-1 method, we used conventional two-step RTA with conditions of 350°C/15 s and 400°C/30 s for the first and second annealing steps, respectively. In the flow-2 approach, a PLA process replaced the second RTA step. From a previous literature, Alberti et al. found that nickel profile in the silicon layer plays a crucial role to activate the Si crystallization during excimer laser annealing.[13] In this work, the flow-2 employed a conventional RTA prior to the PLA to distribute nickel atoms within the desired silicidation depth, which is beneficial to improve the crystalline characteristic of silicide and its interface to the underneath silicon. To study the interactions between Ni and Si atoms during PLA heating, we also prepared a PLA-first annealing sample using a laser energy of 0.6 J cm^{-2} for comparison. Figure 2 presents a correlation chart of blanket-wafer silicide-film stress differences against sheet resistance. The stress difference was taken obtained by subtracting the stress results measured after the initial RTA process and again after completion of the second annealing process. The significant increase in sheet resistance for the PLA-first sample was due to the formation of ultra-thin (10 nm) silicide, as determined using transmission electron microscopy (TEM). The Energy dispersive X-ray spectroscopy (EDS) revealed that the composition of the thin silicide was $NiSi_2$; therefore, the 0.6 J cm^{-2} PLA energy was sufficient to activate the Ni for its reaction with Si. Though the resulting thin silicide is favorable for an ultra-shallow junction, it featured the $NiSi_2$ (111) facet; therefore, this process required further optimization. Upon increasing the laser energy density, the flow-2 process resulted in significant increases in tensile stress and silicide sheet resistance, suggesting that PLA offers a sufficient energy to transform the Ni-rich silicide into $NiSi_2$. However, when the PLA energy density was increased to 2.3 J cm^{-2}, either $NiSi_2$ agglomeration or Si

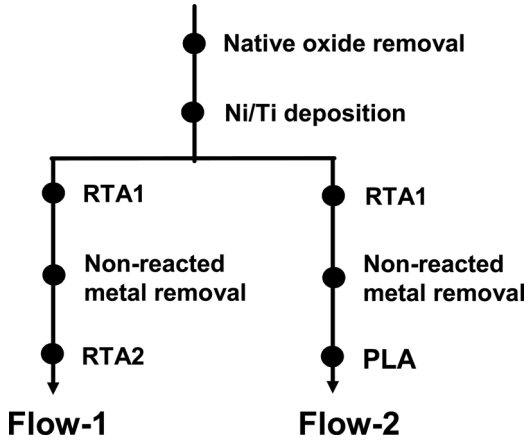

Figure 1. Flow chart of the two different annealing processes used for silicidation.

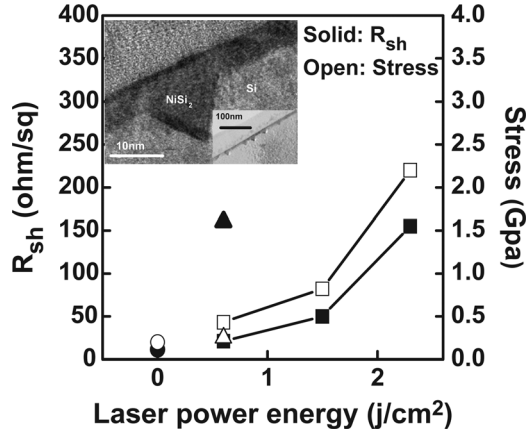

Figure 2. Correlation between the blanket-wafer silicide-film stress differences and sheet resistance. Circles: flow-1 sample; triangles: PLA-first sample; squares: flow-2 sample prepared at various laser powers. Inset: TEM image of the PLA-first sample, revealing a thin silicide layer.

precipitation occurred, leading to an abrupt increase in sheet resistance.[14] Figure 3 shows the grazing incidence X-ray diffraction (GIXRD) spectrum investigation of the various silicidation processes. For the sample employed the two-step RTA annealing process, the spectrum shows that inhomogeneous Ni silicide phases including Ni_2Si and NiSi were appeared. On the other hand, for the flow-2 sample which replaced the second RTA step with PLA, the peak intensity of the signal associated with $NiSi_2$ increased, whereas those of the Ni-rich silicide phases gradually diminished. This result reveals that PLA is conducive to phase nucleation of Ni-rich silicides formed after the initial RTA stage, with the $NiSi_2$ phase appearing after PLA treatment. A sufficient PLA energy density would induce melting of the nickel silicide, with the melt front propagating down to the silicide/Si interface. When the melt front reached the Si substrate, mixing of the silicide and Si occurred and Si-rich nickel silicide having smooth morphology was formed at near the silicide/Si interface.[14,15] In the case of bulk silicide region, excess free energy existed in the polycrystalline nickel silicide region, leading to phase nucleation during the silicide melting process.[16] According to the previous literature, the threshold energy required to melt and solidify $NiSi_2$ is ca. 1.1 J cm^{-2}.[15] In this work, a higher laser energy might be necessary to melt Ni-rich compounds to form a homogeneous silicide phase due to the melting temperature of Ni_2Si (1310°C) is higher than NiSi (980°C) and $NiSi_2$ (993°C).[11] However, it is worth noting that $NiSi_2$ (111) phase spectrum peak shifted to ca. 28.85° at

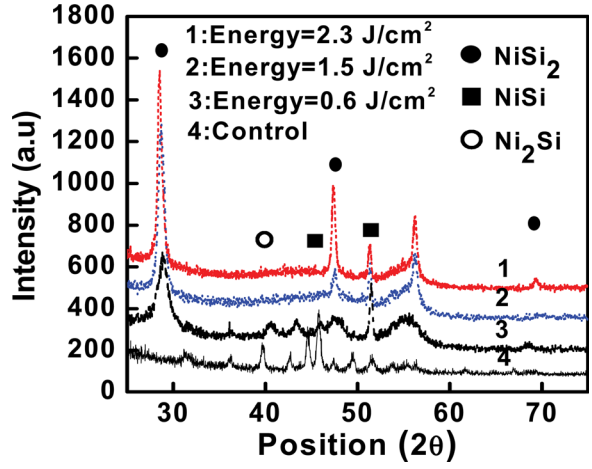

Figure 3. (Color online) GIXRD spectra of samples prepared under various silicidation conditions.

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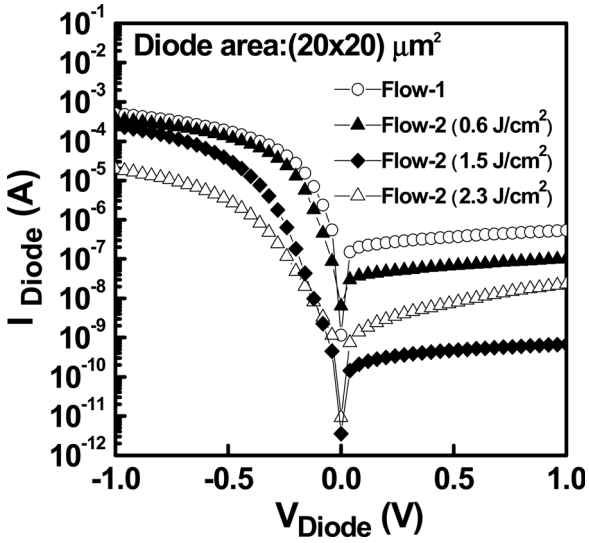

Figure 4. Characteristics of p-type Schottky diodes formed under various silicide annealing conditions. The deduced hole SBH/ideal factor is 0.52 eV/n = 1.6 for flow-1 sample and 0.68 eV/n = 1.28 for flow-2 sample.

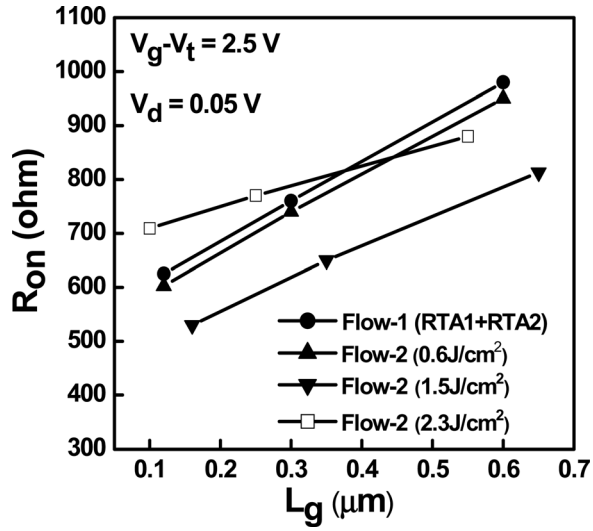

Figure 6. R_{on}–L_g plots of nMOSFET devices prepared under various annealing conditions.

2.3 J cm^{-2} PLA energy densities, indicating that excessive PLA energy density resulted in Si precipitation during solidification and caused the high sheet resistance. Figure 4 shows the p-type Schottky diodes (area: 4×10^{-6} cm^2) *I–V* characteristics comparison between flow-1 and flow-2 samples. The ideal factor of diode was deduced for each sample by linear fitting of the forward-biased *I–V* characteristic based on a thermal emission model at room temperature[17]

$$J = A^* T^2 \left[\exp\left(-\frac{q\phi_b}{kT}\right)\right]\left[\exp\left(-\frac{qV}{nkT}\right) - 1\right]$$

where A^* is the Richardson constant ($A^* = 32$ A cm^{-2} K^{-2}). Based on the *I–V* characteristics, preparing the nickel silicide at 0.6 J cm^{-2} energy densities produced non-uniform $NiSi_2$ layers at the interface; therefore, the PLA effect on silicide SBH modification was insignificant. When we further increased the PLA energy density to 1.5 J cm^{-2}, both the forward and reverse *I–V* characteristics indicated that silicide SBH was modified. The diode exhibited an improved ideality factor ($n = 1.28$) and the extracted SBH ($\Phi_{bo} = 0.68$ eV) was close to the reported value for $NiSi_2$[4] compared to the sample treated with conventional two-step RTA annealing (ideality factor $n = 1.28$ and extracted $\Phi_{bo} = 0.52$ eV). The observed hole barrier height increased from 0.52 to 0.68 eV suggests that the Fermi-level of silicide is shifted from the mid-gap to a level close to the conduction band of silicon due to $NiSi_2$ formation, reducing the barrier height of the electron. The PLA with a sufficient laser energy density improves the silicide phase homogeneity and flatness of $NiSi_2$ at silicide/Si interface. Hence, it could modify the silicide/Si interface structure, including improving the interface state density and modifying the SBH.[17] In the conventional MOSFET, the low SBH silicide is desired to connect to a heavy doped source/drain region for parasitic resistance reduction. The heavy doped region creates a narrow depletion region at the silicide/silicon interface and in addition, the low SBH enhances the carrier tunneling probability thus the so-called specific resistance is reduced.[18] According to the study using the theoretical field emission model and considering the dopant concentration effect, a 0.2 eV SBH reduction will lead to a decrease of approximately one third in the specific resistance observed for a heavily doped source/drain.[19] Further increases in the PLA energy density, however, degraded the reverse bias leakage and led to decline in the diode saturation current and ideality. The agglomeration of $NiSi_2$, the destroyed silicide/Si interface morphology and precipitation of Si due to the interdiffusion of excess Si from substrate to silicide led to a high sheet resistance and affected the diode ideality. Figure 5 displays TEM images of materials produced under the different silicide annealing conditions. Figure 5b shows that PLA samples produced under a laser energy density of 0.6 J cm^{-2} featured smooth silicide/Si interfaces with facetless texture of $NiSi_2$ at the interface. However, increasing the PLA energy density to 2.3 J cm^{-2} caused a Si-rich ($Ni_{0.23}Si_{0.77}$) nickel silicide formation, destroying the interface flatness which was shown in Fig. 5c. Unlike other recently reported techniques for $NiSi_2$ formation,[4] this approach generates facetless $NiSi_2$ at the silicide/Si interface, thereby reducing the likelihood of facet-induced junction leakage. To further achieve the lowest total resistance and improved thermal stability, the optimal PLA energy density should be chosen to balance the needs of sheet resistance and silicide/silicon interfacial resistance.

nMOSFET characteristics and TCAD evaluation.— We employed a total resistance slope-based approach [20] to evaluate the effect of the laser energy density on the silicidation effect of the S/D

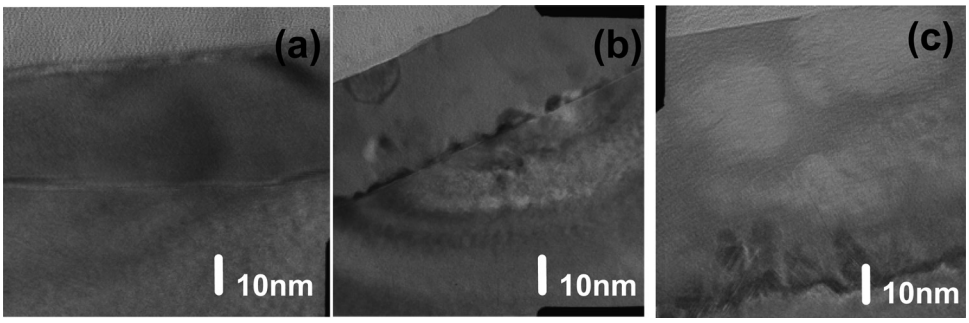

Figure 5. Cross-sectional TEM images of the (a) flow-1 sample, (b) flow-2 sample prepared under a laser energy density of 0.6 J cm^{-2}, and (c) flow-2 sample prepared under a laser energy density of 2.3 J cm^{-2}.

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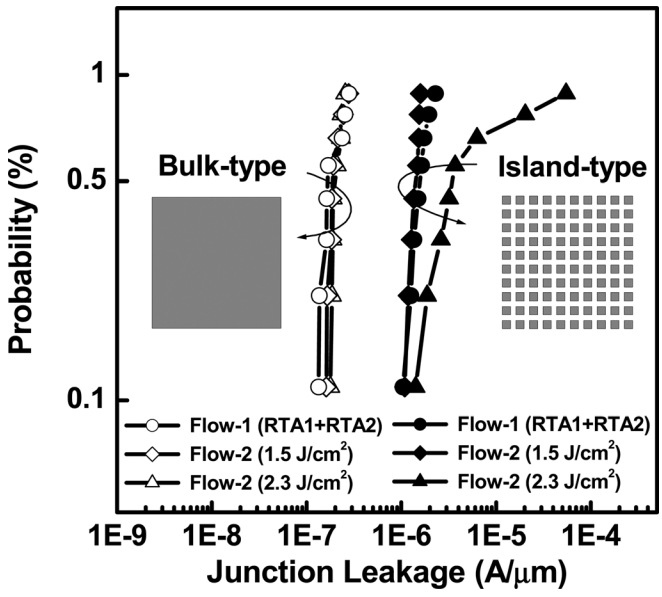

Figure 7. The N^+/P-well statistics junction leakage distribution of different silicidation splits. The dimension for the bulk-type junction structure is 100×100 μm. For the island-type junction structure, a 10×10 array of 10×10 μm active area is used.

series resistance R_{sd} and on the carrier mobility of nMOSFET. We used scanning electron microscopy (SEM; top-view measurement) to calibrate the device's gate length, and used a constant gate overdrive voltage ($V_g - V_t$) of 2.5 V and a value of V_d of 0.5 V in the calculation of the total resistance. Figure 6 presents the $R_{on}-L_g$ characteristics of the devices prepared under various PLA energy densities. Relative to the two-step RTA control wafer, employing the PLA at a specific laser energy range (from 0.6 to 1.5 J cm^{-2}) exhibited a beneficial effect on the value of R_{sd}. We hypothesize that $NiSi_2$, initially formed in the silicide/Si interfacial region, modified the electron SBH. When the laser energy density further increased to 1.5 J cm^{-2}, the $NiSi_2$ crystalline quality and the silicide/Si interface structure were improved hence a minimum total resistance was achieved. In addition, the change in the slope of the $R_{on}-L_g$ plot indicates that the devices benefited from strain effect due to $NiSi_2$ formation. Although high PLA energy density improved the strain strength, it also destroyed the morphology of the silicide and led to agglomeration of $NiSi_2$, resulting in high silicide resistance and increased leakage. Figure 7 shows the silicided N+/P-well junction leakage characteristics. A 10×10 array of square active area (each active area is 20×20 μm) and a bulky active area (active area is 100×100 μm) were employed as monitor structure. From the result, the samples treated by PLA with an energy density of 1.5 J cm^{-2} exhibit tighter junction leakage distribution than the samples treated by the two-step RTA. However, when samples treated by PLA with a 2.3 J cm^{-2} energy density, both the leakage distribution and the leakage current level are degraded due to silicide morphology destruction especially at a periphery-intensive structure. The thermal profile difference and nonuniform topography along the Si to LOCOS interface can affect the silicide morphology and cause severe junction leakage. Consequently, there is no benefit in performance after increasing the PLA power beyond a critical threshold. Figure 8a compares the $I_{on}-I_{off}$ gains for short-channel MOSFET devices. Adopting the PLA for silicidation with a laser energy density of 1.5 J cm^{-2} provided an 8% $I_{on}-I_{off}$ gain over the two-step RTA treated wafer. The inspection of I_d-V_g characteristics in Fig. 8b reveals that saturation current and off-state current were both improved for the PLA devices. To investigate the causes of device performance gain,the device cross-sectional TEM images of the various silicidation processes were compared which is shown in Fig.9. Unlike the two-step RTA-devices, using flow-2 for silicidation at a laser energy density of 1.5 J cm^{-2} produced a flat silicide interface and self-organized (111) $NiSi_2$ orientation appeared beneath the spacer. The shape of silicide beneath the spacer are affected by the spacer profile as well as the thermal profile difference between the exposed source/drain active area and the region covered by gate/spacer to form the self-organized (111) orientation of $NiSi_2$. This self-organized (111) $NiSi_2$ were previous demonstrated to improve the short channel effect due to the trapezoidal shape channel formation.[21] To further investigate the effect of silicide proximity on device performance, we used the TCAD simulation templates (with TSUPREM and MEDICI) for silicide stress and performance evaluation. The MEDICI templates provide the linear region I_{ds} current gain from resistance reduction and ignore the effect of mobility enhancement from the strain. The TSUPREM process simulation results in Fig. 10 reveal that the enhancement in strain strength of device was significant by reducing the spacer width prior to silicidation (silicide proximity). In contrast, excessive reduction of the silicide-to-channel proximity severely impaired device performance due to the current crowding effect, cancelling the gain in mobility. Accordingly, a specific silicide thickness, silicide shape, and silicide-to-channel proximity all

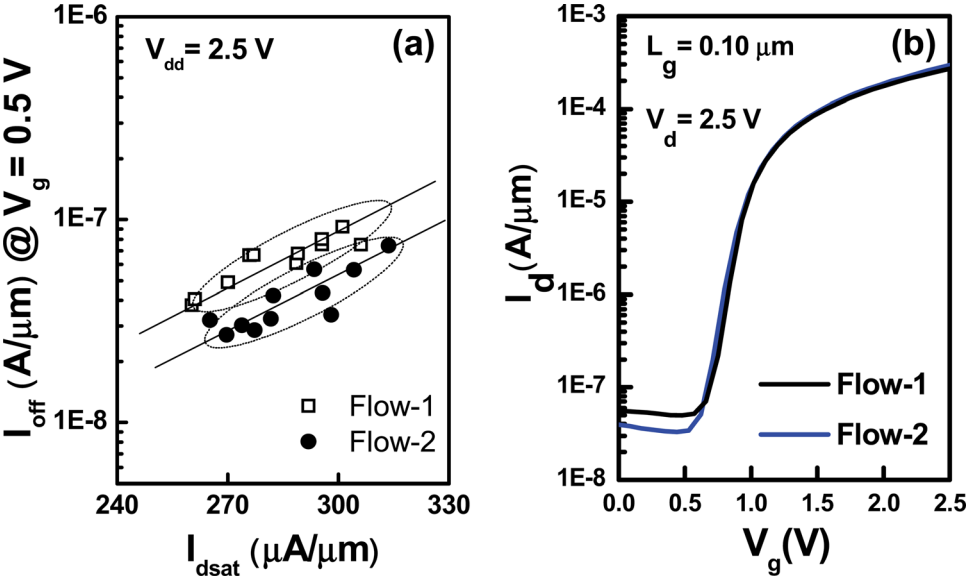

Figure 8. (Color online) (a) $I_{on}-I_{off}$ characteristics of the flow-1 (RTA1 + RTA2) and PLA (energy density: 1.5 J cm^{-2}) devices. (a) I_d-V_g characteristics of the flow-1 (RTA1 + RTA2) and PLA (energy density: 1.5 J cm^{-2}) samples.

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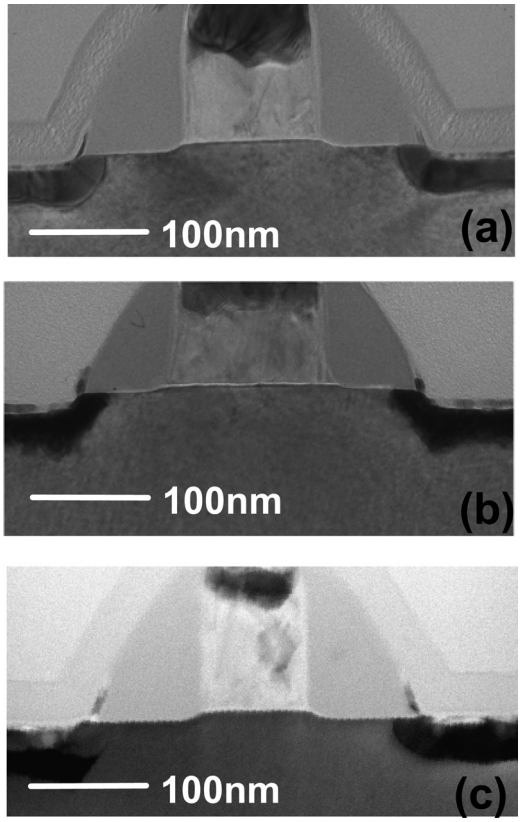

Figure 9. TEM cross-sectional images of the (a) flow-1 sample, (b) flow-2 sample prepared under a laser energy density of 1.5 J cm^{-2}, and (c) flow-2 sample prepared under a laser energy density of 2.3 J cm^{-2}.

provide the benefits of silicide strain without suffering from current crowding penalties. When we factor the self-organized (111) silicide shape of the PLA sample into the TCAD templates, two major effects that help alleviate the performance penalty that arises from reduction in the silicide-to-channel proximity were observed including: (i) a current crowding effect, illustrated in Figs. 11a and 11b,

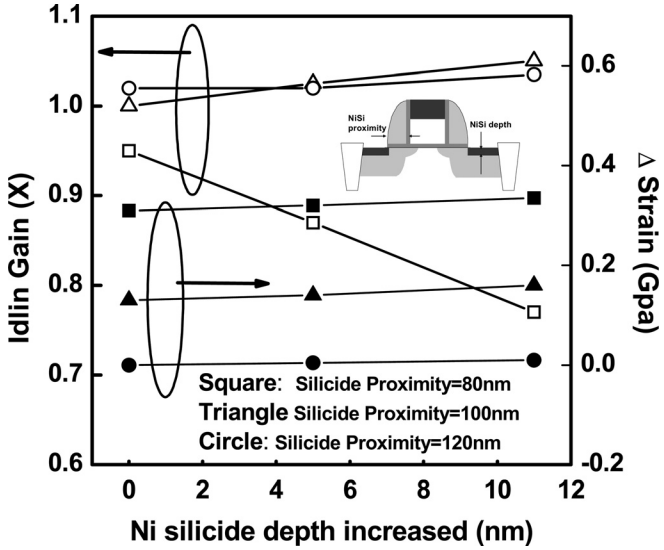

Figure 10. Simulated influence of silicide-to-channel proximity on the values of I_{d-lin} gain and channel strain. Nickel silicide strain:0.7 Gpa; initial thickness:15 nm.

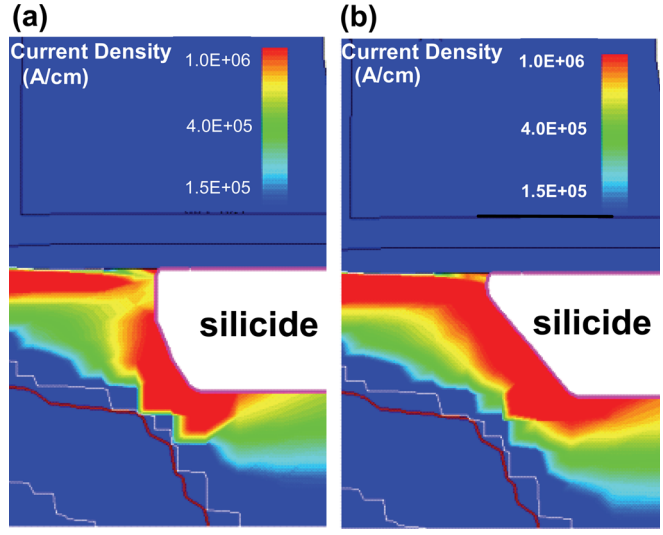

Figure 11. (Color online) TCAD device simulation diagrams. (a) Current crowding effects of the thicker and laterally encroached silicide. (b) Self-organized (111} silicide profile conducive to alleviating the current crowding effect.

and (ii) a decrease in silicide/Si interfacial resistance resulting from a decrease in the SBH. Furthermore, the distance from the silicide to the depletion region in LDD region was larger for the PLA sample, thereby reducing the non–V_g-dependent I_{off} current due to the junction spiking, as revealed in the simulation results in Figs. 12a and 12b. The TCAD simulation results were conform with experimental data and they also clarify the benefit of this self-organized (111) $NiSi_2$ in a MOSFET structure. Despite the benefits gained from strain may decrease as silicide thickness decreases; the improved silicide morphology and intrinsic silicide strain enhancement attained would be beneficial for a significant reduction in the silicide-to-channel proximity. Using PLA for the silicidation process, therefore, reduces shallow junction leakage and increases nMOSFET strain relative to those of conventional annealing processes. Although high PLA energy density might accompany with the integration concern such as poly-Si melting and gate dielectric defect

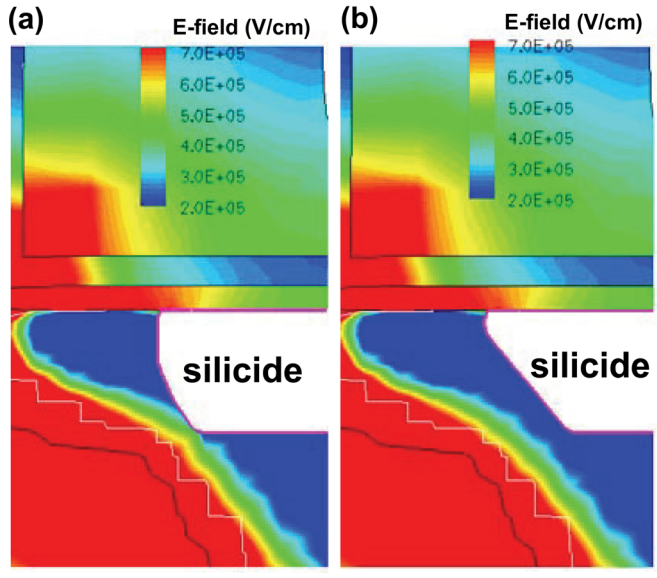

Figure 12. (Color online) TCAD device simulation diagrams. (a) Device electric field at the LDD region, under "off"-state operation conditions, for the thicker and laterally encroached silicide. (b) The device electric field for the self-organized (111) silicide.

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issue were disclosed with current device scheme, the integration concerns might be excluded when the device process flow is changed from "gate-first" process to a "gate-last" process.[22] Notably, the pattern geometry effect of PLA can be alleviated by using a longer-wavelength laser or by inserting an absorption layer to improve the device's uniformity and fluctuation.[23,24]

Conclusion

We demonstrate the modification of nickel silicide SBH and tensile strain achieved through a two-step annealing that combines conventional rapid thermal annealing (RTA) with pulsed laser annealing (PLA) for silicidation. At the laser energy density of 1.5 J cm^{-2}, smooth $NiSi_2$ was formed at the silicide/Si interface on a (100) substrate, reducing the possibility of (111) facet induction and junction leakage. The PLA method improves the silicide phase homogeneity and flatness at silicide/Si interface, introducing a 0.16 eV hole SBH increase compared to the conventional two-step RTA annealing on the p-type Schottky diodes. For device application, the PLA method produced an 8% gain in the nMOSFET's $I_{on} - I_{off}$ characteristics due to the silicide/n^+-Si interfacial resistance, carrier mobility and junction leakage improvement under the laser energy density of 1.5 J cm^{-2}. In addition, the self-organized (111) shape of $NiSi_2$ silicide formation by PLA near the LDD region exhibited a reduced silicide-to-channel proximity; with accommodation for additional current crowding and junction leakage. This method holds promise for replacing current nickel silicide annealing approaches for future applications of extremely scaled-down transistors.

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