A Sub-10-μW Digitally Controlled Oscillator Based on Hysteresis Delay Cell Topologies for WBAN Applications

Shu-Yu Hsu, Jui-Yuan Yu, and Chen-Yi Lee

***Abstract*—This brief presents an all digitally controlled oscillator (DCO) design with two newly proposed hysteresis delay cells (HDCs) for wireless body area network applications. According to circuit topologies, the two HDCs are defined as on–off and cascaded HDCs that provide various propagation delay values. These HDCs form a simple oscillator structure based on a power-of-2 delay stage DCO (P2-DCO) architecture. Each delay stage provides half of the delay of the previous delay stage in descending order, enabling low-power and small-area features. The P2-DCO is verified in a 90-nm CMOS technology for wide operating frequencies with area of 80 μm $\times$ 80 μm and least significant bit resolution of 2.05 ps. With a supply voltage of 1.0 V, the measured dynamic power values are 5.4 and 166 μW at 3.4 and 163.2 MHz, respectively.**

***Index Terms*—Digitally controlled oscillator (DCO), hysteresis delay cell (HDC).**

I. Introduction

RAPID wakeup time reduces wasted system power during the settling period, particularly for low-power and low-system duty-cycle applications. The wireless personal area network [1] and wireless body area network (WBAN) [2] applications typically perform a system duty $< 1\%$ that requires fast wakeup for burst data transmission and goes to sleep right away for best power savings. Accordingly, the settling time of a clock generator or a phase-locked loop (PLL) that determines the time from system sleeping to the active state becomes a critical parameter in system power optimization.

The reference frequency f_{REF} to a PLL, however, is a tradeoff between its settling time and system power reduction. A tens-of-kilohertz quartz crystal as a frequency reference may result in 100 μs to even 1 ms to enable the system from sleeping to operation [1], [12], which can be equal to the duration of a system's active period. This problem can be solved by using a megahertz-scale frequency f_{REF}, because the settling time is inversely proportional to f_{REF} [12]. Although higher f_{REF} effectively reduces the settling time, this frequency reference leads to increased and continuous operation power, even in the sleeping state.

Accordingly, this brief is to develop a digitally controlled oscillator (DCO) in a megahertz-scale frequency (e.g., 5 MHz) with sub-10 μW that minimizes both the system sleeping power by a low-power clock source and the system wakeup power by the reduced settling time.

The DCO, which is widely applied for all-digital clock generation and frequency synthesis [3]–[5], has become an appropriate clock source for low-power and highly integrated WBAN applications [2]. Instead of the utilization of a conventional voltage-controlled oscillator, the DCO possesses the merits of easier porting between different process and voltage scaling with a lower supply voltage. Meanwhile, the all-digital approach minimizes the test, control, and integration efforts. Nevertheless, the DCO power dissipation with a megahertz-scale frequency is still the major bottleneck.

There have been several DCO architectures proposed in the literature. The LC-tank DCO achieves excellent phase noise performance, whereas the wireless sensor node often relaxes the phase noise requirement for more power reduction [14]. The current-starved DCO [6] provides fine delay resolution but features high static power consumption. The standard-cell-based DCO [2], [5] with straightforward delay elements, buffer/inverters, or or-and-inverter logic cells presents high power and poor linearity with insufficient delay resolution. The digitally controlled varactor [7] improves delay resolution but with similar power scale. Therefore, a hysteresis delay cell (HDC) [8] was first proposed for trading off between power and delay resolution. This HDC consists of several standard cells with delay range as multiple inverters, but the resulting power saving is still limited. In addition, all the aforementioned DCOs consume more than 100 μW power, resulting in higher system sleeping power and confining use to low-power WBAN applications.

Consequently, this brief presents two novel HDC circuit topologies (on–off and cascade) and a power-of-2 delay stage DCO (P2-DCO) architecture for power-restricted WBAN applications. Both features possess high power and area efficiency and accordingly overcome the challenge in DCO power reduction, particularly in a sub-10-MHz design.

This brief is organized as follows. Section II gives an overview of the proposed DCO design. Section III presents the proposed HDC cells designed for coarse- and fine-tuning stages. Section IV shows the experimental results and comparisons. Finally, Section V concludes the results.

Manuscript received June 11, 2010; revised August 22, 2010; accepted October 11, 2010. Date of publication December 3, 2010; date of current version December 15, 2010. This work was supported in part by the Ministry of Economic Affairs of Taiwan under Grant 97-EC-17-A-03-S1-005. This paper was recommended by Associate Editor P.-I. Mak.

The authors are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: fishya@si2lab.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2010.2087991

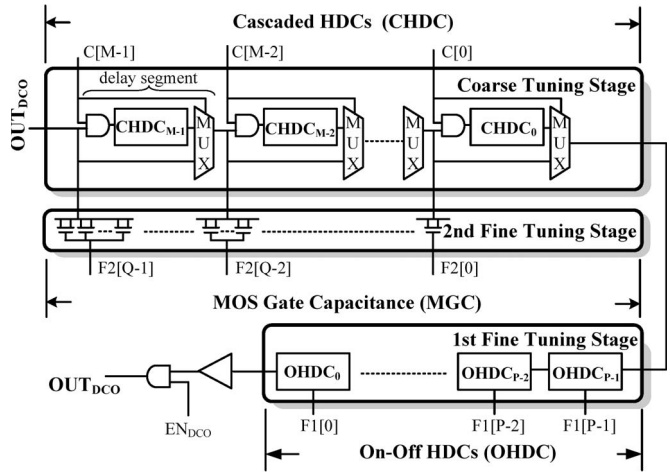

Fig. 1. P2-DCO architecture.

II. DCO Architecture

A. Overview

Fig. 1 illustrates the architecture of the proposed P2-DCO, which includes one coarse-tuning stage and two fine-tuning stages. In each tuning stage, the delay segment is designed in power-of-2 descending order. Therefore, each delay segment generates half of the delay of the previous delay segment. This power-of-2 approach is modeled as

$$\text{Delay}_k = 2 \cdot \text{Delay}_{k-1} \tag{1}$$

where Delay_k is the propagation delay of the kth delay segment within a tuning stage. Moreover, this architecture exempts the need for an additional codeword decoder, which is conventional in the state-of-the-art DCO designs.

The coarse-tuning stage and the first fine-tuning stage are cascaded together based on the ring oscillator structure, whereas the second fine-tuning stage is appended to delay segments' inputs in the coarse-tuning stage. The cascaded HDC (CHDC) and the on–off HDC (OHDC) are utilized in the coarse-tuning stage and the first fine-tuning stage, respectively. Furthermore, in the second fine-tuning stage, the MOS gate capacitance (MGC) is applied for further fine-tuning.

B. Coarse-Tuning Stage

The coarse-tuning stage defines the DCO operation range with multiple delay segments. Each segment comprises CHDCs for delay purposes and the multiplexers for signal propagation path selection. The power-of-2 behavior is accomplished by cascading CHDCs in different numbers or using CHDCs with different delay values. Furthermore, AND gates are used for CHDC input isolation when the CHDC is not in the signal propagation path. Consequently, the redundant power dissipation can be effectively cut down through this isolation.

C. Fine-Tuning Stage

The fine-tuning stage is applied for DCO resolution enhancement. In order to achieve finer resolution, AND gates and multiplexers are eliminated in the first fine-tuning stage. Instead, two topologies of OHDCs with switch capability are performed as the delay elements.

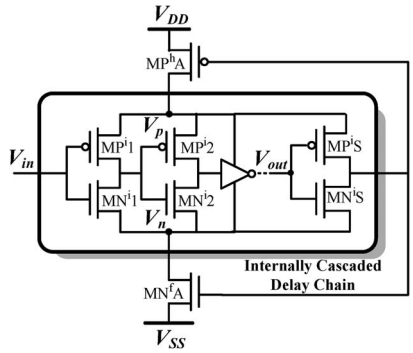

Fig. 2. CHDC.

The second fine-tuning stage utilizes the MGC to generate a picosecond-scale delay from a variant combination of output capacitance loading. The gate capacitance is also arranged in a power-of-2 order by increasing the transistor gate width or combining transistors in multiple.

III. Proposed HDCs

The Boolean function of HDCs is the same as that of a normal inverter, except that HDCs have the hysteresis property. This hysteresis phenomenon induced by a Schmitt trigger has been discussed for low-power operations [9], [10]. Based on the basic structure, this brief further utilizes the low-power property and proposes two HDC topologies to get higher power efficiency and a wide delay range for DCO design.

A. CHDC

The CHDC provides a delay that is tens of times larger than the delay of a minimum-sized inverter in the same manufacturing technology. Meanwhile, a large short current is avoided for low-power purposes.

A general form of the CHDC can be regarded as a chain of internal inverters with a header, a footer transistor, and feedback connections, as shown in Fig. 2. This combination results in a hysteresis effect that the header and the footer are barely turned on at the same time. Because of the hysteresis phenomena, the internal voltages V_p and V_n are deduced from [9]

$$\begin{cases} V_n|_{\text{MP}^h\text{A=ON}} = [V_{\text{in}} + V_{\text{tn}} \cdot (R_n - 1) + V_{\text{SS}} \cdot R_n] / (R_n + 1) \\ V_p|_{\text{MN}^f\text{A=ON}} = [V_{\text{in}} - |V_{\text{tp}}| \cdot (R_p - 1) + V_{DD} \cdot R_p] / (R_p + 1) \end{cases} \tag{2}$$

where $R_n = (\beta_{\text{MN}^f\text{A}}/\beta_{\text{MN}^i1})^{1/2}$, and $R_p = (\beta_{\text{MP}^h\text{A}}/\beta_{\text{MP}^i1})^{1/2}$, with the transconductance β. V_{tn} and V_{tp} denote the NMOS and PMOS threshold voltages. In addition, V_p and V_n are equal to V_{DD} and V_{SS} when MP^{h}A and MN^{f}A are turned on in the linear region, respectively. As a result, voltage scaling is equivalently applied on the internal inverter chain with a lower experienced supply voltage $V'_{DD}|_{\text{MP}^h\text{A=ON}} = V_{DD} - V_n$ or $V'_{DD}|_{\text{MN}^f\text{A=ON}} = V_p - V_{\text{SS}}$. This voltage scaling not only reduces power consumption but also contributes to a longer propagation delay. The average propagation delay t_D with a lower experienced supply voltage, therefore, can be approximated to

$$t_D \approx \sum_{r=1}^{S} \frac{C_L}{2V'_{DD}} \left(\frac{1}{\beta_{\text{MP}^i r}} + \frac{1}{\beta_{\text{MN}^i r}} \right) \tag{3}$$

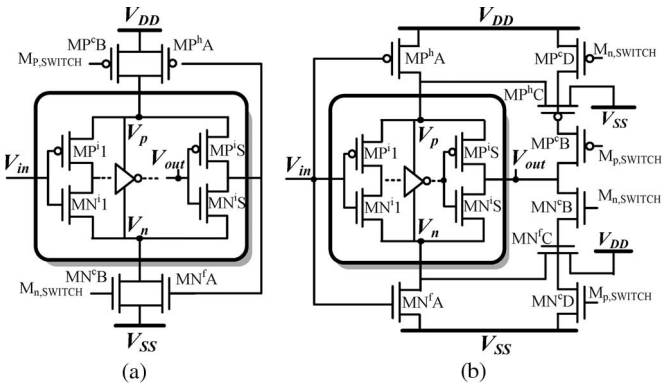

Fig. 3. (a) OHDC-LD. (b) OHDC-SD.

where r, S, and C_L are the index, total number, and output loading of inverters within the internal inverter chain, respectively. Because of lower V'_{DD} induced by the hysteresis phenomenon, a sufficient long delay is generated with a constrained low short-circuit current.

B. OHDC

The OHDC generates a delay resolution that is several times the delay of a minimum-sized inverter. In addition, the OHDCs with hysteresis on–off switch capability eliminate the use of path-selection elements and perform a tradeoff between power and resolution.

Fig. 3 illustrates two general forms of the OHDC, which are the long-delay OHDC (OHDC-LD) and the short-delay OHDC (OHDC-SD) with different delay ranges. By adding two controlling transistors MP^{c}B and MN^{c}B, the OHDC can be switched as a normal inverter chain or a hysteresis delay chain. Therefore, the OHDC generates finer resolution from the delay difference between these two modes and benefits from the power reduction in the hysteresis mode.

Both OHDCs operate as normal inverter chains with a similar propagation delay value when controlling transistors MP^{c}B and MN^{c}B are turned on. Meanwhile, this higher internal voltage implies that V_p and V_n are close to V_{DD} and $V_{\rm SS}$, respectively. On the other hand, the OHDCs remain as Schmitt triggers while the transistors MP^{c}B and MN^{c}B are off. The internal voltages V_p and V_n of the OHDC-LD can be found in (2); in addition, V_p and V_n of the OHDC-SD are expressed as [10]

$$\begin{cases} V_n|_{\mathrm{MP}^h\mathrm{A=ON}} \\ \quad = V_{DD} - V_{\rm tn} - R'_n(V_{\rm in} - V_{\rm SS} - V_{\rm tn}), \quad V_p|_{\mathrm{MP}^h\mathrm{A=ON}} \approx V_{DD} \\ V_p|_{\mathrm{MN}^f\mathrm{A=ON}} \\ \quad = R'_p(V_{DD} + V_{\rm tp} - V_{\rm in}) + (V_{\rm SS} - V_{\rm tp}), V_n|_{\mathrm{MN}^f\mathrm{A=ON}} \approx V_{\rm SS} \end{cases} \tag{4}$$

where $R'_n = (\beta_{\mathrm{MN}^f\mathrm{A}}/\beta_{\mathrm{MN}^f\mathrm{C}})^{1/2}$, and $R'_p = (\beta_{\mathrm{MP}^h\mathrm{A}}/\beta_{\mathrm{MP}^h\mathrm{C}})^{1/2}$. This produces a smaller propagation delay than the delay of the OHDC-LD. Furthermore, the additional transistors MP^{c}D and MN^{c}D prevent the potential short current paths and balance the rise and fall time currents, resulting in improved jitter performance.

Consequently, the delay resolution of both OHDCs is equal to the delay difference $t_{\rm Diff}$ between the ON- and OFF- states

TABLE I
SIMULATION SUMMARIES OF DELAY CELLS

Tuning Stage	Cell Name	Cell Delay (ns)	Power (μW)	Normalized Power
Coarse tuning	AND[8]	0.052	103.93	100%
	$CHDC_2$	2.078	10.49	10%
	$CHDC_1$	1.040	15.93	15%
	$CHDC_0$	0.522	21.94	21%
1st fine tuning	HDC[8]	0.083	151.5	100%
	$OHDC\text{-}LD_1$	0.171	43.19	29%
	$OHDC\text{-}LD_0$	0.086	62.47	41%
	$OHDC\text{-}SD_1$	0.065	53.93	36%
	$OHDC\text{-}SD_0$	0.033	98.80	65%
2nd fine tuning	DCV-LD[8]	0.738ps	153.95	100%
	DCV-SD[8]	0.619ps	159.95	104%
	MGC	1.02ps	137.02	89%

and can be approximated to

$$t_{\rm Diff} \approx \sum_{r=1}^{S} \frac{C_L}{2}\left(\frac{1}{\beta_{\mathrm{MP}^i r}} + \frac{1}{\beta_{\mathrm{MN}^i r}}\right)\left(\frac{1}{V'_{DD}} - \frac{1}{V_{DD} - V_{\rm SS}}\right) \tag{5}$$

where V'_{DD} and $V_{DD} - V_{\rm SS}$ are the experienced supply voltages in the hysteresis and normal inverter modes, respectively. As a result, the OHDC provides finer delay resolution than (3) that the hysteresis cell is simply used as a delay element.

IV. EXPERIMENTAL RESULTS AND COMPARISON

The proposed P2-DCO with novel HDCs is evaluated and fabricated in a 90-nm 1-poly 9-metal CMOS technology. The published approaches are also rebuilt in the same technology for performance comparison.

The P2-DCO power performance can be analyzed by the power and delay characteristics of delay cells. The output period T is synthesized by the turned-on delay cells, which implies that the DCO dynamic power $P_{d,\rm DCO}$ is proportional to the total consumed energy within the used delay cells $\sum(D_k \cdot P_{d,k})$ divided by the total delay $\sum D_k$. A general expression is given by

$$P_{d,\rm DCO} \propto \frac{\sum\limits_k (D_k \cdot P_{d,k})}{\sum\limits_k D_k} = \frac{\sum\limits_k (D_k \cdot P_{d,k})}{T/2} = 2\sum_k (R_k \cdot P_{d,k}) \tag{6}$$

where the delay ratio $R_k = D_k/T$. Note that $P_{d,\rm DCO}$ is not a function of its operating frequency because only part of cells in the delay chain are activated to accumulate the required delay value. Thus, Table I further summarizes the HDCs in this design based on simulation results and compared with [8] with standard cells. The HDCs consist of different numbers of internal inverters and show various delay values. In addition, the proposed cells reduce power consumption to a minimum of 10%, 29%, and 89% of the original power in the coarse-tuning stage and the two fine-tuning stages, respectively. To evaluate the proposed cells, Fig. 4 illustrates the measured P2-DCO power dissipations. Power consumption tremendously decreases with longer output period as the largest delay time is dominated by the most power-to-delay efficient HDCs (larger R_k with smaller $P_{d,k}$) in the delay path. In contrast with the proposed HDC-based P2-DCO, an inverter-based P2-DCO is

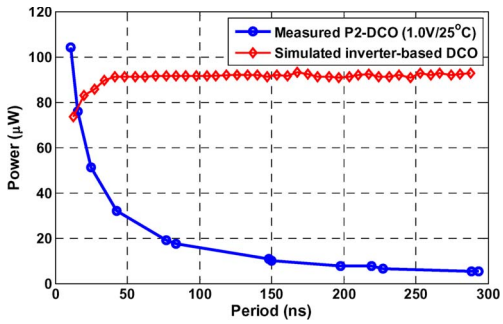

Fig. 4. DCO power comparison.

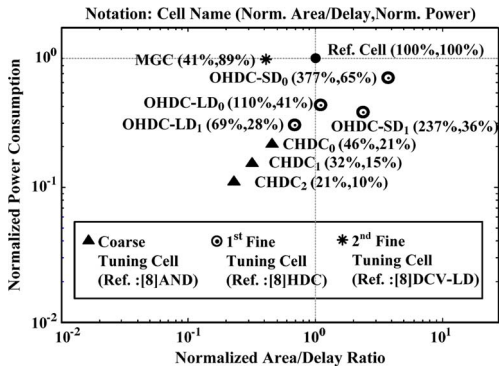

Fig. 5. Comparison of power-to-delay and area-to-delay ratios.

TABLE II
COMPARISONS BETWEEN LINEAR AND POWER-OF-2 APPROACHES

	Linear DCO [8]	P2-DCO
Target Frequency	5MHz	5MHz
Delay Cell W/L	2996μm/90nm	1831μm/90nm
Path Selection W/L	6141μm/90nm	24μm/90nm
Normalized Area	100%	20.3%
Power Consumption	150μW (100%)	7.9μW (5.3%)

simulated for comparison. The simulation result shows that its power consumption is fixed at the same power level with different periods due to the use of identical delay cells.

Generally, the most DCO area is occupied by the coarse-tuning stage to provide a sufficient long delay duration. As a result, Fig. 5 further emphasizes the area and power savings compared with standard cells used in [8]. The proposed CHDCs maximally reduce to a 79% area-to-delay ratio, resulting in smaller DCO area occupation. Some OHDCs exhibit a lower area-to-delay ratio; however, power reduction is the prior concern. On the other hand, the power-of-2 feature minimizes the usage of delay cells and path-selection units in each delay segment, thus implying less area and also less power. For instance, Table II compares the simulation results between the linear DCO approach [8] and the proposed P2-DCO approach at a 5-MHz target frequency. The delay line in the linear DCO requires 2047 AND gates to achieve the target delay D (half-period) and 2047 multiplexers for delay path selection. Contrarily, the P2-DCO requires only eight delay segments, eight multiplexers, and eight AND gates used in the coarse-tuning stage. In addition, the required delay stages and multiplexers are proportional to $O(D)$ and $O(2^D)$ in the linear DCO case, respectively. However, both required delay segments and multiplexers are proportional to $O(log_2(D))$ in the P2-DCO case. Accordingly, the required W/L is summarized, and the

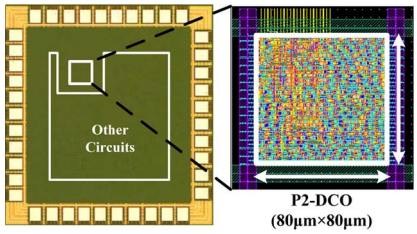

Fig. 6. Microphotograph and layout of the P2-DCO test chip.

TABLE III
MEASUREMENT RESULTS OF THE STEP/RANGE OF THE TUNING STAGE

	Coarse Tuning	1st Fine Tuning	2nd Fine Tuning
Delay Range	1147.79ps ~282.93ns	51.74ps ~4450.17ps	2.05ps ~110.52ps
Least Delay Tuning Step	1147.79ps	51.74ps	2.05ps

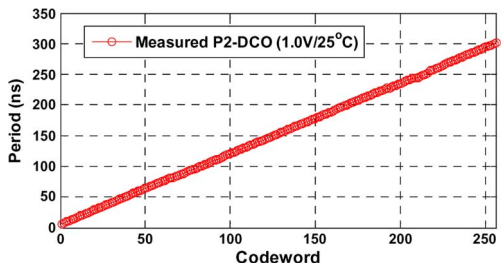

Fig. 7. Measured P2-DCO period in the coarse-tuning stage.

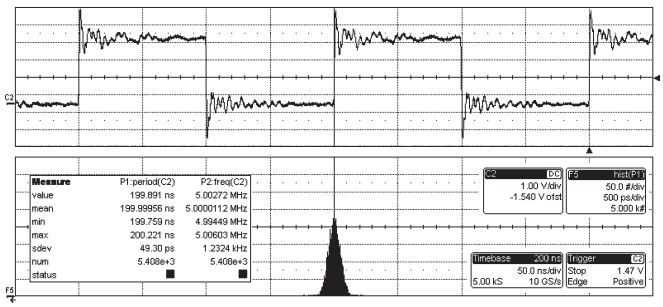

Fig. 8. Jitter histogram of the P2-DCO at 5 MHz.

P2-DCO approach shows a 79.7% area saving and a 94.7% power reduction, as compared with the linear approach.

A test chip is designed based on the required frequency range and resolution. The coarse-tuning stage includes eight delay segments with the DCO delay step from 1 to 128 ns. Each delay segment is a combination of three CHDCs with a power-of-2 order. To ensure the functionality in various design corners, each fine-tuning stage covers at least 1–2 least significant bits (LSBs) of the previous tuning stage. The overlapped range depends on the cell sensitivities to the process–voltage–temperature variation. The first fine-tuning stage, containing combinations of four OHDCs, are utilized to generate the delay step from 64 ps to 2 ns. The second fine-tuning stage produces the DCO delay step from 2 to 64 ps with MGCs.

Fig. 6 shows the microphotograph and layout of the test chip. The P2-DCO occupies an area of 80 μm × 80 μm and is integrated for WBAN applications. The DCO output signal is measured using a LeCroy SDA4000A oscilloscope at 1.0 V/25 °C (with 3.3-V input/output pad supply voltage) to evaluate

TABLE IV
COMPARISONS WITH THE-STATE-OF-THE-ART DESIGNS

	THIS WORK	ISSCC'08[11]	TCAS2'07[8]	TCAS2'05[7]
Process	90nm CMOS	65nm CMOS	90nm CMOS	0.35μm CMOS
Design Approach	Digitally-Controlled Ring Oscillator	Voltage-Controlled Relaxation Oscillator	Digitally-Controlled Ring Oscillator	Digitally-Controlled Ring Oscillator
Supply Voltage (V)	1	1.2 (1.1~1.3)	1	3.3
Operation Range (MHz)	3.4-163.2	12	191-952	18-214
LSB Resolution (ps)	2.05	N/A	1.47	1.55
RMS Jitter	49.30ps (0.02%@5MHz)	-109dBc/Hz* (0.01%@12MHz) **	8.18ps (0.34%@417MHz)	N/A
Power Consumption	5.4μW(3.4MHz) 166μW(163.2MHz)	90μW (12MHz)	140μW (200MHz)	18mW (200MHz)
Area (μm^2)	6400	30000	N/A	40000

*Phase noise $L(f_m)$ with 12MHz oscillator frequency (f_{osc}) and 100kHz offset frequency (f_m). **Equivalent RMS Jitter (%) = $\sqrt{L(f_m)\cdot f_m^2/f_{osc}}$ [13]

the performance. Table III lists the measured least delay tuning step and operation range of each tuning stage in the proposed P2-DCO. The controllable range of each tuning stage is larger than the least DCO delay step of the previous stage; thus, the functionality is guaranteed. In addition, Fig. 7 shows the measurement result in the coarse-tuning stage to analyze the linearity and operation range of the proposed P2-DCO. Fig. 8 shows that the root-mean-square (RMS) phase jitter is 49.30 ps at 5 MHz under 1-V and 40-mV supply noise. This RMS phase jitter is equivalent to −105 dBc/Hz phase noise performance with a 100-kHz offset frequency [13] and complies with WBAN requirements.

Table IV lists the comparison results of the P2-DCO with the state-of-the-art oscillator designs. The P2-DCO provides the least dynamic power consumption (5.4 μW at 3.4 MHz, 166 μW at 163.2 MHz, measured by the difference of the DCO ON and OFF currents) with the least area occupation. Additionally, the proposed HDCs designed in the format of standard cells are compatible with automated computer-aided design tools and, therefore, save design efforts in system integration.

V. CONCLUSION

This brief proposes the on–off and CHDC circuit topologies for low-power DCO design. Accompanied with the power-of-2 structure designed in all-digital methodology, these features demonstrate the feasibility of improved power-to-delay and area-to-delay ratios compared with the state-of-the-art designs. Accordingly, the proposed P2-DCO achieves a megahertz-scale frequency with sub-10-μW power consumption, which minimizes both the system sleeping power and wakeup power. As a result, this brief provides an area/power-efficient solution for a clock source in low-power WBAN applications.

ACKNOWLEDGMENT

The authors would like to thank their colleagues within the SI2 Group, National Chiao Tung University, for fruitful discussions. The authors would also like to thank UMC for test chip fabrication.

REFERENCES

[1] P. Choi, H. C. Park, S. Kim, S. Park, I. Nam, T. W. Kim, S. Park, S. Shin, M. S. Kim, K. Kang, Y. Ku, H. Choi, S. Min Park, and K. Lee, "An experimental coin-sized radio for extremely low-power WPAN (IEEE 802.15.4) application at 2.4GHz," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2258–2268, Dec. 2003.

[2] T. W. Chen, J. Y. Yu, C. Y. Yu, and C. Y. Lee, "A 0.5 V 4.85 Mbps dual-mode baseband transceiver with extended frequency calibration for biotelemetry applications," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 2966–2976, Nov. 2009.

[3] R. B. Staszewski and P. T. Balsara, "Phase-domain all-digital phase-locked loop," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 3, pp. 159–163, Mar. 2005.

[4] R. B. Staszewski, D. Leipold, K. Muhammad, and P. T. Balsara, "All-digital PLL with ultra fast settling," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 2, pp. 181–185, Jan. 2007.

[5] C. C. Chung and C. Y. Lee, "An all-digital phase-locked loop for high-speed clock generation," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 347–351, Feb. 2003.

[6] M. Maymandi-Nejad and M. Sachdev, "A monotonic digitally controlled delay element," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pp. 2212–2219, Nov. 2005.

[7] P. L. Chen, C. C. Chung, and C. Y. Lee, "A portable digitally controlled oscillator using novel varactors," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 5, pp. 233–237, May 2005.

[8] D. Sheng, C. C. Chung, and C. Y. Lee, "An ultra-low-power and portable digitally controlled oscillator for SoC applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 54, no. 11, pp. 954–958, Nov. 2007.

[9] S. F. Al-Sarawi, "Low power Schmitt trigger circuits," *Electron. Lett.*, vol. 38, no. 18, pp. 1009–1010, Aug. 2002.

[10] B. L. Dokic, "CMOS NAND and NOR Schmitt circuits," *Microelectron. J.*, vol. 27, no. 8, pp. 757–765, Nov. 1996.

[11] P. F. J. Geraedts, E. van Tuijl, E. A. M. Klumperink, G. J. M. Wienk, and B. Nauta, "A 90 μW 12 MHz relaxation oscillator with a −162 dB FOM," in *Proc. IEEE ISSCC Dig. Tech. Papers*, Feb 2008, pp. 348–350.

[12] B. Razavi, *RF Microelectronics*. Englewood Cliffs, NJ: Prentice-Hall, 1998.

[13] S. L. J. Gierkink and A. J. M. van Tuijl, "A coupled sawtooth oscillator combining low jitter with high control linearity," *IEEE J. Solid-State Circuits*, vol. 37, no. 6, pp. 702–710, Jun. 2002.

[14] F. Sebastiano, L. J. Breems, K. A. A. Makinwa, S. Drago, D. M. W. Leenaerts, and B. Nauta, "A low-voltage mobility-based frequency reference for crystal-less ULP radios," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 2002–2009, Jul. 2009.