Microelectronic Engineering 87 (2010) 2540–2543

Contents lists available at ScienceDirect

Microelectronic Engineering

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The effect of pulsed laser annealing on the nickel silicide formation

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ARTICLE INFO

Article history:
Received 9 February 2010
Accepted 13 June 2010
Available online 17 June 2010

Keywords:
$NiSi_x$
Pulsed laser annealing (PLA)
Schottky barrier height (SBH)
Rapid thermal annealing (RTA)

ABSTRACT

The pulsed laser annealing (PLA) is used to assist nickel silicide transformation for Schottky barrier height reduction and tensile strain enhancement and the effect of different laser power are investigated. In this report, a two-step annealing process which combine the conventional rapid thermal annealing with pulsed laser annealing is proposed to achieve a smooth silicon-rich $NiSi_x$ interfacial layer on (1 0 0) silicon. With optimized laser energy, a 0.2 eV Schottky barrier height (SBH) modulation is observed from Schottky diode electrical characterization. Furthermore, PLA provides sufficient effective temperature during silicidation which also lead to increased tensile stress of silicide film than the two-step RTA silicide is also investigated. The SBH modulation and tensile stress enhancement benefits of PLA silicidation are considered as an alternative to the conventional rapid thermal annealing for ultra-scaled devices performance enhancement.

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1. Introduction

Nickel silicide is a common silicide material for advanced MOS transistors due to its low formation temperature, low Si consumption, and low line width sheet resistance dependence as compared to cobalt or titanium silicide. However, Fermi-level pining at the NiSi/Si interface sets the work function of NiSi to a mid-gap value of around 4.7 eV, leading to a high source/drain resistance. For this reason, techniques that can potentially reduce the NiSi Schottky barrier height (SBH) are of interest, as they will allow the continued use of nickel silicide in future transistors. A previous study showed that the single crystalline and uniform $NiSi_2$ phase can effectively reduce the SBH by approximately 0.3 eV [1]. However, $NiSi_2$ phase transformation need high temperature and is generally much less stable on the (1 0 0) Si surface than on the (1 1 1) surface [2]. This study report that the advantage of using PLA for $NiSi_x$ formation on (1 0 0) Si. The PLA application is attractive for ultra-scaled semiconductor devices dopant activation due to its high effective temperature with diffusion-less junction profile. By using PLA during silicidation, the Schottky barrier height modulation is observed due to the silicide phase change at silicon interface. The morphology of silicide/silicon interface is smooth when a two-steps annealing process with optimized laser power is adopted. In addition, the strain application for carrier mobility enhancement is more challenge when the technology node is continue shrinking. The aggressive scaling design rules limit the strength of the strain developed in the process due to shrinking device dimensions and issues of proximity [4]. For this reason, process strain enhancement approached from either a type of material aspect or other process that leads to device process optimization become an indispensable procedure for maintaining the strain benefit of ultra-scaled devices [5,6]. The tensile stress enhancement of $NiSi_x$ silicide formation by using PLA is also observed and discussed in this report.

2. Experimental

For experimental study, 6 inch (1 0 0) n and p-type wafers were used as substrates. Before Ni deposition, the wafers were cleaned in HF acid and rinsed with de-ionized water. Inductively-coupled plasma (ICP) pre-sputter was performed for 10 s for native oxide removal, the 20 nm Ni and 15 nm Ti were then deposited sequentially by physical vapor deposition (PVD). The Ti was used as a capping layer to avoid oxygen contamination during silicidation [7]. Wafers then underwent different two-step annealing processes for silicidation and the process flow is shown in Fig. 1. The flow-1 sample employed a two-step rapid thermal anneal (RTA) at 300 °C for 15 s and 400 °C for 30 s in ambient N_2 as a baseline condition. The flow-2 sample was prepared by replacing the first RTA with PLA, and the flow-3 sample was prepared by replacing the second RTA with PLA. The RTA was conducted with Heat Pulse 610 and the PLA was conducted with a pulsed Nd:YAG laser with a 355 nm wavelength and 10 ns pulse period. After the first annealing process, un-reacted Ni and Ti was removed by a wet etchant consisting of H_2SO_4 and H_2O_2 with a ratio of 4:1. The sheet resistance of the sample was measured using a 4-point probe.

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doi:10.1016/j.mee.2010.06.009

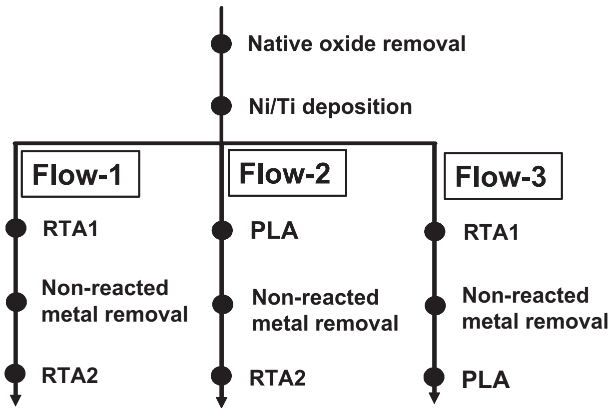

Fig. 1. Three different annealing process flow chart for silicidation evaluation.

The blank wafer stress was measured using a Tencor FLX-2320, which measures the change in the radius of curvature of the substrate. The Schottky diode fabrication was initiated with LOCOS isolation and followed by 35 nm thermal oxide growth. The active area was implanted with BF_2 at 70 keV and a dose of 2×10^{13} cm^{-2} for p-type substrate and phosphorus at 120 keV and a dose of 7.5×10^{12} cm^{-2} for n-type substrate. After implantation, samples were annealed in a 1100 °C furnace for 10 min to activate the dopant. Finally, different Ni silicide formation processes were evaluated and electrical testing was performed using a HP4156.

3. Result and discussion

The correlations of sheet resistance and blanket wafer stress capacities for different annealing conditions and PLA energy densities are shown in Fig. 2. Increased sheet resistance and significant tensile stress enhancement of laser annealed samples are observed compare to the RTA samples. Glancing-incidence XRD was used for silicide phase characterization and result is shown in Fig. 3. The spectrum of the two-step RTA sample reveals inhomogeneous phases of Ni silicide, including Ni-rich silicide and NiSi formed with two-step RTA. By replacing the second RTA with PLA, the rising peak intensity of the Si-rich $NiSi_x$ phase is observed in the spectrum. Increasing the PLA energy density above 1.5 J/cm^2 causes the Ni silicide phase to mostly transfer to $NiSi_2$ and induce significant sheet resistance increasing. Fig. 4 shows transmission

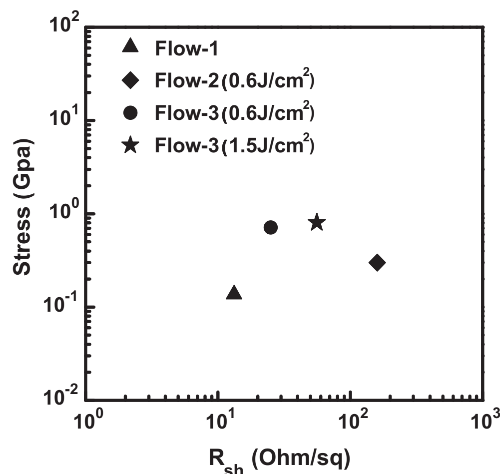

Fig. 2. The stress and sheet resistance correlations of different annealing sequences. The PLA energy density of the flow-3 samples were 0.6 J/cm^2 and 1.5 J/cm^2.

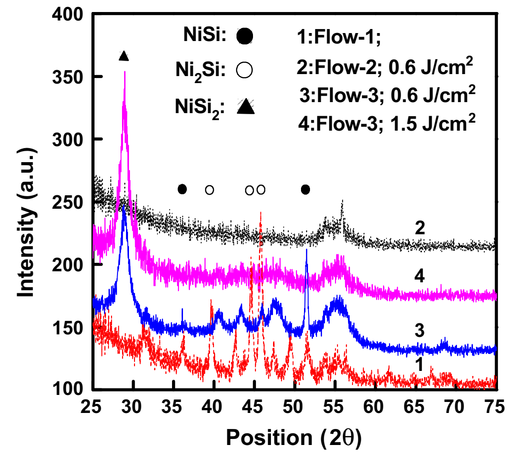

Fig. 3. GIXRD spectrums results for different silicidation sequences.

electron microscopy (TEM) images of different silicidation conditions. Fig. 4a shows that the sample using two-step RTA which exhibits a rough silicide to silicon interface due to the coexistence of inhomogeneous phases. Fig. 4b shows that the sample using PLA first which exhibits an ultra-thin $NiSi_2$ formation. The composition of the thin silicide is verified by an energy dispersive X-ray spectrometer (EDS), revealing that 0.6 J/cm^2 of PLA energy is sufficient to incite the Ni to react with Si to form $NiSi_2$. The resulting thin silicide is favorable for ultra shallow junction, however, a $NiSi_2$ {1 1 1} facet appears which would induce junction spiking issue for devices with shallow junction profile. Compared to the PLA-first sample with the same laser energy, the sample replacing the second RTA with PLA exhibits a flat silicide to silicon interface which is shown in Fig. 4c. The PLA energy induces the melting of nickel silicide, and this melt front propagates down to the silicide and silicon interface. The mixing of silicide and silicon occurs via a liquid phase diffusion, which leads to a flat interface and silicon-rich silicide melt near the interface [8]. The silicide thickness and stress difference correlation is further investigated to exclude the volume change effect, results are shown in Fig. 5. The different silicide thickness are obtained by increasing the RTA temperature and PLA energy density for flow-1 and flow-3, respectively and the silicide layer thickness are investigated by TEM. Based on the result, the combined effect of an increased effective temperature of PLA with different silicide phases formed after PLA can lead to thermal stress differences and result in higher tensile stress. Although the strain benefit decreases as the silicide thickness decreases, the improved silicide morphology using pulsed laser annealing is beneficial for process control with an aggressive reduction in silicide to channel proximity, as it obtains higher channel strain with resistance reduction for future extremely scaled transistors.

Fig. 6a shows the comparison of two favorable Schottky diode I–V characteristics. The area of the measured diode is 4×10^{-6} cm^2 and the zero bias SBH of each sample is deduced by linear fitting of the forward-bias I–V characteristics based on the thermionic emission model at room temperature, using an effective Richardson constant of 32 A/cm^2 K^2 in the calculation [9]. The diode with the PLA shows approximately 0.2 eV SBH increase for hole from a highly rectifying diode with improved ideality factor ($n = 1.28$) and the obtained SBH ($\Phi_{bo} = 0.68$ eV) is close to the reported value for $NiSi_2$ on a (1 0 0) p-type substrate [10,11]. The result is also examined by using the slope of the Arrhenius plot in the reverse-bias region and the result is in good agreement with the value deduced from forward bias current which is shown in Fig. 6b. At the same time, Fig. 6c shows an ohmic-like characteristic

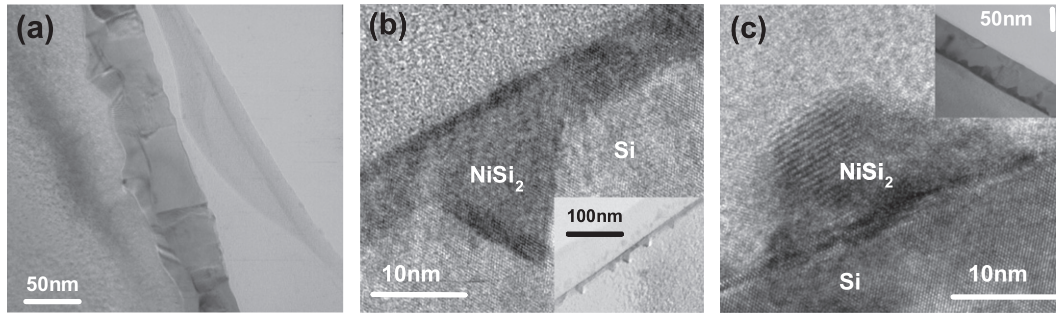

Fig. 4. Cross-sectional TEM images of (a) the flow-1 (two-step RTA) sample. (b) Flow-2 sample with 0.6 J/cm^2 laser annealing. (c) Flow-3 sample with 0.6 J/cm^2 laser annealing.

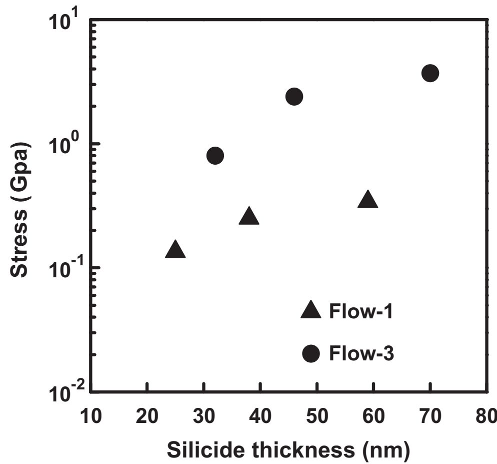

Fig. 5. The stress and silicide thickness correlations. Different 1st RTA conditions (300 °C, 350 °C and 400 °C, all for 15 s) were used to obtain different silicide thickness for the flow-1 and different PLA energy density (0.6 J/cm^2,1.5 J/cm^2 and 2.3 J/cm^2) were used to obtain different silicide thickness for the flow-3.

of laser irradiated sample which was fabricated on n-type substrate, also proves SBH modulation effect. Fine tuning the energy density of PLA within the adequate range improves the diode ideality factor, which is shown in Fig. 7, due to the formation of smooth $NiSi_2$ morphology at the silicon interface. However, increasing the laser energy density above a critical range causes a significant increase of leakage current and a drop in the ideality factor due to degraded interface morphology. From TEM investigation, a Si-rich ($Ni_{0.23}Si_{0.77}$) Ni silicide forms and leads to deterioration in the interface flatness which cause the diode characteristics degradation. For further improvement of the diode ideality factor, while maintaining a reasonable sheet resistance under sufficient laser energy, special consideration should be made of the silicide with uniform composition at the equilibrium phase before the

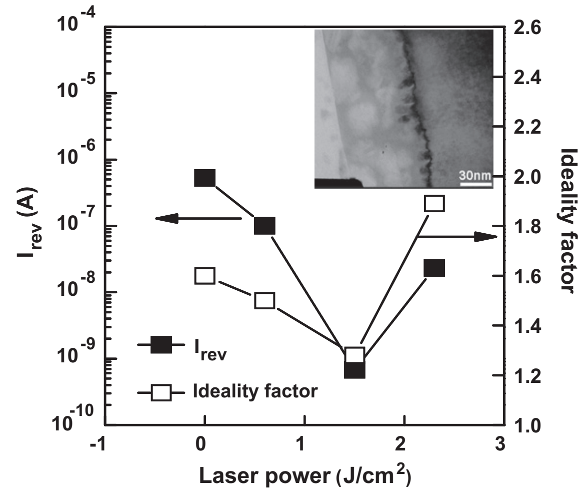

Fig. 7. The reverse-biased (V_d = 0.5 V) diode current and the diode ideality factor of different laser energy densities. The different energy densities are obtained by changing the laser power from 0.7 W to 2.6 W. Inset shows the TEM cross-section view of sample with laser energy density increase to 2.3 J/cm.

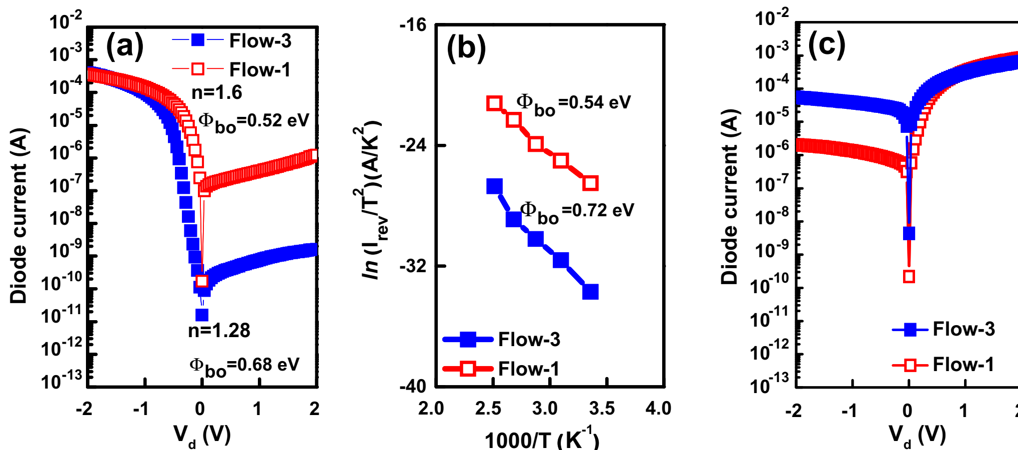

Fig. 6. (a) The highly rectifying p-Si substrate diode of flow-3 with laser energy density equal to 1.5 J/cm^2 indicates SBH increased for hole. (b) The Arrhenius plot of reverse-biased (V_d = 0.5 V) diode current for SBH extraction. (c) A ohmic-like I–V characteristic of flow-3 with n-Si substrate which indicate the SBH reduced for electron.

PLA to improve the microstructure of both the interface and the bulk region of silicide.

4. Conclusion

In summary, this study demonstrates an enhancement of the nickel silicide tensile strain model and a new approach to SBH modulation by replacing the conventional second RTA of a two-step annealing process with pulsed laser annealing. The improved silicide interface morphology, combined with SBH modulation, reduces the interfacial resistance without sacrificing junction leakage and makes this approach attractive for improving ultra-scaled device performance.

Acknowledgement

This work was performed by NDL facilities and supported by the National Science Council, Taiwan.

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