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Improvement in RF performance of 40-nm InAs-channel based HEMTs using Pt gate sinking with two-step recess processes technology

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ABSTRACT

Forty-nanometer InAs HEMT devices fabricated by two-step recess and Pt-buried gate were demonstrated for low-noise and low-power millimeter wave applications. The device exhibited a high transconductance of 1650 mS/mm at a drain voltage of 0.5 V. Improvement of the current-gain cutoff frequency from 395 GHz to 423 GHz was achieved with minimum noise figure below 2.5 dB up to 64 GHz at only 4.33 mW DC power consumption level. Besides, the output conductance was decreased from 2400 mS/mm to 325 mS/mm. These superior performances are attributed to mitigation of the short-channel effect through the proposed technology.

1. Introduction

Among all the components in RF front-end receivers, low-noise amplifier (LNA) plays the most important role in the determination of system sensitivity which is critical in the evaluation for overall system performance. High performance LNA featuring high gain and low-noise with minimum DC power consumption is always desired in millimeter and sub-millimeter wave systems such as outer-space radars and handheld imagers. Among all the possible technologies to meet such stringent requirements, high indium content $In_xGa_{1-x}As$-based HEMTs are particularly promising [1–3], due to their significant transport properties like high electron mobility, high saturation velocity, high sheet electron densities, and large Γ to L valley separation even in low electric field. In addition to the excellent electrical properties of $In_xGa_{1-x}As$ material, the superior band-gap design of HEMTs also makes $In_xGa_{1-x}As$ HEMTs outstanding candidates for applications in ultra high speed and low voltage logic circuitry [4].

Current-gain cutoff frequency (f_T) is an important figure of merit commonly adopted to evaluate the capability of a device for high-frequency operations. Relationship between f_T and intrinsic device parameters can explicitly be expressed as:

$$f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})};$$

where g_m is the intrinsic transconductance and $C_{gs}+C_{gd}$ is the total gate capacitance of the intrinsic device, respectively.

Apparently, increasing g_m and decreasing total gate capacitance are essential to achieve high f_T. In general, small total gate capacitance can be accomplished by shortening the gate length, which also increases the electric field under the gate resulting in the acceleration of the transport property of the channel electrons. Therefore, shrinking the gate length is an effective way to get high g_m and low total gate capacitance so as to attain high f_T [5].

On the other hand, the minimum noise figure (NF_{min}) can also be related semi-empirically to the device parameters as given by [6]:

$$NF_{min} = 1 + 2\pi kf(C_{gs}+C_{gd})[(R_g+R_s)/g_m]^{1/2};$$

with k being a fitting parameter. It is obvious that the reduction of the capacitances and resistances will essentially contribute to the reduction of NF_{min} which is also accomplishable through gate length reduction accompanied by the usage of low resistance structure layers and process.

Although the lateral reduction of gate length seems to be a good approach both for high-frequency and low-noise applications, such approach most likely causes performance degradation due to the inevitable short-channel effect. Thus, care must be taken in obtaining the optimal process control parameters to suppress the short-channel effect. Two-step recess process and Pt gate sinking technology [7,8] have been widely used in the fabrication of HEMTs since they provide the promising solutions that enable vertical reduction of gate-to-channel distance without increasing the access resistance significantly [9]. Meanwhile, the short-channel effect can be effectively minimized. By precise control of the annealing time during Pt gate sinking process, diffusion of Pt toward channel drives the gate electrode further close to channel layer which in turn guarantees excellent device performance at frequencies. Another advantage of using Pt-based structure is the relatively large Schottky barrier height which will suppress gate leakage current [9].

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In this work, the electron beam lithography system was used to fabricate nanometer (40-nm) gate length for InAs HEMTs. Besides, two-step recess and Pt gate sinking processes were applied simultaneously to effectively reduce the gate-to-channel distance on 40-nm device for the first time. Comparisons of the device performance at high frequencies with conventional gate recess process were made and significant improvement was observed.

2. Experimental

The HEMT structure in this study was grown by molecular beam epitaxy (MBE) on a 2-inch diameter InP substrate. The structure layers, from bottom to top, consist of a 500 nm $In_{0.52}Al_{0.48}As$ metamorphic buffer layer, a 5 nm InAs channel layer composed of a 3 nm $In_{0.53}Ga_{0.47}As$ lower sub-channel layer with a 2 nm $In_{0.53}Ga_{0.47}As$ upper sub-channel layer and an 8 nm $In_{0.52}Al_{0.48}As$ Schottky barrier layer with Si planar doping ($4 \times 10^{12}\ cm^{-2}$), a 5 nm InP etching stop layer and a 40 nm highly Si-doped $In_{0.53}Ga_{0.47}As$ cap layer ($1 \times 10^{19}\ cm^{-3}$). The $In_{0.53}Ga_{0.47}As$ sub-channels were adopted to enhance better confinement of electrons in the thin InAs layer and improve the electron transport properties.

For the device fabrication, the active area of the device was isolated by wet etching. Au–Ge–Ni–Au was deposited on heavily doped *n*-InGaAs cap layer and then alloyed in rapid thermal annealing (RTA) to form source and drain ohmic contacts with low contact resistance and sheet resistance. Before the formation of T-shaped gate photoresist, the 600 Å silicon nitride was deposited by plasma enhanced chemical vapor deposition as the support of the following 40-nm gate foot. The T-shaped gate photoresist was carried out by using 50-kV JEOL electron beam lithography system (JBX 6000FS). The tri-layer EB photoresist system (ZEP/PMGI/ZEP) with double exposure and development was used to define the 40-nm gate length. The top layer of T-shaped gate was exposed with low dosage, and the fine footprint was written with high dosage. Through anisotropic CF_4 RIE dry etching, the gate foot was precisely replicated on 600 Å SiN_x layer. Then, the two-step recess technique was performed. The first step of recess was cap layer etching performed by using PH-adjusted solution of succinic (S.A.), NH_4OH and H_2O_2. And the second step of recess etching was achieved by inductive coupled plasma (ICP) with argon ambient to remove the InP etching stop layer under the gate. Schottky gate metal, which was composed of Pt (6 nm)/Ti(80 nm)/Pt(60 nm)/Au(180 nm), was then deposited by electron beam evaporation. Gate metal will form after lift-off procedure by acetone and ZDMAC. An adequate time of Pt sinking annealing at 250 °C was controlled to obtain the optimal performance for these devices. Finally, 100-nm-thick silicon nitride layer was deposited by PECVD at 200 °C for 10 min for devices passivation.

SEM image of the 40-nm T-shaped gate is shown in Fig. 1. As can be seen from the SEM image, the fabricated 40-nm T-gate shows structural stability even with very narrow gate footprint.

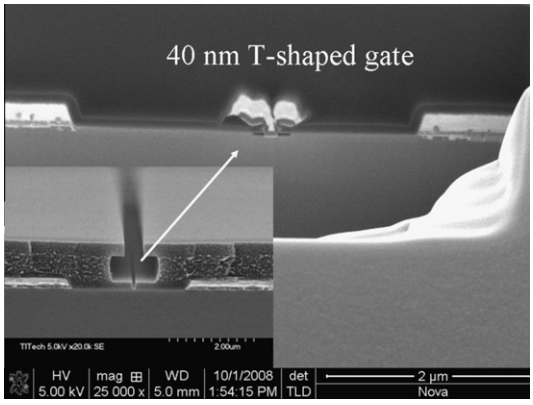

Fig. 1. SEM images of the 40-nm T-shaped gate photoresist profile and the finished 40-nm gate after the two-step recess process.

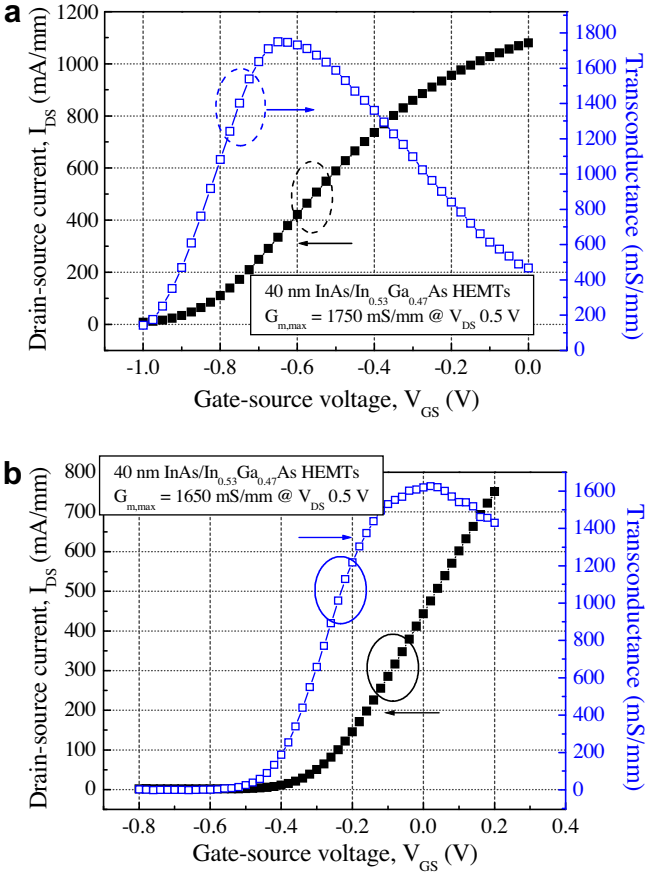

Fig. 2. Transconductance versus gate-source voltage of 40-nm InAs HEMTs for (a) conventional and (b) with two-step recess and gate sinking process.

3. Result and discussion

The transconductance (g_m) and the drain-source current plotted as functions of gate-source voltage are shown in Fig. 2a for conventional device and Fig. 2b for device with two-step recess and gate sinking process. The 40-nm InAs HEMTs exhibit very high transconductance resulting from the high electron mobility of the InAs channel material. Obviously, a shift in the threshold voltage from −1.0 V to −0.4 V is observed for device with two-step recess and gate sinking. Meanwhile, the corresponding gate bias for peak g_m occurrence also shifted toward more positive side. Both shifts in the threshold voltage and peak g_m occurrence evidenced the reduction in the gate-to-channel distance with the tradeoff being a slight decrease in $g_{m,max}$ from 1750 mS/mm to 1650 mS/mm at V_{DS} = 0.5 V for device with two-step recess and gate sinking process. Such decrease in $g_{m,max}$ arose mainly from an slight increase in the source resistance as gate-channel thickness was scaled down, though other factors also appeared to be involved. Besides, the output conductance (g_o) of 325 mS/mm at V_{DS} = 0.5 V with two-step recesses was obtained. For the conventional structure, the g_o was 2400 mS/mm. The output conductance plays an important role in determining the maximum voltage gain attainable and

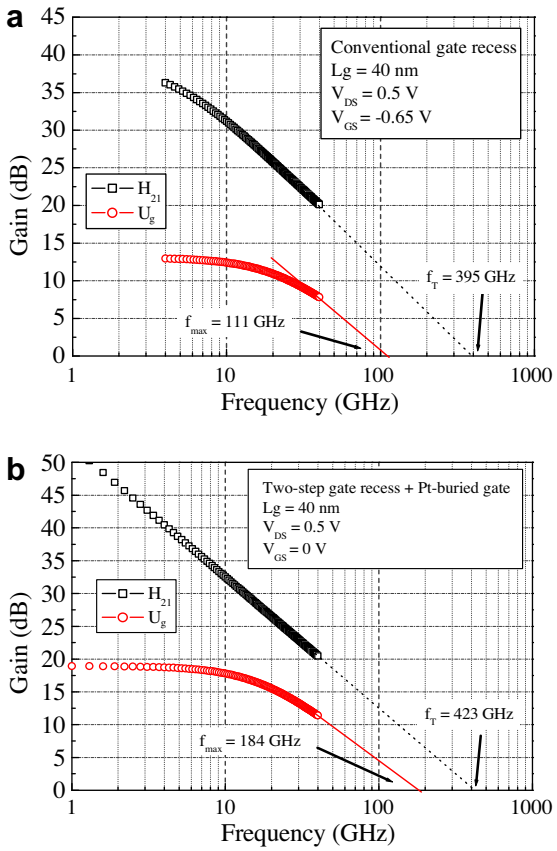

Fig. 3. Frequency dependence of the current-gain (H_{21}) and the Mason's unilateral gain (U_g) of 40-nm InAs/$In_{0.53}Ga_{0.47}As$ composite channel HEMTs for (a) conventional device biased at V_{DS} = 0.5 V and V_{GS} = −0.65 V; and (b) with two-step recess and gate sinking processes biased at V_{DS} = 0.5 V and V_{GS} = 0 V.

optimum output matching properties from the device. Moreover, reduction of output conductance effectively guarantees the suppression of short-channel effect which is of crucial importance for small gate-length devices.

The *S*-parameters of the 40-nm InAs HEMTs were measured to 40 GHz using Cascade Microtech™ on-wafer probing system with Anritsu 37369C vector network analyzer. Fig. 3a and b shows the frequency dependence of the current-gain (H_{21}) and the Mason's unilateral gain (U_g) for the conventional device and the device with two-step recess and gate sinking process measured at V_{DS} = 0.5 V. The parasitic effects (mainly capacitive) due to the probing pads have been carefully removed from the measured *S*-parameters using the same method as in [10] and the equivalent circuit model in [11]. Since the geometry of the probing pads are relatively large compared to the device itself, the *S*-parameters of the open probing pads have been carefully characterized through full-wave electromagnetic simulations with measurement. The value of f_T and f_{max} are extracted by extrapolating the H_{21} and the U_g with a −20 dB/decade slope. A higher f_T of 423 GHz and f_{max} of 184 GHz were obtained for device with two-step recess and gate sinking processes as compared to the conventional device with an f_T of 395 GHz and an f_{max} of 111 GHz. Such RF performance improvements were mainly resulted from the reduced gate-to-channel distance

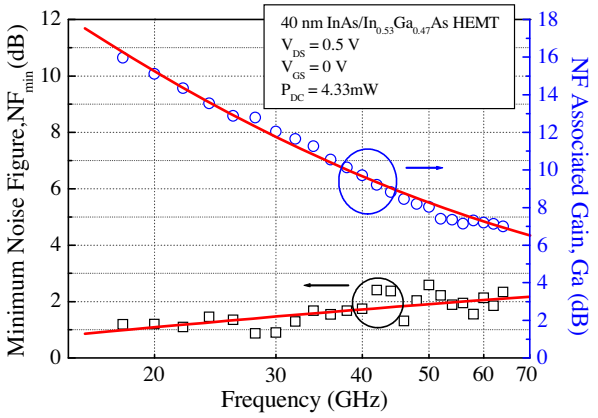

Fig. 4. Measured minimum noise figure (NF_{min}) and the associated gain of the 40-nm InAs HEMTs with two-step recess and gate sinking processes at V_{DS} = 0.5 V; the corresponding DC power consumption was 4.33 mW.

through the two-step recess and gate sinking processes. In this study, the significant improvement of f_{max} was mainly attributed to the reduction in R_g and C_{gd}. Table 1 summarizes the extracted intrinsic parameters for both devices at same drain bias conditions with gate bias set at peak g_m. Clearly, the decrease of total gate capacitance ($C_{g,total}$) and increase of the RF transconductance both contributed to the increase of f_T as expected. It is worth mentioning that the total DC power consumption is as low as 4.33 mW for device with two-step recess and gate sinking process.

To demonstrate the capability of the proposed device for low-noise applications at high frequencies, noise measurement was performed on the device with DC bias set as the same for maximum f_T, shown in Fig. 4. As is observed from the figure, the overall NF_{min} is below 2.5 dB with frequency ranging from 18 GHz to 64 GHz, and the corresponding associated gain (Ga) is 7 dB at 64 GHz while the total DC power consumption remains as low as 4.33 mW. Overall, these superior results show great potential of 40-nm InAs/$In_{0.53}Ga_{0.47}As$ HEMTs for ultra low-power, high-frequency and low-noise RF applications.

4. Summary

In this study, the 40 nm InAs/$In_{0.53}Ga_{0.47}As$ HEMTs using two-step recess and Pt gate sinking technologies for RF performance improvement is demonstrated. Vertical reduction of the gate-to-channel distance is achieved by the advanced process technology and the short-channel effect has been effectively minimized with the electrons in the channel further accelerated. Significant improvement of f_T and f_{max} was exhibited attributing to the increase in transconductance and decrease in total gate capacitance due to the shorter gate-to-channel distance.

For the first time, noise characterization up to V-band was performed on the fabricated 40-nm device biased at extremely low DC power consumption level of 4.33 mW. The device exhibited a minimum noise figure of lower than 2.5 dB up to 64 GHz with corresponding associated gain of 7 dB at 64 GHz.

Overall, the promising experimental results demonstrated that superior device performance for low-noise and low-power millimeter/sub-millimeter wave applications can be achieved by using

Table 1
Summary of extracted RF parameters for 40 nm InAs/$In_{0.53}Ga_{0.47}As$ HEMTs at V_{DS} = 0.5 V for conventional device and device with two-step recess and Pt gate sinking process.

	$G_{m,RF}$ (mS)	C_{gs} (fF)	C_{gd} (fF)	$C_{g,total}$ (fF)	R_g (Ω-mm)	H_{21} @ 40 GHz (dB)	f_T (GHz)	f_{max} (GHz)
Conventional	190	29	48.4	77.4	0.344	20.12	395	111
With two-step recess and gate sinking	196	37.7	33.3	71	0.256	20.5	423	184

40-nm InAs HEMTs with two-step recess and Pt gate sinking technologies.

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