SCR Device With Dynamic Holding Voltage for On-Chip ESD Protection in a 0.25-μm Fully Salicided CMOS Process

Ming-Dou Ker and Zi-Ping Chen

***Abstract*—A dynamic-holding-voltage silicon-controlled rectifier (DHVSCR) device is proposed and verified in a 0.25-μm/2.5-V salicided CMOS process. In the DHVSCR device structure, the control nMOS and pMOS transistors are directly embedded in SCR device structure. The proposed DHVSCR device has the characteristics of tunable holding voltage and holding current by changing the gate voltage of embedded nMOS and pMOS. Under normal circuit operating condition, the DHVSCR has a holding voltage higher than the supply voltage without causing a latch-up issue. Under an electrostatic discharge (ESD) stress condition, the DHVSCR has a lower holding voltage to effectively clamp the overshooting ESD voltage. From the experimental results, the DHVSCR with a device width of 50 μm can sustain a human-body-model ESD level of 5.6 kV.**

***Index Terms*—Electrostatic discharge (ESD), holding voltage, latch-up, silicon-controlled rectifier (SCR).**

I. Introduction

On-chip electrostatic discharge (ESD) protection is necessary for advanced subquarter-submicrometer CMOS integrated circuits (ICs). A silicon-controlled rectifier (SCR) device is an attractive choice for on-chip ESD protection, since it can offer the maximum ESD robustness while occupying the smallest layout area. But, the SCR device often has a high trigger-on voltage in the subquarter-micrometer CMOS technology, which is generally greater than the gate-oxide breakdown voltage of the input stage. To reduce the trigger-on voltage of the SCR device, a low-voltage-triggered SCR (LVTSCR) device was reported [1], [2]. However, an LVTSCR device is often susceptible to latch-up danger during normal circuit operations in a noisy environment [3]. Such latch-up phenomenon often leads to IC function failure or even destruction. Two methods were reported to solve this problem [4]. One way is to increase the holding voltage of the SCR device to be larger than the supply voltage [5], [6]. But, this method leads to more power dissipation (Power $\cong I_{\rm ESD} \times V_{\rm hold}$) located on the LVTSCR device during ESD transition, therefore, in turn causing a lower ESD robustness. The other way is to increase the triggered current of SCR greater than 200 mA [7], [8]. Besides, the high-holding current SCR (HHI-SCR) device [9] has been also reported to increase holding current above certain minimum latch-up triggered current. But, this device needs to shunt a very small resistance ($\sim$ 2 Ω) [9] from the external shunt resistor to increase its holding current. To fabricate this small resistance with high current conduction, it will take up a large layout area on the chip. Recently, the latch-up free gate-couple LVTSCR (LFGCPSCR) device [10] was reported to avoid SCR turn-on during normal condition. But, the device width of the controlled nMOS for LFGCPSCR should be very large ($\sim$ 1000 μm) to increase the holding voltage of LFGCPSCR [10]. A large chip area must be occupied by the controlled nMOS transistor with a huge channel width to realize the LFGCPSCR.

Manuscript received April 13, 2004. The review of this brief was arranged by Editor R. Singh.

M.-D. Ker is with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: mdker@ieee.org).

Z.-P. Chen is with the Product and ESD Engineering Department, SOC Technology Center, Industrial Technology Research Institute, Hsinchu, Taiwan, R.O.C. (e-mail: zpchen@itri.org.tw).

Digital Object Identifier 10.1109/TED.2004.834904

According to previous solutions and problems, a dynamic holding voltage SCR (DHVSCR) device is proposed in this brief to solve ESD protection issues without latch-up danger [11]. Compared to the HHI-SCR [9] and LFGCPSCR [10], the DHVSCR does not need to shunt an external resistor to modify the holding current of HHI-SCR, nor to add a large controlled nMOS transistor to increase the holding voltage of LFGCPSCR. The control transistor is directly embedded in the DHVSCR device structure, therefore, the layout area of the new proposed DHVSCR device can be efficiently reduced to save silicon cost.

II. Holding Voltage of SCR Devices

The first-order equivalent circuit of SCR device is shown in Fig. 1(a) [12], where $R_{\rm well}$ and $R_{\rm sub}$ denote the equivalent N-well and p-substrate resistances, respectively. The $Q_{\rm pnp}$ and $Q_{\rm npn}$ denote the p-n-p and n-p-n bipolar junction transistors, respectively. The R_{s1} and R_{s2} denote the parasitic resistances in the semiconductor. The external variable resistance $R_{\rm ext}$ is shunted to the p-substrate resistance $R_{\rm sub}$. When SCR operated in latch-up holding state, the p-n-p and n-p-n transistors should be both turned on. The holding voltage ($V_{\rm hold}$) of SCR device can be expressed as [13]

$$V_{\rm hold} \cong V_{\rm cep} + V_{\rm ben} \times \left[1 + \frac{R_{s2}}{(R_{\rm sub}//R_{\rm ext})}\right] \tag{1}$$

where the $V_{\rm cep}$ is the voltage difference between the collector and emitter of p-n-p bipolar junction transistor $Q_{\rm pnp}$. The $V_{\rm ben}$ is the voltage difference between the base and emitter of n-p-n bipolar junction transistor $Q_{\rm npn}$. According to (1), the holding voltage of SCR can be adjusted by changing the resistance of $R_{\rm ext}$. If the resistance of $R_{\rm ext}$ is smaller than that of $R_{\rm sub}$, the holding voltage of SCR can be increased. On the contrary, the holding voltage of SCR device can be reduced when the resistance of $R_{\rm ext}$ is larger than that of $R_{\rm sub}$.

III. DHVSCR Device

The device cross-sectional view of DHVSCR is shown in Fig. 1(b), where a pMOS PM2 and an nMOS NM2 are inserted into the SCR device structure. Compared with the traditional pMOS-LVTSCR structure [2], which has a similar device structure as that of the lateral insulated gate bipolar transistor [14], the shallow trench isolation region is replaced by an embedded nMOS NM2 in DHVSCR. The source of NM2 is connected to the cathode of DHVSCR, and the drain of NM2 is connected to that of pMOS PM2. When NM2 operated under ON state, the channel resistance of NM2 is smaller than the resistance of $R_{\rm sub}$, therefore, the holding voltage of DHVSCR can be raised up greater than the supply voltage. So, the latch-up phenomenon will not happen on the DHVSCR during normal circuit operating condition. On the contrary, the channel resistance of NM2 becomes larger than the resistance of $R_{\rm sub}$, when NM2 operated under the off state. Thus, the holding voltage of DHVSCR can be reduced smaller than the supply voltage. The effectiveness of the embedded nMOS transistor NM2 is similar to the variable resistance $R_{\rm ext}$. Therefore, the holding voltage of DHVSCR can be adjusted by changing the operation state of NM2. In addition, to improve turn-on speed of DHVSCR devices under ESD stress condition, the gate-coupling technique [15] or *RC*-based detection circuit [16] can be used to control the gate of PM2. On the contrary, the gate of PM2 will be biased at 2.5-V supply voltage to avoid SCR being accidentally triggered on during normal circuit operating condition.

0018-9383/04$20.00 © 2004 IEEE

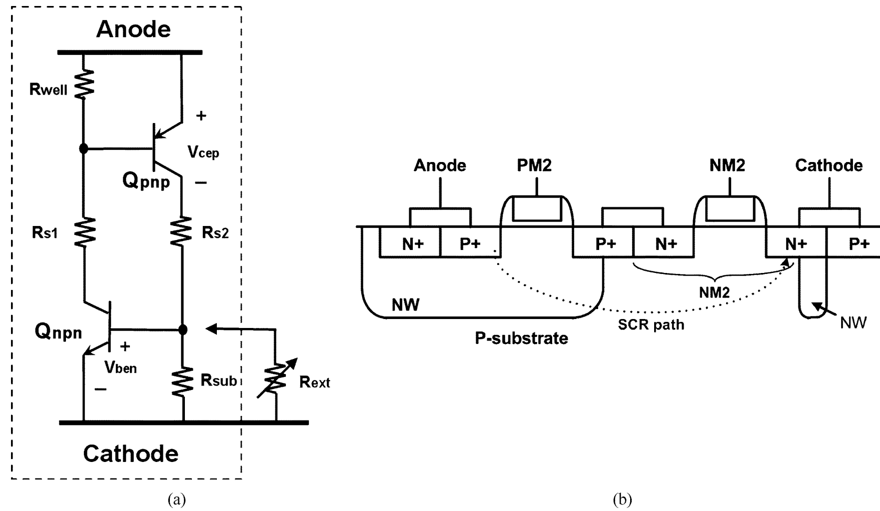

Fig. 1. (a) First-order equivalent circuit of SCR device, where the resistance of R_{ext} is used to shunt the p-substrate resistance R_{sub} for adjusting its holding voltage. (b) Device cross-sectional view of the new proposed DHVSCR.

IV. Experimental Results

The proposed DHVSCR has been fabricated in a 0.25-μm CMOS process with fully salicided diffusion. The snapback current-voltage (*I–V*) curves of DHVSCR at different temperatures under normal circuit operating and ESD stress conditions are measured in Fig. 2(a) and (b), respectively. Under normal circuit operating conditions, the gate voltage of embedded PM2 and NM2 is biased at 2.5 V, as the inset shows in Fig. 2(a). In Fig. 2(a), the trigger-on voltage (V'_{t1}) and holding voltage (V'_{hold}) of DHVSCR at the temperature of 25 °C are 7.48 and 3.08 V, respectively. When the temperature is increased to 125 °C, the trigger-on voltage (V''_{t1}) and holding voltage (V''_{hold}) of DHVSCR are decreased to 6.86 and 2.73 V, respectively. Because the holding voltage of DHVSCR at 125 °C is still higher than the V_{dd} supply voltage of 2.5 V, the latch-up issue can be overcome at such a high temperature. Under ESD stress condition, the gate voltage of PM2 and NM2 is biased at 0 V. In Fig. 2(b), the trigger-on voltage (V_{t1}) and holding voltage (V_{hold}) of SCR are dropped to only 3.57 and 2.17 V, respectively. With the lower trigger-on and holding voltages, the overstress ESD pulse can be effectively clamped by the DHVSCR to protect the internal circuits against ESD damage. So, the holding voltage and trigger-on voltage of DHVSCR can be adjusted by controlling the gate voltage of NM2 and PM2.

To verify the effectiveness of NM2 in the DHVSCR structure, the holding voltage of DHVSCR is measured with different external resistance (VR) connected between the node R and ground. The measurement setup is shown in the inset of Fig. 3, where the gate voltage of NM2 (PM2) is biased at 0 V (2.5 V) to turn off the channel resistance of NM2 (PM2). From the experimental results in Fig. 3, the holding voltage of DHVSCR can be increased greater than 2.5 V when the shunt resistance of VR is less than 100 Ω. This has verified the effectiveness of NM2 in the DHVSCR structure, which is used to increase the holding voltage of the DHVSCR to avoid latch-up issues under the normal circuit operating condition.

Besides, the human-body-model (HBM) and machine-model (MM) ESD robustness of the traditional pMOS-LVTSCR [2] and DHVSCR are measured by a ZapMaster ESD tester, where the devices are in a fully salicided process without using extra masks to block the silicided diffusion. For ESD robustness measurement, the failure criterion is defined at leakage current greater than 1 μA under a 2.5-V bias on pMOS-LVTSCR and DHVSCR. With a device width of 50 μm in the pMOS-LVTSCR, the HBM and MM ESD levels are 6.2 kV and 250 V, respectively. With the same device width of 50 μm in the DHVSCR, the HBM and MM ESD levels are 5.6 kV and 200 V, respectively. The ESD level of DHVSCR is slightly less than that of pMOS-LVTSCR, because the holding voltage of DHVSCR ($\sim$ 2.17 V) under ESD stress condition is slightly higher than that ($\sim$ 1.3 V) of pMOS-LVTSCR. However, with a device width of only 50 μm, the ESD level of DHVSCR is

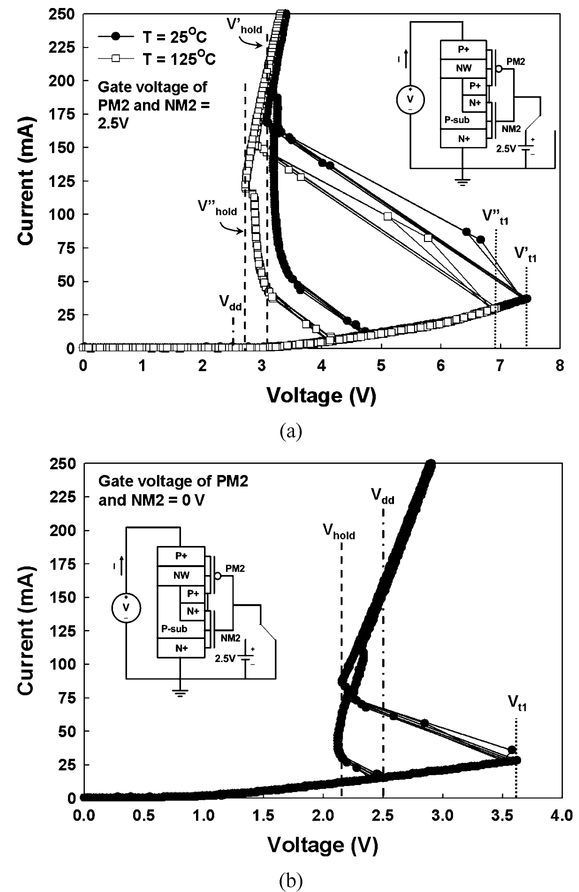

Fig. 2. Snapback *I–V* curves of DHVSCR measured under (a) the normal circuit operating condition with the gate bias of 2.5 V on PM2 and NM2 at the temperature of 25 °C or 125 °C, and (b) the ESD stress condition with the gate bias of 0 V on PM2 and NM2 at the temperature of 25 °C.

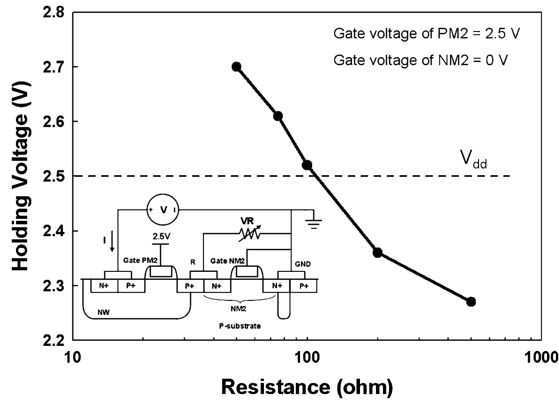

Fig. 3. Dependence of the shunt resistance (VR) on the holding voltage of DHVSCR. The measurement setup is shown in the inset.

still high enough for on-chip ESD protection design without latch-up issues.

V. Conclusion

The proposed DHVSCR device has been successfully verified in a 0.25-μm/2.5-V fully salicided CMOS process. From the experimental results, the holding voltage of DHVSCR can be adjusted by changing the gate bias of the embedded nMOS and pMOS in DHVSCR structure to avoid latch-up issue during normal circuit operating condition. The proposed DHVSCR device with suitable ESD-detection circuit can be used in I/O pads, power-rail, and whole-chip ESD protection circuits. For whole-chip ESD protection design, all DHVSCR devices can be controlled by a common ESD-detection circuit to save the layout area of ESD-detection circuit for every pin.

References

[1] A. Chatterjee and T. Polgreen, “A low-voltage triggering SCR for on-chip ESD protection at output and input pads,” *IEEE Electron Device Lett.*, vol. 12, pp. 21–22, Jan. 1991.

[2] M.-D. Ker, C.-Y. Wu, and H.-H. Chang, “Complementary-LVTSCR ESD protection circuit for submicrometer CMOS VLSI/ULSI,” *IEEE Trans. Electron Devices*, vol. 43, pp. 588–598, Apr. 1996.

[3] M.-D. Ker, “ESD protection for CMOS ASIC in noisy environments with high-current low-voltage triggering SCR devices,” in *Proc. IEEE Int. ASIC Conf. and Exhibits*, 1997, pp. 283–286.

[4] M.-D. Ker and H.-H. Chang, “How to safely apply the LVTSCR for CMOS whole-chip ESD protection without be accidentally triggered on,” in *Proc. EOS/ESD Symp.*, 1998, pp. 72–85.

[5] G. Notermans, F. Kuper, and J. M. Luchies, “Using an SCR as ESD protection without latch-up danger,” *Microelectron. Reliab.*, vol. 37, pp. 1457–1460, 1997.

[6] J. Z. Chen, T. A. Vrotsos, and Y.-S. Chang, “Tunable Holding Voltage SCR ESD Protection,” US Patent 6 172 404, Jan. 2001.

[7] M.-D. Ker, “Lateral SCR devices with low-voltage high-current triggering characteristics for output ESD protection in submicron CMOS technology,” *IEEE Trans. Electron Devices*, vol. 45, pp. 849–860, Apr. 1998.

[8] ——, “ESD protection for CMOS output buffer by using modified LVTSCR devices with high trigger current,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 1293–1296, Aug. 1997.

[9] M. Markus, C. Russ, K. Verhaege, J. Armer, P. Jozwiak, and R. Mohn, “High holding current SCR’s (HHI-SCR) for ESD protection and latch-up immune IC operation,” in *Proc. EOS/ESD Symp.*, 2002, pp. 10–17.

[10] C.-S. Lai, M.-H. Liu, S. Su, and T.-C. Lu, “A novel SCR ESD protection structure with low-loading and latchup immunity for high speed I/O pads,” in *Proc. Int. Symp. VLSI Technology, Systems, Applications*, 2003, pp. 80–83.

[11] Z.-P. Chen and M.-D. Ker, “Dynamic holding voltage SCR (DHVSCR) device for ESD protection with high latch-up immunity,” in *Proc. Int. Conf. Solid State Devices and Materials*, 2003, pp. 160–161.

[12] R. R. Troutman, *Latchup in CMOS Technology: The Problem and Its Care*. Norwell, MA: Kluwer, 1986.

[13] A. Bandyopadhyay, P. R. Verma, A. B. Bhattacharyya, and M. J. Zarabi, “LATCHSIM-a latch-up simulator in VLSI CAD environment for CMOS and BiCMOS circuits,” in *Proc. IEEE Int. Conf. VLSI Design*, 1994, pp. 339–342.

[14] M. R. Simpson, “Analysis of negative differential resistance in the *I–V* characteristics of shorted-anode LIGBTs,” *IEEE Trans. Electron Devices*, vol. 38, pp. 1633–1640, July 1991.

[15] M.-D. Ker, H.-H. Chang, and C.-Y. Wu, “A gate-coupled PTLSCR/NTLSCR ESD protection circuit for deep-submicrometer low-voltage CMOS ICs,” *IEEE J. Solid-State Circuits*, vol. 32, pp. 38–51, Aug. 1997.

[16] M.-D. Ker and H.-H. Chang, “Novel cascade NLSCR/PLSCR design with tunable holding voltage for safe whole-chip ESD protection,” in *Proc. IEEE Custom Integrated Circuit Conf.*, 1998, pp. 541–544.

A Comprehensive Study on the FIBL of Nanoscale MOSFETs

Bing-Yue Tsui and Li-Feng Chin

***Abstract*—Fringing-induced barrier lowering (FIBL) effect on nanoscale MOSFET is comprehensively examined. It is observed that by combining stack gate dielectric, conductive spacer, short sidewall spacer, and minimum gate/drain (G/D) overlap, the I_{off} with a dielectric constant of (k) 100 is only 1.6 times higher than that with $k = 3.9$ when the gate length is 25 nm. The fully depleted silicon-on-insulator device shows even better FIBL immunity. It is concluded that although the FIBL effect can not be eliminated, it would not an issue beyond the 45-nm technology node.**

***Index Terms*—Fringing-induced barrier lowering (FIBL), high dielectric constant material, MOSFET, silicon-on-insulator (SOI), stack gate dielectric.**

I. Introduction

Silicon dioxide $(\mathrm{SiO_2})$ has been used as the gate dielectric of CMOS devices for several decades and as device dimensions scale down, the thickness of SiO_2 must be reduced to keep sufficient current driving capability. However, when the thickness of SiO_2 becomes thinner than 3 nm, direct tunneling current increases dramatically [1]. Although many high dielectric constant (high-κ) materials have been proposed to solve this problem [2]–[10], a side effect called fringing-induced barrier lowering (FIBL) arising from the use of high-κ gate dielectric is a serious problem [11]–[16]. The electrical field originating at the drain penetrates into the channel through the high-κ dielectric and suppresses the barrier height from source to channel. Therefore, the degradation of off-state current (I_{off}) limits the allowable κ value of the gate dielectric.

Manuscript received April 16, 2004; revised July 9, 2004. This work was supported by the National Science Council (NSC) of China under Contract NSC-91-2215-E-009-018. The review of this brief was arranged by Editor R. Singh.

The authors are with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: bytsui@mail.nctu.edu.tw).

Digital Object Identifier 10.1109/TED.2004.835022

0018-9383/04$20.00 © 2004 IEEE