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Low temperature MOSFET technology with Schottky barrier source/drain, high-K gate dielectric and metal gate electrode

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Abstract

Both P- and N-channel MOSFETs with Schottky barrier silicide source/drain (S/D), high-K gate dielectric and metal gate were successfully fabricated using a simplified low temperature process. The highest temperature after the high-K dielectric formation is 420 °C. PMOSFETs with PtSi S/D show excellent electrical performance of an $I_{on}/I_{off} \sim 10^7 - 10^8$ and a subthreshold slope of 66 mV/dec, similar to those formed by a normal process with an optimized sidewall spacer. NMOSFETs with $DySi_{2-x}$ S/D have ~3 orders of magnitude larger I_{off} than that of PMOSFETs and show two slopes in the subthreshold region, resulting in the $I_{on}/I_{off} \sim 10^5$ at low drain voltage. It can be attributed to the relatively higher barrier height (Φ_n) of $DySi_{2-x}$/n-Si than that of PtSi/p-Si (Φ_p) and the rougher $DySi_{2-x}$ film. Adding a thin intermediate Ge layer (~1nm) between Dy and Si can improve the film morphology significantly. As a result, the improved performance of N-MOSFET is observed.

1. Introduction

To scale down metal-oxide-semiconductor field effect transistors (MOSFETs) to tens of nanometers, several essential problems should be overcome or lessened, such as the large direct tunneling current of ultra-thin gate oxide, the depletion and boron diffusion of the poly-Si gate electrode, and the difficulty to form ultra-shallow source/drain (S/D) junctions with low resistance, etc. High-K gate dielectric [1] and metal gate [2] have been used to overcome the first two problems. For the third problem, Schottky barrier silicide S/D structure [3,4] is a potential solution because silicide/Si has an atomic abrupt interface, the ultra-shallow S/D Schottky junction can be easily and accurately formed, and the parasitic resistance of the totally silicidized S/D is much lower than that of conventional heavily doped S/D. Moreover, the *S*chottky barrier *S*ource/*D*rain *T*ransistor (SSDT) eliminates S/D doping and subsequent annealing procedures, the fabrication process is inherent low temperature and simple, those are benefit for high-K dielectrics and metal gate electrodes because they may be degraded by high temperature treatment [5]. Therefore,

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it is very attractive to integrate high-K dielectric, metal gate and silicide S/D using a low temperature process.

However, SSDT usually suffers from a large leakage current and a low I_{on}/I_{off} ratio [6–8]. Carriers from source to channel should transport over a Schottky barrier height (Φ_n for NSSDT, and Φ_p for PSSDT), which behaves as an additional resistance between source and drain, thus reduces the drain on current (I_{on}). Higher I_{on} needs smaller barrier height. On the other hand, drain to substrate forms a reverse-biased Schottky diode. The diode reverse current dominates the MOSFET off current (I_{off}), which depends exponentially on the barrier height (Φ_p for NSSDT, and Φ_n for PSSDT). Smaller off current needs higher barrier height. Because the sum of Φ_n and Φ_p equals approximately to the energy bandgap E_g, i.e., $\Phi_n + \Phi_p \approx E_g$ (1.12 eV for Si), requirements to increase I_{on} and decrease I_{off} need a silicide with barrier height Φ_n as low as possible for NSSDT, and vice versa for PSSDT. In literature, erbium and platinum silicides are usually used for N and P-channel MOSFETs, respectively, [6,7,9,10] because rare earth (RE) metal silicides have the lowest barrier height while PtSi has the second highest barrier height among the known silicides [11]. However, the electrical performance of the reported NSSDT is not as good as that of PSSDT because the barrier height of $ErSi_{2-x}$ is not low enough and the formed RE silicide film by solid-state reaction of deposited RE metal and sub-Si is quite rough [12]. This is the critical obstacle of the usage of SSDT technology.

2. Device fabrication

Si (1 0 0) wafers of both n- and p-type with resistivity of 4–8 Ω cm were used as the starting substrates. After a standard RCA clean and diluted HF (DHF) solution dipping, a ~6 nm HfO_2 film was deposited at 400 °C using $Hf[OC(CH_3)_3]_4$ and O_2 in a MOCVD system, followed by an in situ post-deposition annealing in N_2 ambient at 700 °C to improve the film quality. Then, a HfN (~50 nm)/TaN (~100 nm) stack was deposited as a metal gate in a sputtering system with a base pressure of $\sim 1.4\times10^{-7}$ torr at room temperature, where TaN is used as a capping layer to reduce the gate sheet resistance (~10 Ω/sq.). The wafers were patterned using standard photolithography and reactive ion etching (RIE) procedures to etch the TaN/HfN/HfO_2 stack. Immediately after DHF dipping to remove the native oxide in the S/D region, the patterned wafers were loaded into the sputtering system again to deposit Pt (~100 nm, for PSSDT) or Dy (~100 nm)/HfN (~70 nm) stack (for NSSDT). Silicidation of Pt or Dy was performed by a furnace forming gas anneal at 420 °C for 1 h. Since Dy, as well as other RE metals, can be easily oxidized during ex situ anneal, a capping layer of thermally stable HfN [2] is used to prevent Dy oxidization during the annealing. The un-reacted Pt was etched in a hot diluted aqua regia solution, while the HfN capping layer and the un-reacted Dy were removed by DHF and diluted HNO_3 solutions sequentially.

3. Results and discussion

Fig. 1(a)–(c) show the cross sectional transmission electron microscopy (XTEM) image, the gate leakage current and the C–V curves of the HfN/HfO_2/Si stack, respectively. The effective oxide thickness (EOT) can be deduced using the quantum mechanical (QM) model from the C–V curves. The EOT is between 1.5 and 2.0 nm for all of the MOS-capacitor samples measured where the XTEM image shows that HfO_2 has been partly crystallized. For comparison, the gate leakage of a MOS-capacitor device which has the same stack made by the same process but with an additional 950 °C 30 s anneal is shown in Fig. 1(b). It has a higher gate leakage and its EOT is ~2.4nm. According to gate leakage simulation [13], when scaled up to the same EOT, the device without the high temperature anneal has a 4–5 orders of magnitude lower gate leakage than that with high temperature anneal. The benefit of the low temperature fabrication process to the high-K dielectric quality has also been reported by other authors [5].

Fig. 2 shows the schematic and XTEM image of the cross-sectional SSDT structure formed by a simplified one-mask process. There is a "hole" between S/D and gate, which acts as a sidewall spacer to separate them. The "hole" is formed during the DHF dipping before the Pt or Dy deposition because the bottom layer (HfN) of the gate stack is horizontally etched by the DHF solution slightly, while the top layer (TaN) is not etched. The electrical characteristics of a PSSDT are shown in Fig. 3. It has excellent electrical performance with an $I_{on}/I_{off} \sim 10^7 - 10^8$ and a subthreshold slope of 66 mV/dec. The off current is mainly attributed to the reverse leakage of the PtSi/n-Si Schottky contact because the drain to substrate Si forms a PtSi/n-Si diode which is always reverse biased. The I–V and C–V characteristics of the PtSi/n-Si diode are shown in Fig. 4, from which the barrier height can be deduced to be 0.84 eV (I–V) and 0.86 eV (C–V), respectively, with an I–V ideality factor of 1.02 and a doping concentration (N_D) of 1.1×10^{-15} cm^{-3}. The calculated diode saturation current at zero bias is about 3.8×10^{-12} A for a diode with area of 1.0×10^{-4} cm^2, in close agreement with the transistor off current (Fig. 3(b)).

The "hole" size in Fig. 2 influences the PSSDT on current significantly. Fig. 5 shows that I_{on} at $V_{ds} = 0.05$ V and $V_g = 1.5$ V decreases from 0.18 to 0.10 mA with an increase in the DHF dipping time from 60 to 105 s. A device with DHF dipping time of 5 min reduces I_{on} by

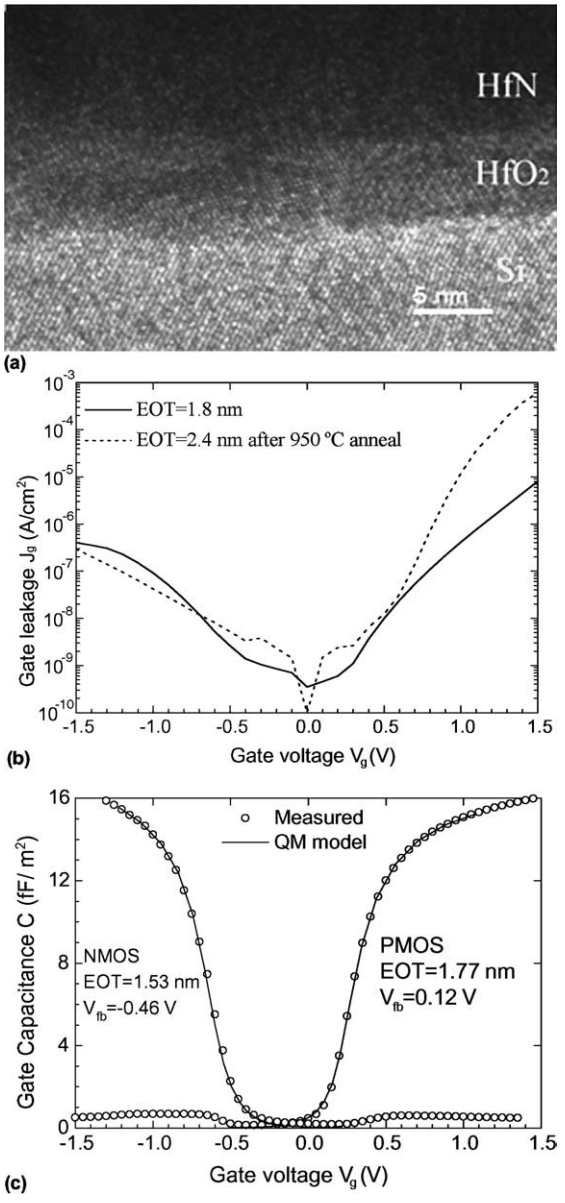

Fig. 1. HRTEM image (a), gate leakage I–V curves (b) and C–V curves (c) of the TaN/HfN/HfO_2/sub-Si MOSC structure. An additional high temperature anneal increases the gate leakage significantly.

about 3 orders of magnitude, where a big "hole" between S/D and gate is really observed in this case by TEM. For comparison, SSDT devices were also fabricated using a normal process (four-masks) with sidewall spacer thickness of 20, 50 and 100 nm, respectively. The electrical characteristics of the device with 20 nm spacer are shown in Fig. 6. Its electrical performance is similar to that fabricated by the simplified one mask process (Fig. 3) and the drain drivability decreases dramatically

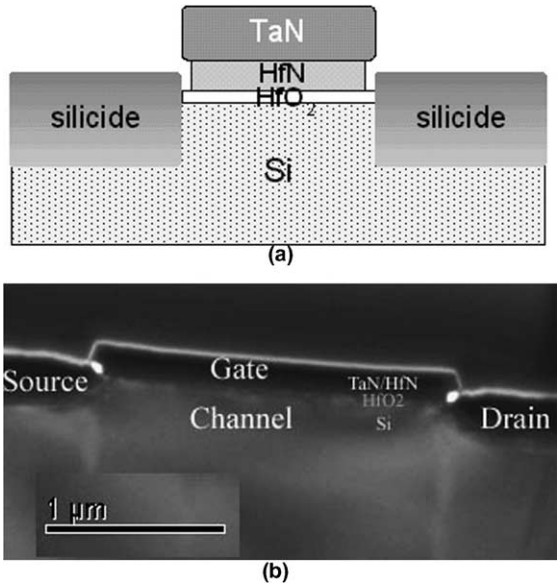

Fig. 2. Schematic (a) and XTEM image (b) of a SSDT fabricated by a simplified low temperature process. A "hole" between S/D and gate acts as a sidewall spacer to separate them.

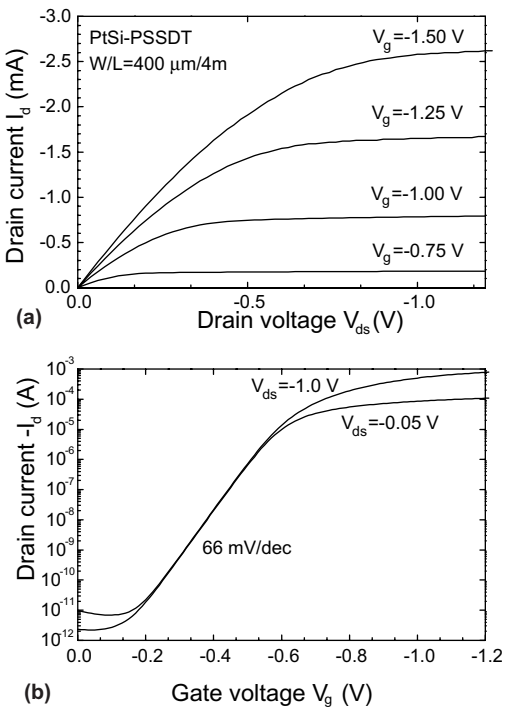

Fig. 3. I_d–V_d (a) and I_d–V_g (b) curves of PSSDT with PtSi S/D. The channel width and length are 400 and 4 μm, and EOT = 2.0 nm.

with increasing the spacer thickness. I_{on} at $V_g = V_d = -1.75$ V for the device with a 50 nm spacer is only

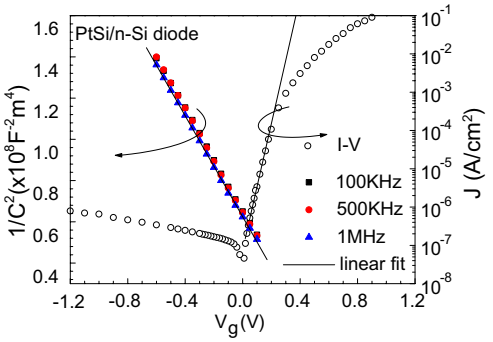

Fig. 4. I–V and C–V curves of the PtSi/n-Si diode, where the barrier heights are deduced to be 0.84 and 0.86 eV from I–V and C–V, respectively, with corresponding an ideality factor $n = 1.02$ and doping concentration $N_D = 1.1 \times 10^{15}$ cm^{-3}, close to the expected value.

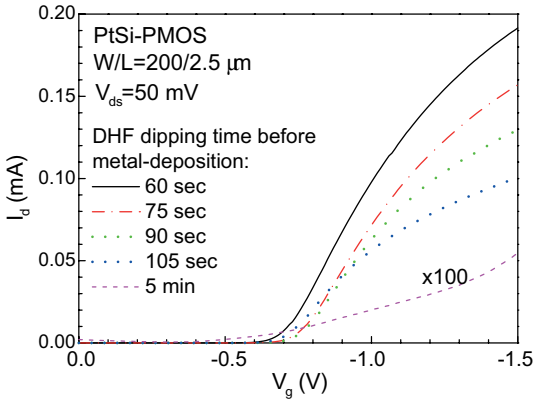

Fig. 5. Effect on the drain drivability with an increase in the DHF dipping time. The current decreases about 3 orders of magnitude after 5 min DHF dipping.

about 0.4 μA, a reduction of about 4 orders of magnitude compared with that for the device with the 20 nm spacer. A device with 100 nm spacer shows even a smaller I_{on}. In summary, the above results confirm the feasibility of our simplified low temperature process for fabrication of SSDTs.

N-SSDTs with $DySi_{2-x}$ silicide were also fabricated using the same simplified one-mask process. However, the $DySi_{2-x}$ film as well as other RE silicides produces a rougher surface because the RE silicides are not formed through the layer-by-layer mode, but by the islanded-preferred mode during the solid-state reaction with the substrate Si [12]. In practice, many small square pits in the silicide surface are observed and atomic force microscope (AFM) data show that the roughness $\langle R_{ms} \rangle$ of the $DySi_{2-x}$ is about 6.5 nm for a 1×1 μm area. No improvement of the $DySi_{2-x}$ film morphology was found

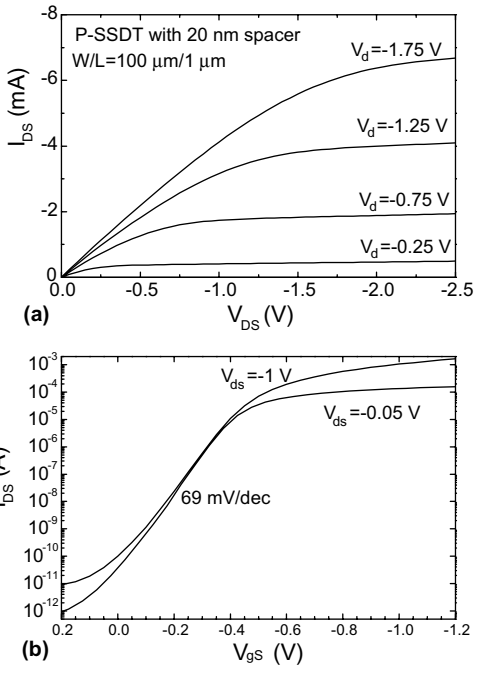

Fig. 6. I_d–V_d (a) and I_d–V_g (b) curves of PSSDT with PtSi S/D which is fabricated using a normal 4-mask process with a sidewall spacer of 20 nm. The channel width and length are 100 and 1 μm, respectively.

by using other capping layers, such as Pt, Ti, Ta, Ru and Al, etc., or by in situ vacuum anneal without a capping layer. Fig. 7 illustrates the I–V and C–V properties of the $DySi_{2-x}$/n-Si diode. The deduced barrier heights are 0.66 and 0.88 eV from I–V and C–V, respectively. The significant difference in the barrier height values and the larger than unity ideality factor ($n = 1.10$) from the I–V data imply a large barrier height inhomogeneity for the $DySi_{2-x}$/p-Si contact [14]. The reverse leakage current is

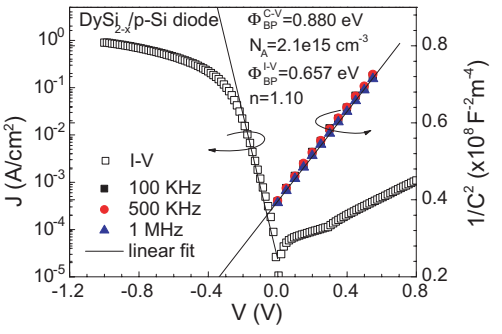

Fig. 7. I–V and C–V curves for the $DySi_{2-x}$/p-Si diode, the barrier heights are deduced to be 0.66 and 0.88 eV from I–V and C–V, respectively, with corresponding an ideality factor $n = 1.10$ and doping concentration $N_A = 2.1 \times 10^{15}$ cm^{-3}.

much larger than that for the PtSi/n-Si contact and increases faster with increasing reverse bias voltage, showing the poor rectifying property of the $DySi_{2-x}$/p-Si contact. The transistor properties for the NSSDT are shown in Fig. 8. The drain off current is about 3 orders of magnitude larger than that of PSSDT, resulting in an I_{on}/I_{off} ratio of about 10^5 at the low drain bias region ($V_{ds} = 0.2$V). Moreover, the subthreshold curve has two slopes, ~80 mV/dec at $V_g < 0.23$ V and ~340 mV/dec at $V_g > 0.23$ V. These phenomena can be attributed to the relatively large electron barrier height of $DySi_{2-x}$ and the rough surface morphology. The key point for the development of the N-SSDT is to reduce the electron barrier height and to improve the silicide quality.

It was reported that the RE silicide formed by co-evaporation of Si and RE metal has a good surface morphology [15]. However, it cannot be used in our process because it is not compatible with a self-aligned S/D fabrication process (the silicide above gate cannot be selectively etched). For our process, we find that adding a thin intermediate Ge layer can improve the Dy silicide film morphology significantly. No square pits were found on the surface of $DySi_{2-x}$ formed by the solid-state reaction of the HfN/Dy/Ge/sub-Si multilayer. The deposited amorphous Ge layer may obstruct the crystallization of $DySi_{2-x}$ during its growth. Fig. 9 shows the I–V curves of the $DySi_{2-x}$/p-Si diodes with three different thickness of Ge intermediate layer ~1, ~6 and ~30 nm. For devices with a thin Ge intermediate layer, the barrier height is close to the reported value (0.74 eV [11]) with the ideality factor near 1, implying an improvement of the Schottky contact with the intermediate Ge layer. However, a thick intermediate Ge layer

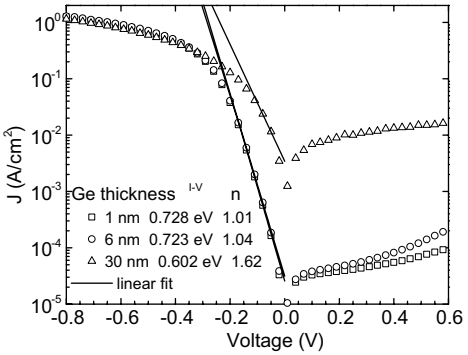

Fig. 9. I–V curves of $DySi_{2-x}$/gp-Si diode formed from the solid-state reaction of HfN/Dy/Ge/sub-Si multilayer with different thickness of intermediate Ge layer (~1, ~6 and ~30 nm) where a thinner Ge intermediate layer shows better rectifying.

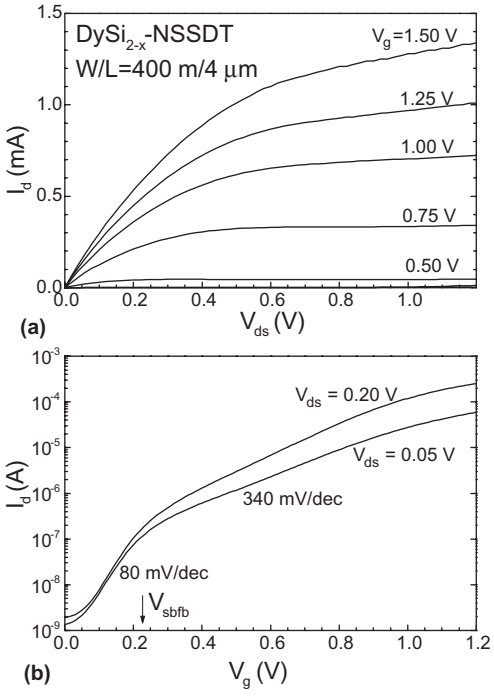

Fig. 8. I_d–V_d (a) and I_d–V_g (b) curves of NSSDT with $DySi_{2-x}$ S/D. The channel width and length are 400 and 4 μm, respectively, and EOT = 1.5 nm. The subthreshold slope is $S = 80$ mV/dec at $V_g < 0.23$ V and 340 mV/dec at $V_g > 0.23$ V.

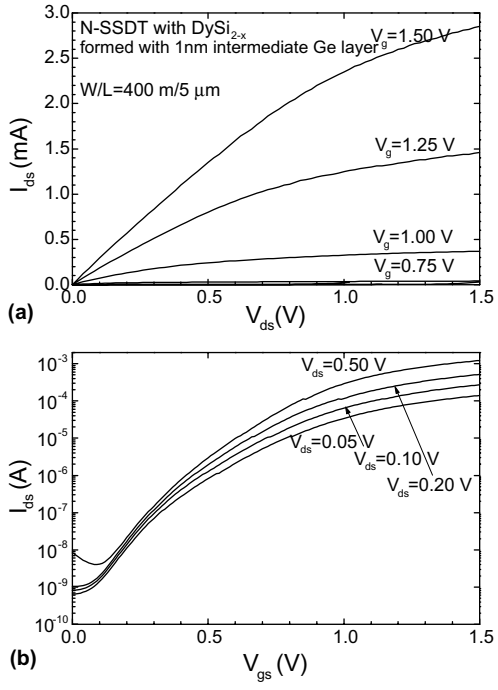

Fig. 10. I_d–V_d (a) and I_d–V_g (b) curves of NSSDT with $DySi_{2-x}$ S/D, which was formed with an intermediate Ge layer (~1 nm). The channel width and length are 400 and 5 μm, respectively, the device has a lower I_{off} and a higher I_{on} as compared to Fig. 8.

(~30 nm) will degrade the diode performance significantly as seen in Fig. 9. In addition, the sheet resistance of the silicide film increases significantly with an increase in the Ge thickness because the Ge intermediate layer delays the reaction of Dy and Si. Therefore, the intermediate Ge thickness should be kept small and optimized. The electrical performance of NSSDT with $DySi_{2-x}$ formed by ~1 nm intermediate Ge layer is shown in Fig. 10. It has a smaller I_{off} and a higher I_{on} than those of the NSSDT without the Ge intermediate layer (Fig. 8). The total I_{on}/I_{off} ratio at $V_{ds} = 0.2V$ improves about 5–6 times. Further studies on the detailed effects of Ge on $DySi_{2-x}$ are proceeding.

4. Conclusion

A simplified low temperature process is reported integrating the use of a high-K gate dielectric, a metal gate and a Schottky barrier silicided S/D structure. A "hole" which is formed by the side etching of the HfN layer during DHF dipping acts as a sidewall spacer to separate the S/D and gate. PSSDTs with PtSi S/D have shown excellent electrical performance, similar to devices fabricated by a normal process with an optimized sidewall thickness. For NSSDTs with $DySi_{2-x}$ S/D, the relatively large electron barrier height (Φ_n) and the poor silicide surface morphology result in worse electrical performance than that of the PSSDT. Adding a thin intermediate Ge layer can improve the $DySi_{2-x}$ silicide film, as well as the N-SSDT electrical performance.

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