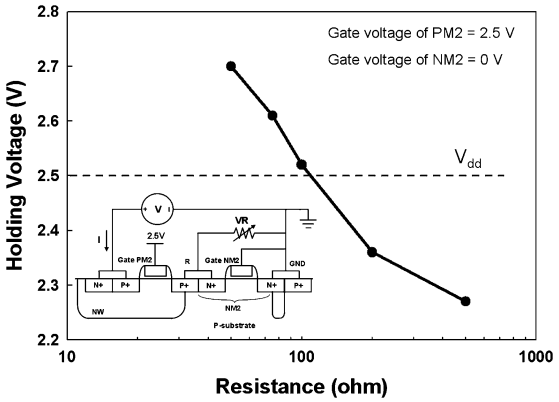

Fig. 3. Dependence of the shunt resistance (VR) on the holding voltage of DHVSCR. The measurement setup is shown in the inset.

still high enough for on-chip ESD protection design without latch-up issues.

V. Conclusion

The proposed DHVSCR device has been successfully verified in a 0.25-μm/2.5-V fully salicided CMOS process. From the experimental results, the holding voltage of DHVSCR can be adjusted by changing the gate bias of the embedded nMOS and pMOS in DHVSCR structure to avoid latch-up issue during normal circuit operating condition. The proposed DHVSCR device with suitable ESD-detection circuit can be used in I/O pads, power-rail, and whole-chip ESD protection circuits. For whole-chip ESD protection design, all DHVSCR devices can be controlled by a common ESD-detection circuit to save the layout area of ESD-detection circuit for every pin.

References

[1] A. Chatterjee and T. Polgreen, "A low-voltage triggering SCR for on-chip ESD protection at output and input pads," *IEEE Electron Device Lett.*, vol. 12, pp. 21–22, Jan. 1991.

[2] M.-D. Ker, C.-Y. Wu, and H.-H. Chang, "Complementary-LVTSCR ESD protection circuit for submicrometer CMOS VLSI/ULSI," *IEEE Trans. Electron Devices*, vol. 43, pp. 588–598, Apr. 1996.

[3] M.-D. Ker, "ESD protection for CMOS ASIC in noisy environments with high-current low-voltage triggering SCR devices," in *Proc. IEEE Int. ASIC Conf. and Exhibits*, 1997, pp. 283–286.

[4] M.-D. Ker and H.-H. Chang, "How to safely apply the LVTSCR for CMOS whole-chip ESD protection without be accidentally triggered on," in *Proc. EOS/ESD Symp.*, 1998, pp. 72–85.

[5] G. Notermans, F. Kuper, and J. M. Luchies, "Using an SCR as ESD protection without latch-up danger," *Microelectron. Reliab.*, vol. 37, pp. 1457–1460, 1997.

[6] J. Z. Chen, T. A. Vrotsos, and Y.-S. Chang, "Tunable Holding Voltage SCR ESD Protection," US Patent 6 172 404, Jan. 2001.

[7] M.-D. Ker, "Lateral SCR devices with low-voltage high-current triggering characteristics for output ESD protection in submicron CMOS technology," *IEEE Trans. Electron Devices*, vol. 45, pp. 849–860, Apr. 1998.

[8] ——, "ESD protection for CMOS output buffer by using modified LVTSCR devices with high trigger current," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1293–1296, Aug. 1997.

[9] M. Markus, C. Russ, K. Verhaege, J. Armer, P. Jozwiak, and R. Mohn, "High holding current SCR's (HHI-SCR) for ESD protection and latch-up immune IC operation," in *Proc. EOS/ESD Symp.*, 2002, pp. 10–17.

[10] C.-S. Lai, M.-H. Liu, S. Su, and T.-C. Lu, "A novel SCR ESD protection structure with low-loading and latchup immunity for high speed I/O pads," in *Proc. Int. Symp. VLSI Technology, Systems, Applications*, 2003, pp. 80–83.

[11] Z.-P. Chen and M.-D. Ker, "Dynamic holding voltage SCR (DHVSCR) device for ESD protection with high latch-up immunity," in *Proc. Int. Conf. Solid State Devices and Materials*, 2003, pp. 160–161.

[12] R. R. Troutman, *Latchup in CMOS Technology: The Problem and Its Care*. Norwell, MA: Kluwer, 1986.

[13] A. Bandyopadhyay, P. R. Verma, A. B. Bhattacharyya, and M. J. Zarabi, "LATCHSIM-a latch-up simulator in VLSI CAD environment for CMOS and BiCMOS circuits," in *Proc. IEEE Int. Conf. VLSI Design*, 1994, pp. 339–342.

[14] M. R. Simpson, "Analysis of negative differential resistance in the *I–V* characteristics of shorted-anode LIGBTs," *IEEE Trans. Electron Devices*, vol. 38, pp. 1633–1640, July 1991.

[15] M.-D. Ker, H.-H. Chang, and C.-Y. Wu, "A gate-coupled PTLSCR/NTLSCR ESD protection circuit for deep-submicrometer low-voltage CMOS ICs," *IEEE J. Solid-State Circuits*, vol. 32, pp. 38–51, Aug. 1997.

[16] M.-D. Ker and H.-H. Chang, "Novel cascade NLSCR/PLSCR design with tunable holding voltage for safe whole-chip ESD protection," in *Proc. IEEE Custom Integrated Circuit Conf.*, 1998, pp. 541–544.

A Comprehensive Study on the FIBL of Nanoscale MOSFETs

Bing-Yue Tsui and Li-Feng Chin

***Abstract*—Fringing-induced barrier lowering (FIBL) effect on nanoscale MOSFET is comprehensively examined. It is observed that by combining stack gate dielectric, conductive spacer, short sidewall spacer, and minimum gate/drain (G/D) overlap, the I_{off} with a dielectric constant of (k) 100 is only 1.6 times higher than that with $k = 3.9$ when the gate length is 25 nm. The fully depleted silicon-on-insulator device shows even better FIBL immunity. It is concluded that although the FIBL effect can not be eliminated, it would not an issue beyond the 45-nm technology node.**

***Index Terms*—Fringing-induced barrier lowering (FIBL), high dielectric constant material, MOSFET, silicon-on-insulator (SOI), stack gate dielectric.**

I. Introduction

Silicon dioxide ($\mathrm{SiO_2}$) has been used as the gate dielectric of CMOS devices for several decades and as device dimensions scale down, the thickness of $\mathrm{SiO_2}$ must be reduced to keep sufficient current driving capability. However, when the thickness of $\mathrm{SiO_2}$ becomes thinner than 3 nm, direct tunneling current increases dramatically [1]. Although many high dielectric constant (high-κ) materials have been proposed to solve this problem [2]–[10], a side effect called fringing-induced barrier lowering (FIBL) arising from the use of high-κ gate dielectric is a serious problem [11]–[16]. The electrical field originating at the drain penetrates into the channel through the high-κ dielectric and suppresses the barrier height from source to channel. Therefore, the degradation of off-state current (I_{off}) limits the allowable κ value of the gate dielectric.

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Several investigations have been performed to understand the effect of FIBL on the device and circuit performance [11]–[18]. However, current knowledge on FIBL is still insufficient. The above studies simulated FIBL with different effective oxide thicknesses (EOT), gate lengths (L_g), junction depths, and/or spacer lengths ($L_{\rm sp}$). Although several orders of magnitude increase in $I_{\rm off}$ due to FIBL have been reported, there has also been a report of only a few times increase in $I_{\rm off}$ [11], [13], [15]. Furthermore, the shortest gate length studied in the literature is 50 nm [13], [18], but it is known that the high-κ dielectric will not be used before the 45-nm technology node [19].

In this brief, the effect of device structure parameters on FIBL with L_g down to 25 nm is desirable and the impact of a high-κ dielectric under a spacer is re-evaluated. The effect of FIBL on silion-on-insulator (SOI) device is also investigated in a similar way.

II. Simulation Procedure

This brief uses commercial SUPREME and MEDICI programs to generate a typical device structure with simple shallow source/drain junction was generated [20], [21]. In most cases, the spacer length was set to be equal to the gate length. Since the shortest L_g in this work is 25 nm, the doping profiles of the 25-nm device were carefully adjusted so that the threshold voltage ($V_{\rm th}$) was 0.25 V and the $I_{\rm off}$ at $k = 3.9$ was 3×10^{-7} A/μm at a drain voltage of 1 V. This device is called the 25-nm reference device. Poly-depletion, quantum-effect, impact ionization, energy balance, and channel surface scattering were all considered. Five κ values for the gate dielectric were studied, including 3.9, 15, 25, 50, and 100. The channel width and effective oxide thickness were fixed at 1 μm and 1 nm, respectively. For the fully depleted SOI devices, the thickness of Si layer was 50 nm and the doping profiles were identical to those used for bulk devices.

III. Results and Discussion

The effect of L_g was examined first. With identical doping conditions and $L_{\rm sp}$, the $I_{\rm off}$ degradation increased upon decreasing the gate length and increasing the κ value. The increase in $I_{\rm off}$ when the κ value increased from 3.9 to 100 was less than one decade, even though the L_g is only 25 nm. It seems that the FIBL effect does not degrade $I_{\rm off}$ as seriously as those reported previously.

The impact of a high-κ dielectric under a spacer was also examined. It was observed that as long as the κ value is lower than 25, the FIBL effect is not serious and the $I_{\rm off}$ ratio between 25-nm devices with and without the high-κ dielectric under an SiO_2 spacer is only 1.3. This result indicates that it is not necessary to remove the high-κ dielectric immediately after gate patterning if the κ value is lower than 25 and there are no special issues, such as contamination or parasitic capacitance.

Fig. 1 shows the simulated equal potential contour of the 25-nm reference device with $k = 100$. It can be observed that most of the fringing field lines which originate from the drain region out of spacer and under a spacer tend to terminate at the gate electrode. The main fringing field resulting in barrier lowering originates from the gate/drain (G/D) overlap region. Since the fringing field originates from the G/D overlap region, FIBL should be sensitive to the length of overlap region ($L_{\rm ov}$). The $L_{\rm ov}$ in Fig. 1 is 1 nm. To increase the $L_{\rm ov}$ while maintaining the same source/drain doping profile and similar device performance, the gate structure of the 25-nm reference device was removed. Then, the gate structure with $L_g = 50$ nm was reconstructed so that the $L_{\rm ov}$ became 13.5 nm. Fig. 2 shows that the $I_{\rm off}$ degradation of the device with $L_{\rm ov} = 13.5$ nm is one order of magnitude higher than that with $L_{\rm ov} = 1$ nm. Since the $L_{\rm ov}$ decreases upon scaling down the design rule to control the short channel effect, the degradation of $I_{\rm off}$ due to FIBL effect could be relaxed due to the short $L_{\rm ov}$. The different $L_{\rm ov}$ may explain the wide variation of $I_{\rm off}$ degradation in the previous literature.

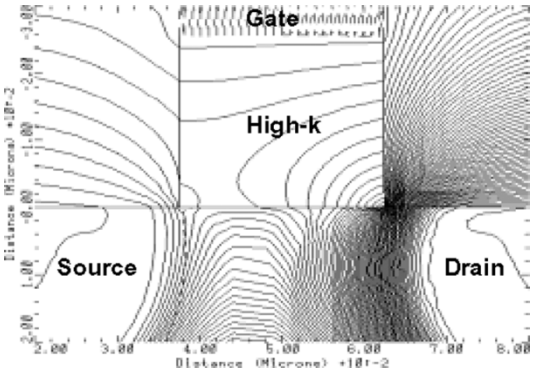

Fig. 1. Simulated equal potential contour of the 25-nm reference device with $k = 100$, EOT = 1 nm, and $L_{\rm sp} = 25$ nm. The gate, source, and substrate electrodes are all grounded and the drain electrode is biased at 1 V.

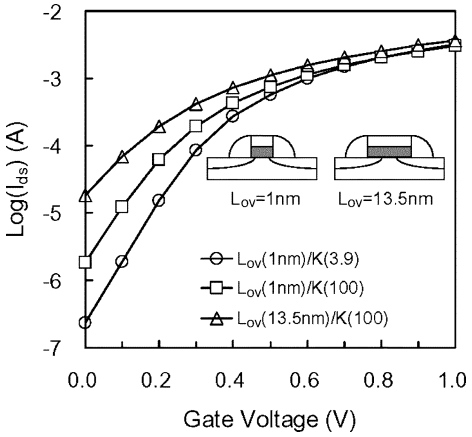

Fig. 2. Simulated *I–V* characteristics of the 25-nm devices with various $L_{\rm ov}$ and κ values.

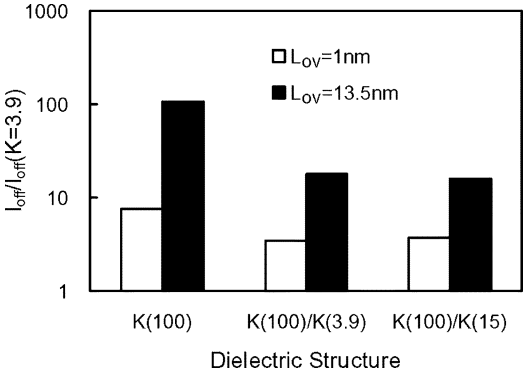

Fig. 3. FIBL-induced $I_{\rm off}$ degradation of the 25-nm devices with various gate dielectric structures and various $L_{\rm ov}$.

In the real gate structure, it is difficult to avoid a buffer layer or interfacial layer between Si channel and high-κ layer. Fig. 3 compares the effect of the buffer layer κ value. The EOT of the buffer layer is fixed at 0.3 nm and the total EOT of the gate dielectric is fixed at 1 nm. The κ value of the high-κ layer is 100. It can be observed that the FIBL-induced $I_{\rm off}$ degradation can be reduced by 50% using a stack gate dielectric. It is also observed that when $L_{\rm ov}$ is 1 nm, a κ value

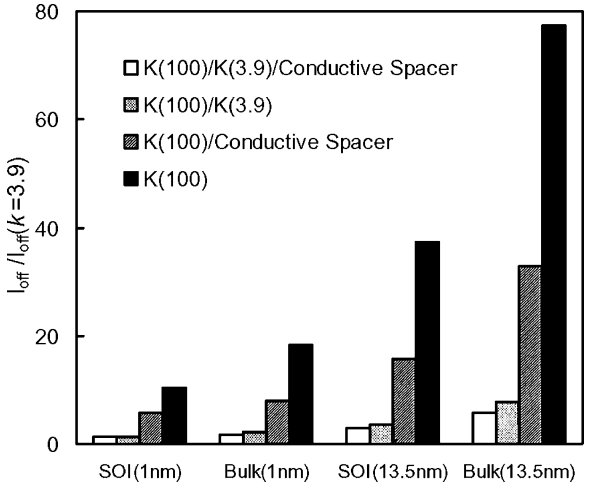

Fig. 4. FIBL-induced $I_{\rm off}$ degradation on SOI and bulk devices.

for the buffer layer of 3.9 or 15 results in almost identical $I_{\rm off}$. However, when $L_{\rm ov} = 13.5$ nm, a buffer layer with higher κ value results in lower $I_{\rm off}$. Using SiO_2 as a buffer layer, because the thickness is only 0.3 nm, the fringing field can penetrate the SiO_2 layer and enter the high-κ layer easily. The physical thickness of a buffer layer with $k = 15$ is 1.15 nm, so that less fringing field enters the upper high-κ layer. It is thus, concluded that the buffer layer at the high-k/Si interface can relax the FIBL effect regardless of whether it is oxide or silicate.

It has been reported that SOI devices, especially fully depleted SOI devices, have better immunity to the FIBL effect [15], [16]. Since the SOI devices would be the mainstream beyond the 45-nm technology node, the FIBL induced $I_{\rm off}$ degradation on SOI and bulk devices are compared. The L_g and $L_{\rm sp}$ are 25 nm and the EOT is 1 nm for both SOI and bulk devices. Since the fringing field terminating at the gate electrode does not play a role in $I_{\rm off}$ degradation, the efficiency of a conductive spacer is also considered in this part. Fig. 4 confirms that the $I_{\rm off}$ degradation of an SOI device is smaller than that of the bulk device. It is also clear that the conductive spacer can relax the $I_{\rm off}$ degradation, and longer $L_{\rm ov}$ results in more severe $I_{\rm off}$ degradation. These trends for SOI device are consistent with those of the bulk device. If the $L_{\rm ov}$ can be controlled to be 1 nm, a simple stack gate dielectric scheme can reduce the $I_{\rm off}$ degradation factor to two, even if the κ value is 100. It is expected that the novel device structures such as ultrathin body SOI and multiple gate SOI can further reduce the $I_{\rm off}$ degradation.

IV. Conclusion

In this brief, TCAD tools were used to investigate the FIBL effect of 25-nm devices. The key factor to affect the FIBL effect is the gate to drain overlap length. Most of the fringing field originates from this region. Since the overlap length must be reduced to control short channel effect, it is expected that the FIBL effect can be further relaxed. It is known that a stack gate dielectric scheme with buffer layer ($k < 15$) between the high-κ dielectric and the Si substrate can relax the FIBL effect. A conductive spacer is another effective method to reduce the FIBL effect but the process is more complicated. A fully depleted SOI device shows better resistance to FIBL-induced $I_{\rm off}$ degradation. It is expected that the ultrathin body SOI and multiple gate SOI devices will exhibit even better FIBL effect resistance. Therefore, it is concluded that although the FIBL effect can not be eliminated with suitable device structure, its impact on device performance is diminished for the sub-45-nm technology node and beyond.

References

[1] S. H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, "Quantum-mechanical modeling of electron tunneling current from the inversion layer of ultrathin oxide nMOSFETs," *IEEE Electron Device Lett.*, vol. 18, pp. 209–211, May 1997.

[2] J. L. Autran, R. Device, C. Chaneliere, and B. Balland, "Fabrication and characterization of Si-MOSFETs with PECVD amorphous Ta_2O_5 gate insulator," *IEEE Electron Device Lett.*, vol. 18, pp. 447–449, Sept. 1997.

[3] J. H. Lee, K. Koh, N. I. Lee, M. H. Cho, Y. K. Ki, J. S. Jeon, K. H. Cho, H. S. Shin, M. H. Kim, K. Fujihara, H. K. Kang, and J. T. Moon, "Effect of polysilicon gate on the flatband voltage shift and mobility degradation for ALD-$\mathbf{Al_2O_3}$ gate dielectric," in *IEDM Tech. Dig.*, 2000, pp. 645–648.

[4] A. Chin, Y. H. Wu, S. B. Chen, C. C. Lias, and W. J. Chen, "High quality La_2O_3 and Al_2O_3 gate dielectrics with equivalent oxide thickness 5–10 A," in *IEEE Symp. VLSI Tech. Dig.*, 2001, pp. 13–14.

[5] R. Choi, K. Onishi, S. K. Chang, H. J. Cho;, Y. H. Kim, S. Krishnan, M. S. Akbar, and J. C. Lee, "Effects of deuterium anneal on MOSFETs with HfO_2 gate dielectrics," *IEEE Electron Device Lett.*, vol. 24, pp. 144–146, Feb. 2003.

[6] C. H. Choi, T. S. Jeon, R. Clark, and D. L. Kwong, "Electrical properties and thermal stability of CVD HfOxNy gate dielectric with poly-Si gate electrode," *IEEE Electron Device Lett.*, vol. 24, pp. 215–217, Apr. 2003.

[7] W. Zhu, T. P. Ma, T. Tamagawa, Y. Di, J. Kim, R. Carruthers, M. Gibson, and T. Furukawa, "HfO_2 and HfAlO for CMOS: thermal stability and current transport," in *IEDM Tech. Dig.*, 2001, pp. 463–466.

[8] A. Morioka, H. Watanabe, M. Miyamura, T. Tatsumi, M. Saitoh, T. Ogura, T. Iwamoto, T. Ikarashi, Y. Saito, Y. Okada, Y. Mochiduki, and T. Mogami, "High mobility MISFET with low trapped charge in HfSiO films," in *IEEE Symp. VLSI Tech. Dig.*, 2003, pp. 165–166.

[9] W. J. Qi, R. Nieh, B. H. Lee, K. Onishi, and L. Kang, "Performance of MOSFETs with ultrathin ZrO_2 and Zr silicate gate dielectrics," in *IEEE Symp. VLSI Tech. Dig.*, 2000, pp. 15–16.

[10] Z. J. Luo, T. P. Ma, E. Cartier, M. Copel, T. Tamagawa, and B. Halpern, "Ultrathin ZrO_2 (or silicate) with high thermal stability for CMOS gate applications," in *IEEE Symp. VLSI Tech. Dig.*, 2001, pp. 135–136.

[11] G. C. F. Yeap, S. Krishnan, and M. R. Lin, "Fringing-induced barrier lowering (FIBL) in sub-100-nm MOSFETs with high-$\boldsymbol{\kappa}$ gate dielectrics," *Electron. Lett.*, vol. 34, no. 11, pp. 1150–1152, 1998.

[12] C. H. Lai, L. C. Hu, H. M. Lee, L. J. Do, and Y. C. King, "New stack gate insulator structure reduce FIBL effect obviously," in *Proc. VLSI-TSA*, 2001, pp. 216–219.

[13] D. L. Kencke, W. Chen, H. Wang, S. Mudanai, Q. Ouyang, A. Tasch, and S. K. Banerjee, "Source-side barrier effects with very high-$\boldsymbol{\kappa}$ dielectrics in 50-nm Si MOSFETs," in *Proc. Dev. Res. Conf.*, 1999, pp. 22–23.

[14] Y. Kamata, M. Ono, and A. Nishiyama, "Influences of elevated extension structure on the performance of MISFETs with high-$\boldsymbol{\kappa}$ gate dielectric," in *Proc. Int. Workshop Gate Insulator*, 2001, pp. 206–209.

[15] S. C. Lin and J. B. Kuo, "Fringing-induced barrier lowering (FIBL) effects of 100-nm FD SOI NMOS devices with high permittivity gate dielectrics and LDD/sidewall oxide spacer," in *Proc. Int. SOI Conf.*, 2002, pp. 93–94.

[16] X. Liu, S. Lou, Z. Xia, D. Guo, H. Zhu, J. Kang, and R. Han, "Characteristics of different structure sub-100-nm MOSFETs with high-$\boldsymbol{\kappa}$ gate dielectrics," in *Proc. 6th Int. Conf. Solid-State Integrated-Circuit Technology*, vol. 1, 2001, pp. 333–336.

[17] N. R. Mohapatra, M. P. Desai, S. G. Narendra, and V. R. Rao, "The effect of high-$\boldsymbol{\kappa}$ gate dielectrics on deep submicrometer CMOS device and circuit performance," *IEEE Trans. Electron Devices*, vol. 49, pp. 826–831, May 2002.

[18] N. R. Mohapatra, M. P. Desai, and V. R. Rao, "Detailed analysis of FIBL in MOS transistors with high-$\boldsymbol{\kappa}$ gate dielectrics," in *Proc. 16th Int. Conf. VLSI Design*, 2003, pp. 99–104.

[19] International Technology Roadmap for Semiconductors, Semiconductor Industry Association, 2003.

[20] *User's Manual for MIDICI Two-Dimensional Device Simulation*, Synopsis Co., 2003.

[21] *User's Manual for SUPREM Two-Dimensional Process Simulation*, Synopsis Co., 2003.