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Comparison of oxide breakdown progression in ultra-thin oxide silicon-on-insulator and bulk metal-oxide-semiconductor field effect transistors

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Enhanced oxide breakdown progression in ultra-thin oxide silicon-on-insulator *p*-type metal-oxide-semiconductor field-effect transistors is observed, as compared to bulk devices. The enhanced progression is attributed to the increase of hole stress current resulting from breakdown induced channel carrier heating in a floating-body configuration. Numerical analysis of hole tunneling current and hot carrier luminescence measurement are performed to support our proposed theory. This phenomenon is particularly significant to the reliability of devices with ultra-thin oxides and low operation gate voltage. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1776640]

I. INTRODUCTION

The aggressive scaling of advanced complementary metal-oxide-semiconductor (CMOS) field effect transistors (MOSFETs) has pushed the gate oxide thickness towards its limit in terms of reliability.[1–4] In ultra-thin gate oxide MOSFETs, oxide breakdown (BD) has been shown to evolve in a continuous manner from initial stages to final shorting.[5–7] Previous study has shown that a small increase in gate leakage due to oxide BD does not disrupt circuit operation, and the failure criterion should be changed to a higher level of gate leakage.[8,9] Therefore, the oxide failure time is determined by BD hardness involved in a progressive process, or in other words, by BD evolution rate. Presently, the silicon-on-insulator (SOI) technology has emerged to be a candidate for advanced CMOS technology for its higher performance. The BD progression in conventional bulk CMOS devices[10–12] has been widely investigated. In this paper, we will investigate the influence of floating body effect on BD progression in partially depleted (PD) *p*-type SOI MOSFETs.

Several concerns of hard breakdown evolution in ultra-thin oxides have been proposed.[7–14] Monsieur *et al.*[7] reported that for low gate stress bias, the defect generation rate being very low, the degradation of the BD conduction path becomes macroscopic and can last thousands of seconds even in the case of accelerated test. Linder *et al.*[9] showed that the growth of BD current could be exponentially dependent on gate bias, oxide thickness, and any other parasitics, such as inversion layer resistances, altering the observed growth rate drastically. Alam *et al.*[13] indicated that circuits do continue to operate after the first soft breakdown (SBD), and suggested that the standard reliability specification is too restrictive, and should be redefined, particularly for pMOS devices. In ultra-thin oxide pMOSFETs, enhanced gate oxide BD growth rate was observed with a negative substrate bias.[14] Furthermore, the floating body configuration of partially depleted SOI CMOS may result in a nonzero body voltage due to various body charging mechanisms[15–18] and thus affects ox-

ide BD evolution. The objective of this paper is therefore to investigate floating body effect on BD progression rate. A model based on breakdown induced channel carrier heating will be proposed to explain the observed phenomenon.

II. DEVICES AND EXPERIMENT

The devices in this work were made with an optimized 0.13 μm CMOS process on *p*-type SOI wafer and have a gate length of 0.5 μm, a gate width of 2 μm, and an oxide thickness of 1.6 nm. The gate oxide was grown with rapid plasma nitridation process. The test devices have an H-gate structure with an additional contact to facilitate the measurement of the body current and voltage. In this paper, all devices were stressed at constant gate voltage with the source and drain grounded. Figure 1 shows typical BD evolution in a 1.4 nm oxide and a 2.5 nm oxide bulk pMOSFETs. In the 1.4 nm gate oxide pMOSFET, oxide BD is evolved in a progressive way, and the gate leakage current increases gradually with stress time. As a contrast, the 2.5 nm oxide pMOSFET exhibits an abrupt jump in gate leakage current after BD. Since a slight gate leakage increases due to oxide BD is considered to be nondestructive for circuit operation,[8] we define oxide breakdown time t_{BD} and device fail time t_{fail}
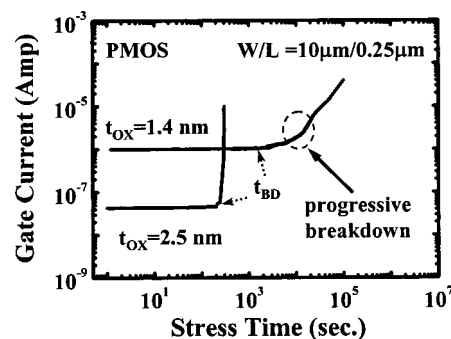

FIG. 1. Comparison of breakdown behavior in a 1.4 nm oxide pMOSFET and in a 2.5 nm oxide pMOSFET. The stress gate voltage is −3 V for the 1.4 nm oxide and −4.5 V for the 2.5 nm oxide. t_{BD} denotes the onset time of oxide breakdown.

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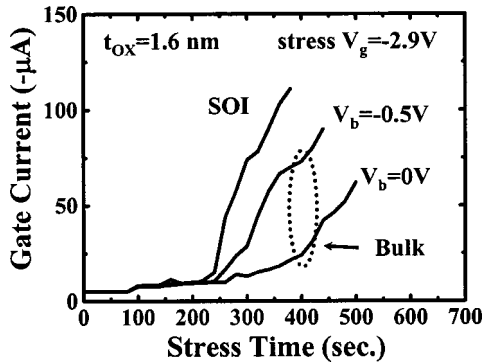FIG. 2. Oxide breakdown progression in bulk and SOI pMOSFETs. The stress gate bias is −2.9 V and temperature is 125 °C.

as the time when the gate leakage current reaches 1.5 times and 15 times its prestress value, respectively.

III. RESULT AND DISCUSSION

A. A shorter t_{fail} in SOI pMOSFETs

Figure 2 shows the gate leakage current evolution with stress time at a stress gate voltage of $V_g = -2.9$ V for various applied substrate biases (V_b) in pMOSFETs. The oxide t_{BD} is almost the same for different substrate biases. This can be understood because oxide defect generation rate is dependent on injected charge energy and fluence during stress,[19–22] regardless of applied substrate bias. After the onset of BD, the BD growth rate exhibits an apparent dependence on substrate bias. A forward substrate bias can significantly enhance BD growth rate. It should be noted that the SOI device with floating-body configuration has the worst BD progression rate in Fig. 2. The statistic Weibull distributions of oxide t_{BD} and t_{fail} for SOI (floating substrate) and bulk (grounded substrate) pMOSFETs are plotted in Fig. 3. Although the floating substrate configuration does not affect t_{BD}, it does cause a two times shorter t_{fail} than in bulk pMOSFETs.

B. Mechanism of enhanced BD progression in SOI

The floating body configuration of SOI devices may result in a small forward body voltage due to various body
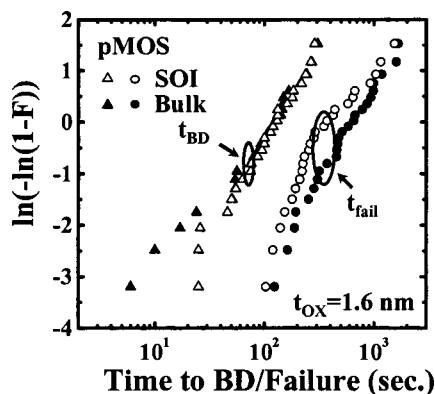

FIG. 3. The Weibull plots of t_{BD} and t_{fail} distribution for 1.6 nm oxide SOI and bulk pMOSFETs. The stress gate bias is −2.9 V and the temperature is 125 °C. t_{BD} and t_{fail} are defined as the time for gate current to reach 1.5 times and 15 times its prestress value, respectively.
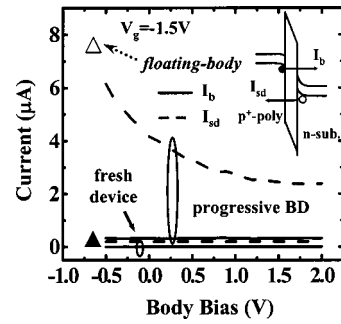

FIG. 4. The V_b dependence of pre-BD and post-BD electron currents I_b and hole currents I_{sd} at $V_g = -1.5$ V. Distinct V_b dependence of the post-t_{BD} I_{sd} is noted. The floating body configuration corresponds to a body voltage of approximately −0.65 V. The inset illustrates carrier flow in a pMOSFET at a negative gate bias.

charging processes. In an ultra-thin oxide pMOSFET, the gate stress current may have comparable electron and hole components at a negative gate bias. To analyze the polarity of dominant stress current in a pMOSFET, a charge separation technique is utilized to measure electron stress current and hole stress current. The inset of Fig. 4 illustrates the carrier flow at a negative gate bias, I_b denotes electron current and comes from valance-band electron tunneling from the gate electrode. I_{sd} stands for hole tunneling current from the inverted channel. The substrate bias dependence of electron current and hole current before and after t_{BD} is shown in Fig. 4. Note that the electron and hole currents in a fresh device are independent of substrate bias. Interestingly, the post-t_{BD} hole current, unlike the pre-BD, I_b, and I_{sd}, exhibits a significant V_b dependence. Furthermore, Fig. 5 reveals that the V_b dependence of the post-t_{BD} hole current increases with BD evolution. Since the hole stress current dominates gate stress during (BD) evolution and increases with a forward body bias, the enhanced (BD) progression in a floating body configuration can be understood.

C. BD caused carrier heating

Since the post-t_{BD} electron current does not exhibit V_b dependence (Fig. 4), the possibility that the V_b dependence of the post-t_{BD} hole current is caused by the variation of effective gate-to-channel voltage resulting from V_b modulated channel resistance can be excluded. Otherwise, the post-t_{BD} I_b should have the same V_b effect as the post-
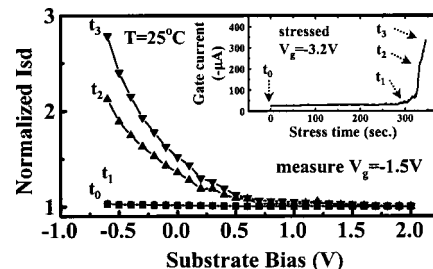

FIG. 5. The V_b dependence of the hole current I_{sd} at different stress times, $t_0, t_1, t_2,$ and t_3. I_{sd} is normalized to its value at $V_b = 2$ V. Gate current vs stress time in a stress condition of $V_g = -3.2$ V and $T = 25$ °C is shown in the inset.
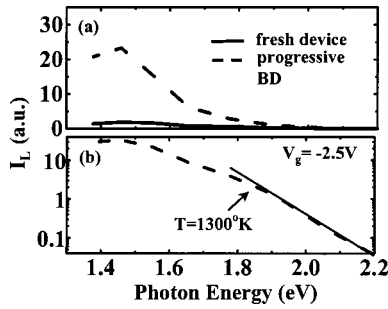
FIG. 6. Spectral distribution of light emission in a 1.4 nm oxide pMOSFET at $V_g = -2.5$ V. The extracted carrier temperature from the high-energy tail of the spectrum is around 1300 K.

t_{BD} I_{SD}. Moreover, substrate impact ionization and negative bias-temperature instability effects are also excluded because the trend of the V_b dependence is opposite.

To further investigate the origin of the V_b dependence of the post-t_{BD} hole current, we measured the spectral distribution of hot carrier light emission before and after t_{BD} (Fig. 6). The light intensity is greatly increased after oxide BD. The high-energy tail of the post-t_{BD} spectral distribution indicates the rise of the carrier temperature. Similar finding was also reported by other groups.[23] The extracted carrier temperature from the high-energy tail of the spectrum is around 1300 K [Fig. 6(b)]. There are two possible theories to explain the rise of channel carrier temperature at a BD spot. First, based on the model proposed by Rasras *et al.*,[23] the gate voltage may penetrate into the substrate after BD and causes lateral field heating of channel carriers. However, this process is unlikely here since the post-t_{BD} electron current and hole current have distinctly different V_b dependence. The second possible reason is that high-dissipated energy, released by valence electrons tunneling from the gate through the BD path, will locally produce a rise of hole temperature. A temperature range of 1000 to 2000 K was estimated in Ref. 24. Electron-hole scattering or Auger recombination is suspected to be the responsible energy transfer process.
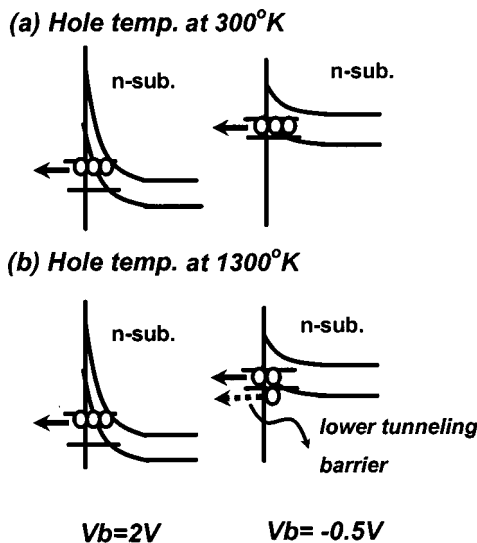

FIG. 7. Illustration of hole distribution in subbands at a hole temperature of 300 K and 1300 K. Higher carrier temperature results in a larger V_b effect.
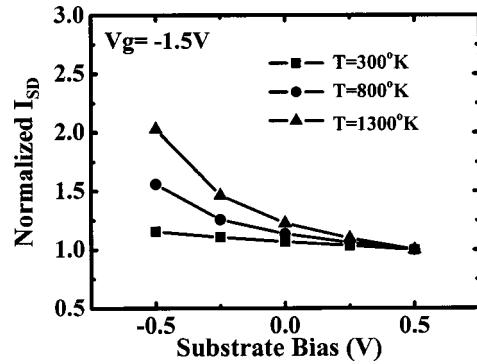

FIG. 8. Simulated substrate bias effect on hole tunneling current in a 1.6 nm oxide pMOSFET. I_{sd} is normalized to its value at $V_b = 2$ V. Simulated $V_g = -1.5$ V.

To show that the rise of hole temperature may account for the observed V_b dependence, we calculate the hole tunneling current with hole temperature at 300 K and 1300 K. In our calculation, we solve the coupled Poisson and Schrödinger equations to obtain the subband structure for the inversion holes (Fig. 7). A simple one-band effective mass approximation is used for simplicity. The hole tunneling current is calculated according to the Tsu-Esaki formula[25]

$$I_{sd} = q m_{\parallel}^* \left(\frac{1}{2\pi^2 \hbar^3} \right) k_B T \sum_n D_n (\ln\{1 + \exp[(E_n - E_f)/k_B T]\}$$
$$- \ln\{1 + \exp[(E_n - E_{f'})/k_B T]\}), \tag{1}$$

where E_f ($E_{f'}$) denotes the Fermi energy in the channel (poly gate) and D_n is the hole tunneling probability of the nth subband. m^* is the hole effective mass in Si. Other variables have their usual definitions. It should be emphasized that it is not our intention to consider detailed trap-assisted charge transport in the BD path. It is also not our intension to calculate the precise current value before and after oxide BD, since the BD area and BD caused effective oxide thinning cannot be easily determined. Instead, our purpose is to investigate the effect of hole temperature on the inversion hole distribution in different subbands and the corresponding substrate bias effect on hole tunneling current. Therefore, a simple WKB formula for direct tunneling is employed for D_n.

Our result in Fig. 8 clearly shows that the hole tunneling current exhibits a larger V_b dependence at 1300 K. The simulation can well interpret the measured V_b dependence of the

TABLE I. Calculated distribution of channel holes in the lowest three subbands. The gate bias in simulation is -1.5 V. The parameters used in simulation is $m^*(\text{Si}) = 0.67\ m_0$, $m^*(\text{SiO}_2) = 0.55\ m_0$, ϕ_h (hole barrier height at SiO$_2$ interface) = 4.25 eV, $t_{ox} = 1.6$ nm, and N_B (substrate doping) = 1×10^{18} cm^{-3}.

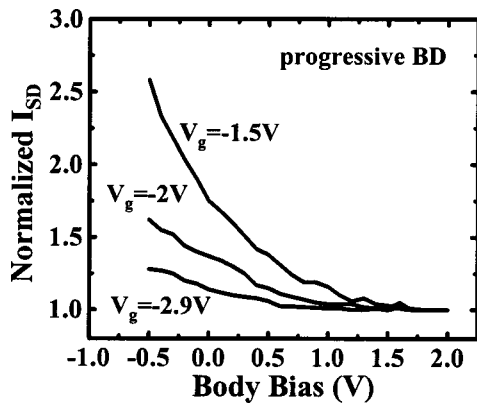| | Channel hole dist. (%) | | | |
| | 300 K | | 1300 K | |
Subband	$V_b = -0.5$	$V_b = 2$	$V_b = -0.5$	$V_b = 2$
1st	96.6	99.5	39.8	99.4
2nd	3	0.5	18	0.6
3rd	0.3	0	11.6	0

FIG. 9. Substrate bias dependence of the post-BD hole current at various gate biases. I_{sd} is normalized to its value at $V_b = 2$ V.

FIG. 11. t_{fail} (63%) vs gate stress bias for SOI and bulk pMOS devices.

post-t_{BD} I_{sd} by simply using an elevated hole temperature. The trend in Fig. 8 is similar to the measured V_b dependence in Fig. 5. To explain the temperature effect on the V_b dependence in more detail, the distribution of inversion holes in the lowest three subbands is given in Table I. At $T = 300$ K, channel holes mostly reside in the first subband no matter of V_b. At $T = 1300$ K, a large part of holes are thermally excited to higher subbands at a forward body voltage (-0.5 V), where the oxide tunneling probability is larger. Thus, a much larger hole tunneling current is obtained at negative body voltages.

SOI and bulk pMOSFETs at various gate stress biases. Accelerated BD progression is noticed in SOI samples and the trend becomes more apparent at lower gate stress biases. Figure 12 shows the range of oxide thickness and stress gate voltage, where the hole current component is dominant in a fresh device and after breakdown. For example, for an oxide thickness of 1.6 nm, hole current is dominant in stress for $V_g < 2.5$ V in a fresh device and for $V_g < 3.0$ V after BD. High-energy electron impact ionization does not need to be considered until V_g is above 3.5 V. Figure 12 also reveals that the hole current dominant region increases not only with BD progression but with decreasing oxide thickness. It implies that the floating body enhanced BD progression will become more significant as oxide thickness scales down.

IV. THE IMPACT OF GATE STRESS BIAS

From previous discussion, the V_b dependence of hole stress current was identified to be the origin of the floating-body enhanced BD progression. Now, the impact of gate stress bias scaling on the enhanced BD progression is explored. Figure 9 shows the V_b dependence of BD current at various measurement gate biases. The V_b dependence is more distinguished at a smaller gate bias. Figure 10 shows the range of the gate stress bias where hole current is dominant. The hole current dominates gate stress at small gate biases (less than ~3.0 V) and the hole component of the stress current increases during BD evolution. This result is consistent with the findings in Fig. 9 that a large V_b dependence of the post-BD stress current is obtained at smaller gate voltages. Figure 11 compares the 63% time-to-failure in
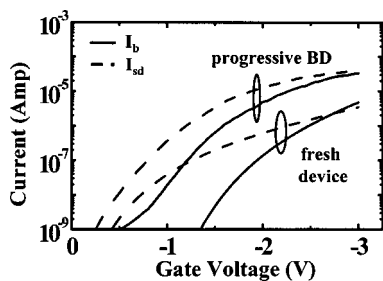
V. CONCLUSION

In ultra-thin oxide SOI pMOSFETs, breakdown progression is aggravated by a forward body bias. An enhanced post-t_{BD} gate current is observed in SOI devices due to the charging of the floating body. Numerical analysis shows that the V_b enhanced hole stress current can be explained by the increase of hole temperature at the breakdown spot. The V_b accelerated BD progression is more significant at a lower stress gate bias and for a thinner oxide.

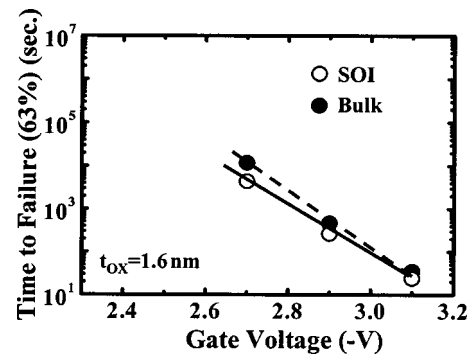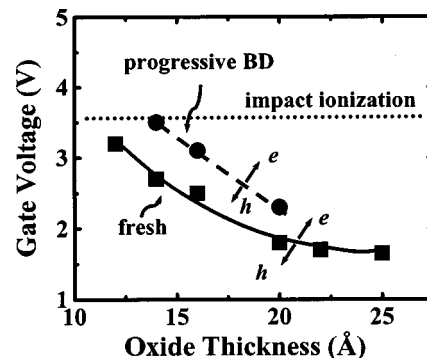FIG. 10. Gate bias dependence of electron current and hole current in a fresh pMOSFET and during progressive BD.

FIG. 12. The range of oxide thickness and stress gate voltage, where the hole current component is dominant in a fresh device and after breakdown h or e represents hole current or electron current dominant regime, respectively.

[1] E. Harari, J. Appl. Phys. **49**, 2478 (1978).

[2] I. C. Chen, S. Holland, K. K. Young, C. Chang, and C. Hu, Appl. Phys. Lett. **49**, 669 (1986).

[3] M. Houssa, T. Nigam, P. W. Mertens, and M. M. Heyns, J. Appl. Phys. **84**, 4351 (1998).

[4] E. Miranda, J. Sune, R. Rodriguez, M. Nafria, and X. Aymerich, Appl. Phys. Lett. **73**, 490 (1998).

[5] T. Hosoi, P. L. Re, Y. Kamakura, and K. Taniguchi, Tech. Dig. - Int. Electron Devices Meet. **2002**, 155.

[6] B. P. Linder, S. Lombardo, J. Stathis, A. Vayshenker, and D. Frank, IEEE Electron Device Lett. **23**, 661 (2002).

[7] F. Monsieur, E. Vincent, D. Roy, S. Bruyere, J. C. Vildeuil, G. Pananakakis, and G. Ghibaudo, Proc. Int. Reliab. Phys. Symp. ,2002, p. 45.

[8] B. Kaczer, R. Degraeve, G. Groeseneken, M. Rasras, S. Kubicek, E. Vandamme, and G. Badenes, Tech. Dig. - Int. Electron Devices Meet. **2000**, 553.

[9] B. P. Linder, J. H. Stathis, D. J. Frank, S. Lombardo, and A. Vayshenker, Proc. Int. Reliab. Phys. Symp. ,2003, p. 402.

[10] E. Wu, E. Nowak, J. Aitken, W. Abadeer, L. K. Han, and S. Lo, Tech. Dig. - Int. Electron Devices Meet. **1998**, 187.

[11] S. Lombardo, F. Crupi, and J. H. Stathis, Proc. Int. Relab. Phys. Symp. , 2001, p. 163.

[12] B. P. Linder, J. H. Stathis, R. A. Wachnik, E. Wu, S. A. Cohen, A. Ray, and A. Vayshenker, Symp. VLSI Tech. (2000).

[13] M. A. Alam, R. K. Smith, B. E. Weir, and P. J. Silverman, Tech. Dig. - Int. Electron Devices Meet. **2002**, 151.

[14] Tahui Wang *et al.*, Proc. Int. Reliab. Phys. Symp. , 2003, p. 437.

[15] T. Ouisse, G. Ghibaudo, J. Brini, S. Cristoloveanu, and G. Borel, J. Appl. Phys. **70**, 3912 (1991).

[16] J. Pretet, N. Subba, D. Ioannou, S. Cristoloveanu, W. Maszara, and C. Raynaud, IEEE Electron Device Lett. **23**, 300 (2002).

[17] T. Poiroux, O. Faynot, C. Tabone, H. Tigelaar, H. Mogul, N. Bresson, and S. Cristoloveanu, IEEE International SOI Conference (2002).

[18] M. C. Chen *et al.*, Proc. Int. Reliab. Phys. Symp. , 2002, p. 404.

[19] J. S. Suehle, IEEE Trans. Electron Devices **49**, 958 (2002).

[20] J. H. Stathis, J. Appl. Phys. **86**, 5757 (1999).

[21] E. Miranda and J. Sune, Appl. Phys. Lett. **78**, 225 (2001).

[22] R. Degraeve, G. Groeseneken, R. Bellens, J. L. Ogier, M. Depas, P. J. Roussel, and H. E. Maes, IEEE Trans. Electron Devices **45**, 904 (1998).

[23] M. Rasras, I. De Wolf, G. Groeseneken, R. Degraeve, and H. E. Maes, Tech. Dig. - Int. Electron Devices Meet. **2000**, 537.

[24] S. Lombardo, A. La Magna, C. Spinella, C. Gerardi, and F. Crupi, J. Appl. Phys. **86**, 6382 (1999).

[25] R. Tsu and L. Esaki, Appl. Phys. Lett. **22**, 562 (1973).