Separation of Channel Backscattering Coefficients in Nanoscale MOSFETs

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***Abstract*—Channel backscattering coefficients in the k_BT layer (near the source) of 1.65-nm-thick gate oxide, 68-nm gate length bulk n-channel MOSFETs are systematically separated into two distinct components: the quasithermal-equilibrium mean-free-path for backscattering and the width of the k_BT layer. Evidence to confirm the validity of the separation procedure is further produced: 1) the near-source channel conduction-band profile; 2) the existing value of k_BT layer width from the sophisticated device simulation; and 3) an analytic temperature-dependent drain current model for the channel backscattering coefficients. The findings are also consistent with each other and therefore corroborate channel backscattering as the origin of the coefficients. Other interpretations and clarifications are determined with respect to the very recently released Monte Carlo particle simulation. Consequently, it can be reasonably claimed that the separated components, as well as their dependencies on temperature and bias, are adequate while being used to describe the operation of the devices undertaken within the framework of the channel backscattering theory.**

***Index Terms*—MOSFETs, nanoscale, scattering.**

I. INTRODUCTION

CHANNEL backscattering theory has recently been introduced to provide the mesoscopic aspects of carrier transport in nanoscale MOSFETs [1]–[6]. In the schematic illustration of the theory for the saturation case shown in Fig. 1, a k_BT layer, where k_B ($= 8.614 \times 10^{-5}$ eV/°K) is Boltzmann's constant and T is the temperature, exists in a small fraction ($0 \leq x \leq l$) of the channel [2]–[6]. This specific zone located near the source critically determines the current drive at the drain

$$I_D = Q_{\mathrm{inv}} v_{\mathrm{inj}} \frac{(1 - r_C)}{(1 + r_C)} \tag{1}$$

where Q_{inv} is the inversion-layer charge density per unit area at the top of the source-channel junction barrier, v_{inj} is the thermal injection velocity at the top of the source-channel junction barrier, and r_C is the channel backscattering coefficient through the k_BT layer. The theory also argues that the backscattering coefficient r_C is functionally linked to both the quasithermal-equilibrium mean-free-path λ for backscattering and the width l of the k_BT layer: $r_C = l/(l + \lambda)$.

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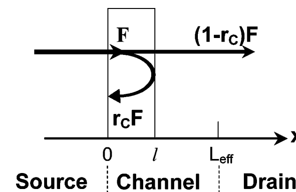

Fig. 1. Schematic diagram of channel backscattering theory. F is the incident flux from the source, l is the critical length over which a k_BT/q drop is developed, and r_C is the channel backscattering coefficient. The channel length L_{eff} is the physical gate length minus the source/drain extensions.

Experimentally, r_C can be assessed by current–voltage (*I–V*) fitting [3], [7], [8] or a temperature dependent technique [9]. To describe the operation of the device within the framework of the channel backscattering theory, λ and l must be further decoupled from the experimental r_C; however, little work was done in this direction.

On the other hand, very recently released Monte Carlo particle simulation [10] for the first time exhibited a relevant mechanism in a 10-nm gate length double-gate MOSFET case: the backscattering by the drain. The simulation [10] further revealed two other novel behaviors: (1) the reflection velocity distribution relative to the injection velocity distribution and (2) the non-Ohmic region in the drain. In a sense, these new mesoscopic properties must be taken into account when practically applying the currently recognized theory of channel backscattering to a certain device.

In this paper, assessment of r_C and its decoupling into λ and l both are systematically demonstrated in 68-nm gate length bulk MOSFETs. Evidence to confirm the validity of the separation procedure subsequently follows, which also consistently corroborates channel backscattering as the origin of the underlying r_C. Other interpretations and clarifications are determined relative to the above mentioned Monte Carlo simulation results. Eventually, the separated components, as well as their dependencies on temperature and bias, are used to describe the operation of the devices within the framework of the channel backscattering theory.

II. DEVICES UNDER STUDY

Halo-implanted bulk n-channel MOSFETs were formed using a state-of-the-art process. Fitting of a C-V (capacitance versus voltage) curve led to the following process parameters: the physical gate oxide thickness $t_{\mathrm{OX}} = 1.65$ nm, the n^+ polysilicon doping concentration $N_{\mathrm{POLY}} = 9 \times 10^{19}$ cm^{-3},

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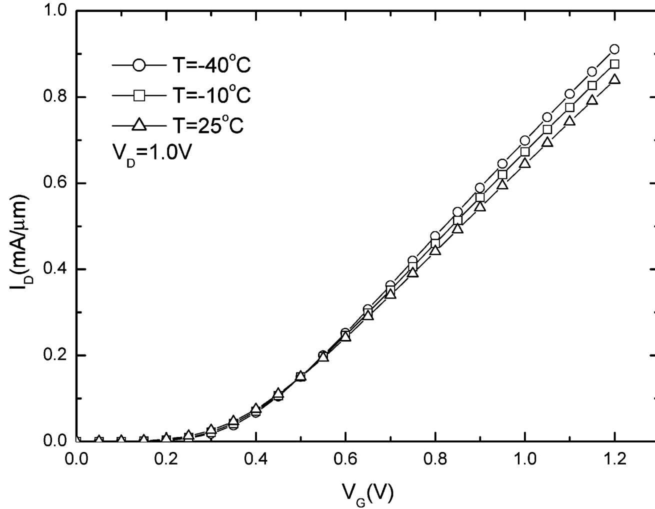

Fig. 2. Measured drain current versus gate voltage at $V_D = 1$ V for three temperatures.

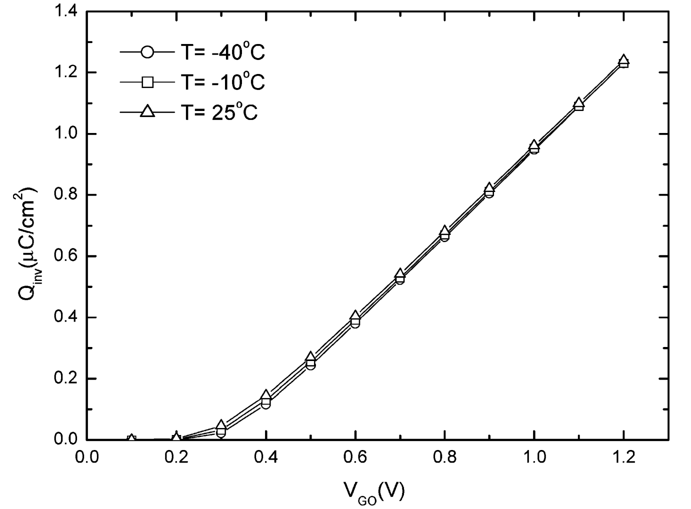

Fig. 3. Calculated inversion-layer charge density versus intrinsic gate voltage for three temperatures.

and the channel doping concentration $\mathrm{N_A} = 8 \times 10^{17}\ \mathrm{cm}^{-3}$. The physical gate length and width of the devices under study were 68 nm and 10 μm, respectively. Fig. 2 depicts measured drain current versus gate voltage characteristics at a drain voltage $V_D = 1$ V for three temperatures, $-40\,°$C, $-10\,°$C, and $25\,°$C. The near-thermal-equilibrium threshold voltage V_{tho} was 0.36, 0.34, and 0.33 V for temperatures of $-40\,°$C, $-10\,°$C, and $25\,°$C, respectively, which were obtained using the peak transconductance extrapolation method at $V_D = 25$ mV. The temperature coefficient of V_{tho} was -0.49 mV/°K. The drain-induced-barrier-lowering (DIBL), defined under constant subthreshold conduction as the magnitude of the gate voltage shift divided by a change in drain voltage (from 25 mV to 1 V), was about 110 mV/V.

III. Assessment of r_C

To account for the source series resistance R_S, drain series resistance R_D, and DIBL, (1) is augmented into

$$I_D = C_{\mathrm{eff}} \times [(V_G - I_D R_S) - (V_{\mathrm{tho}} - DIBL \times (V_D - I_D R_S - I_D R_D))] \times \upsilon_{\mathrm{inj}} \times \frac{1 - r_C}{1 + r_C}. \quad (2)$$

Here, the terms $V_G - I_D R_S$ and $V_D - I_D R_S - I_D R_D$ represent the intrinsic gate voltage and intrinsic drain voltage, respectively; and the term $V_{\mathrm{tho}} - DIBL \times (V_D - I_D R_S - I_D R_D)$ indicates the threshold voltage later designated as V_{th}. The effective gate capacitance C_{eff}, the near-thermal-equilibrium threshold voltage V_{tho} and the thermal injection velocity υ_{inj} were all calculated in advance using a one-dimensional quantum mechanical numerical program [11] dedicated to an n^+ polysilicon/gate oxide/p-type substrate MOS system. This program employed the same algorithm on the basis of the triangular potential well approximation as in [12]. With known process parameters (i.e., $\mathrm{t_{ox}}$, $\mathrm{N_{POLY}}$, and $\mathrm{N_A}$) as input, the simulator quantified the subband energy levels and Fermi level, which in turn yielded electron population in the underlying two-dimensional electron gas (2DEG) inversion layer. The resulting inversion-layer charge density $Q_{\mathrm{inv(eq)}}$ under equilibrium conditions versus intrinsic gate voltage V_{GO} is shown in Fig. 3, with temperature used as the parameter. Fitting to the one-dimensional MOS electrostatics formula $Q_{\mathrm{inv(eq)}} = C_{\mathrm{eff}}(V_{GO} - V_{\mathrm{tho}})$ yielded $C_{\mathrm{eff}} = 1.38\ \mu\mathrm{F/cm^2}$ and the $V_{\mathrm{tho}} = 0.32$ V, 0.31 V, and 0.30 V for temperatures of -40 °C, -10 °C, and 25 °C, respectively. The corresponding threshold quantities, as well as temperature coefficient (-0.33 mV/°K), are all comparable with those measured under quasithermal-equilibrium conditions (i.e., $V_D = 25$ mV, as mentioned above).

Again with the same subband levels and Fermi level as input, the effective thermal injection velocity at the top of the source-channel junction barrier can be readily calculated [4] as

$$\upsilon_{\mathrm{inj}} = \frac{\sum n_s^i \upsilon_{\mathrm{inj}}^i}{\sum n_s^i} \quad (3)$$

where n_s^i is the charge density associated with subband i in a certain direction (for example, a stream with a positive wavevector) and $\upsilon_{\mathrm{inj}}^i$ is the corresponding thermal injection velocity [4], [13]

$$n_s^i = \gamma \frac{m_{di}}{\pi \hbar^2} \frac{k_B T}{2} \ell n \left[1 + \exp\left(\frac{E_f - E_i}{k_B T}\right)\right] \quad (4)$$

$$\upsilon_{\mathrm{inj}}^i = \sqrt{\frac{2 k_B T m_{ci}}{\pi m_{di}^2}} \frac{\Im_{1/2}\left(\frac{E_f - E_i}{k_B T}\right)}{\ell n \left[1 + \exp\left(\frac{E_f - E_i}{k_B T}\right)\right]}. \quad (5)$$

Here, γ is the valley degeneracy, m_{ci} is the conductivity effective mass for subband i, m_{di} is the density-of-states effective mass for subband i, E_i is the energy level of subband i, E_f is the Fermi level, and $\Im_{1/2}$ is the Fermi–Dirac integral of order one-half. For twofold valleys, $m_{ci} = m_t$ and $m_{di} = m_t$, and for fourfold valleys, $m_{ci} = 2m_l m_t/(m_l + m_t)$, and $m_{di} = (m_l m_t)^{1/2}$, where the longitudinal mass $m_l = 0.916 m_o$ and the transverse mass $m_t = 0.19 m_o$. The results are displayed in Fig. 4 against intrinsic gate voltage with temperature used as the parameter. From these results, some important properties can be drawn. First, at low gate voltages, or at the nondegenerate limit, the thermal injection velocity considerably increases with temperature, regardless of gate voltage, as expected. Second, at

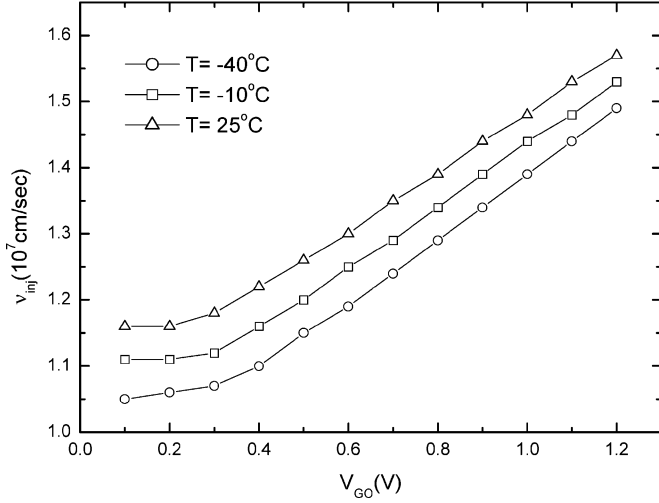

Fig. 4. Calculated thermal injection velocity versus intrinsic gate voltage for three temperatures.

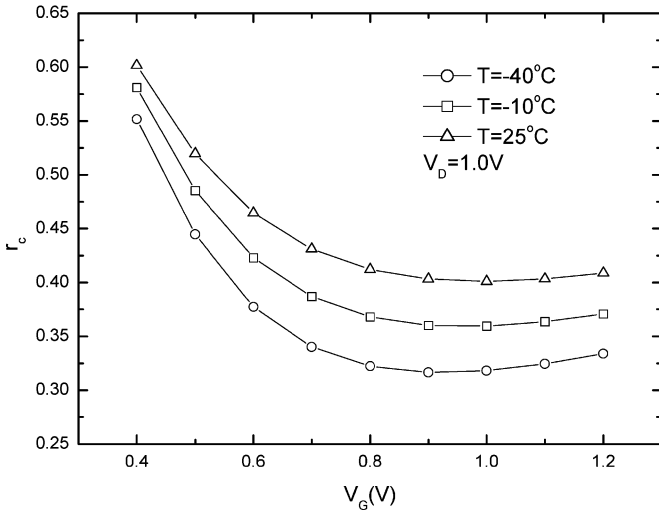

Fig. 5. Extracted backscattering coefficients corresponding to Fig. 2.

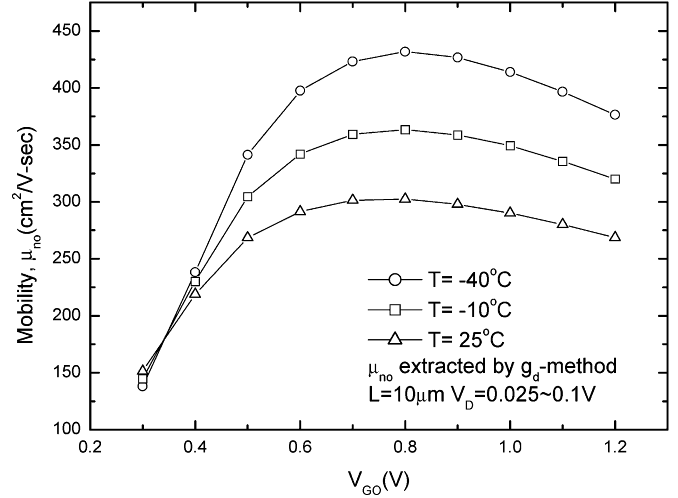

Fig. 6. Measured mobility versus intrinsic gate voltage for three temperatures.

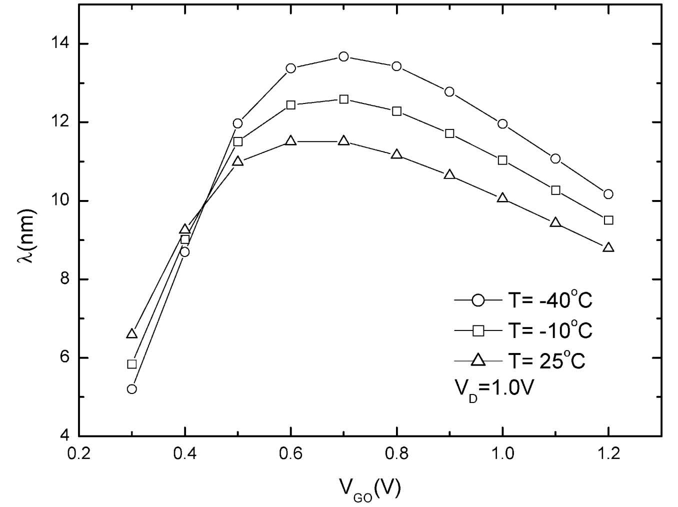

Fig. 7. Extracted mean-free path versus intrinsic gate voltage for three temperatures.

high gate voltages, or near the degenerate limit, the thermal injection velocity increases with gate voltage whereas the rate of increase declines with increasing temperature. The same dependencies are mentioned elsewhere [4].

The source series resistance R_S was about 75 Ω-μm, which was determined using the ratio-and-shift method on long-channel devices (up to 10 μm) from the same manufacturing process. As usually adopted, the drain series resistance R_D was assumed to be equal to R_S. Now all the parameters in (2) are known, except r_C. At this time, r_C can be assessed by fitting (2) to I_D versus V_G in Fig. 2. The results are given in Fig. 5 against gate voltage with temperature used as the parameter. It can be seen that: 1) r_C decreases with increasing gate voltage and then, critically, tends to saturate and 2) r_C decreases with decreasing temperature, in agreement with [9]. On the other hand, the Monte Carlo simulation [10] revealed a non-Ohmic property in the drain of the ultra short channel devices. This specific case of $R_D = 0$ was also included in the calculation and the corresponding change in r_C was found to be very small. The reasons are that R_D of 75 Ω-μm multiplied by the drain current (0.64 $\mathrm{mA}/\mu\mathrm{m}$ in Fig. 2, for example) is negligible relative to $V_D = 1$ V.

IV. Separated Components

Long-channel devices from the same process were also employed to characterize near-thermal-equilibrium mobility $\mu_{\rm no}$. Fig. 6 displays measured mobility versus intrinsic gate voltage with temperature used as the parameter, which was obtained using a drain conductance method [14]. It can be seen that the mobility versus gate voltage curve can be separated into three well-known distinct components [14]: Coulombic scattering, phonon scattering, and surface roughness scattering. Further observation points out that different temperature dependencies exist between different components, as expected.

The mean-free-path λ in the k_BT layer is functionally linked to $\mu_{\rm no}$ and $v_{\rm inj}$ through $\lambda = 2\mu_{\rm no}(k_BT/q)/v_{\rm inj}$ [1]–[6]. Substituting the measured $\mu_{\rm no}$ and calculated $v_{\rm inj}$ into the formula, λ was quantified as plotted in Fig. 7 against intrinsic gate voltage with temperature used as the parameter. It can be seen that a critical gate voltage of 0.45 V exists, above which the mean-free-path decreases with increasing temperature, and below which

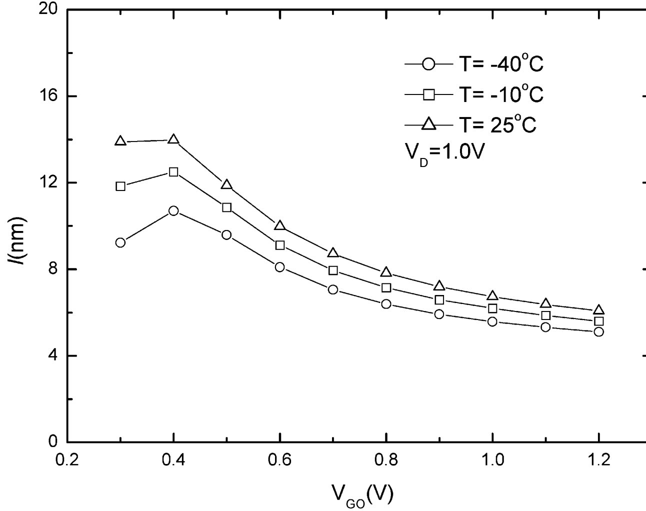

Fig. 8. Extracted k_BT layer width corresponding to Fig. 2.

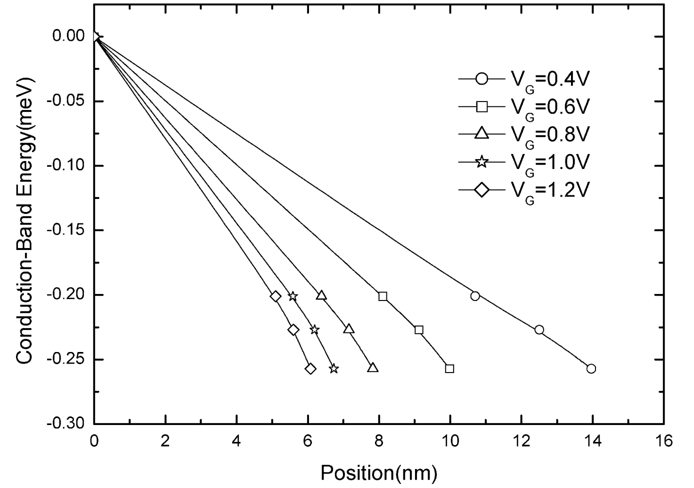

Fig. 9. Near-source channel conduction-band profile transformed from Fig. 8.

an increase in temperature produces an increase in the mean-free-path. The former dependence can be attributed to the surface roughness scattering dominating while the thermal injection prevails in the latter. Since the magnitude of the mean-free-path has been known, the corresponding k_BT-layer width can readily be obtained from Fig. 5. The results are shown in Fig. 8 versus gate voltage for three temperatures. It can be seen that the k_BT layer narrows with increasing gate voltage and decreasing temperature. A change in temperature produces a broad spread in k_BT-layer widths, especially at low gate voltages.

V. Evidence

Evidence to confirm the validity of the above separation procedure is produced: 1) the near-source channel conduction-band profile; 2) the k_BT layer width in the literature involving sophisticated device simulation; and 3) an analytic temperature-dependent drain current model for the channel backscattering coefficients. The findings are also consistent with each other and therefore corroborate channel backscattering as the origin of the r_C in underlying devices.

A. Near-Source Channel Conduction-Band Profile

Within the framework of the channel backscattering theory, the channel conduction band is bent downward by a thermal energy k_BT while traversing from the injection point (i.e., the top of the source-channel junction barrier) to the end of the k_BT layer. According to this definition, the temperature dependent k_BT-layer widths in Fig. 8 were transformed into the near-source channel conduction-band profile as plotted in Fig. 9. Strikingly, it can be seen that the potential gradient increases in magnitude with increasing distance from the source. Indeed, sophisticated device simulations on bulk devices [8], [15] exhibited the same trend. Thus, the conduction-band profile in Fig. 9 can serve as strong evidence for the work.

B. Existing Value of l

Hydrodynamic device simulation [15] on a 2.5-nm-thick physical gate oxide, 50-nm channel length bulk MOSFET yielded an l value of around 9.5 nm at $V_G = V_D = 1$ V. Our extracted value at the same applied biases is 6.7 nm (see Fig. 8) for a 1.65-nm-thick physical gate oxide, 68-nm gate length bulk MOSFET. We found that the difference between the two l values can almost be eliminated if the two factors are offset in advance. The first factor is the different potential drop across the source: the study in [15] conducted by Choi used 0.25 V, whereas we used 0.05 V. Therefore a downward shift of 0.2 V in gate voltage from 1 to 0.8 V is required for fair comparison, giving a corresponding l of 7.8 nm. The second factor is due to the different gate oxide thickness. A first-order approximation (0.2-V threshold voltage was assumed; the equivalent electrical gate oxide thickness in inversion was about 3.35 nm in [15] and 2.5 nm in our work) was performed to retain the same inversion-layer charge density, leading to an updated gate voltage of around 0.65 V. At this point the k_BT layer width becomes 9.3 nm, quite close to the 9.5-nm result exhibited in [15].

C. Temperature-Dependent Drain Current Model for λ/l

An analytical temperature dependent drain current model in [9] is extended in general form as follows:

$$\frac{dI_D}{dT}\times\frac{1}{I_D}=\frac{-\eta}{(\mathrm{V}_G-\mathrm{V}_{th})}+\frac{a}{T}+\frac{2}{T}(b+1-a-c)\frac{1}{2+\frac{\lambda}{l}}. \quad (6)$$

Here, η stands for the temperature coefficient of near-thermal-equilibrium threshold voltage. The other constants appear in the following power law relationship: the injection thermal velocity $v_{\mathrm{inj}} \propto T^{\mathrm{a}}$; the low lateral-field mobility $\mu_{\mathrm{no}} \propto T^b$; and the width of the k_BT layer $l \propto T^{\mathrm{c}}$. The numerical constants a, b, and c can be determined from the temperature dependencies of the calculated v_{inj} in Fig. 4, the measured μ_{no} in Fig. 6, and the extracted l in Fig. 8, respectively. The resulting power exponents are plotted in Fig. 10 against gate voltage. Then by substituting these constants and experimental drain currents into (6), we obtained the channel backscattering coefficients at 25 °C, as shown in Fig. 11. Again, a good agreement was achieved.

VI. Further Discussion

Further interpretations and clarifications can be determined relative to the backscattering by the drain in the ultra short channel (10-nm channel length) double-gate MOSFET at

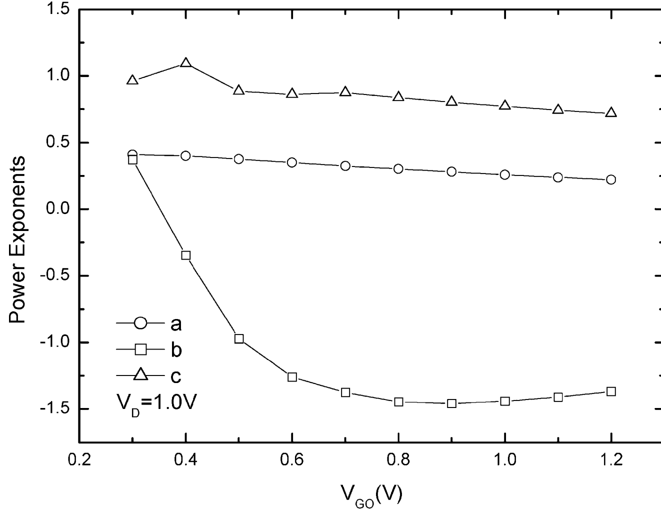

Fig. 10. Fitted power exponents versus gate voltage.

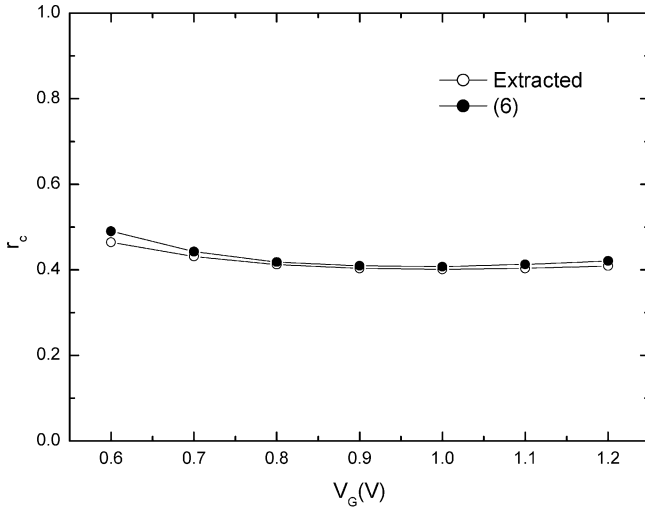

Fig. 11. Comparison of extracted r_C at 25 °C with that from (6).

$V_D = 0.2$ V [10]. First, quasiballistic electrons moving out of the k_BT layer and entering into the remainder of the channel experience a process of energy loss via phonon emission. This loss in energy increases with increasing channel length, as in our device, which effectively prohibits backscattering from the drain reaching the beginning point of the channel. Second, the large drain voltage of 1 V applied in our work causes a large barrier height to be encountered near the drain, which significantly increases the difficulties the backscattered electrons from the drain have been overcoming the barrier height. Finally, in a bulk device operated in saturation as in our work, the distributions of the electric field and the current flow lines near the drain are essentially two dimensional, which effectively enlarges the path of the drain backscattering to the source.

The simulation work [10] further pointed out the possible difference between the distribution shape of the injection velocity and that of the reflection velocity. On the other hand, under the quasiballistic conditions (i.e., the energy loss in a backscattering event can be ignored on average), the events of multiple backscatterings through the k_BT layer can lead to a relationship of $r_C = l/(l+\lambda)$ (see [1, Chapter 2] for details). In other words, a simple form of $r_C = l/(l+\lambda)$ can apply equally to the forward and backward flux streams. Therefore, according to the work of [10], if a single r_C is used, then the average reflection velocity at the top of the source-channel barrier should be expressed as the injection velocity υ_{inj} multiplied by a certain factor θ (≥ 1). Here, θ is introduced to reflect the contribution of the fast carriers [10]: $\theta = 1$ means that the distribution of the reflection velocity at the top of the source-channel barrier can be approximated by a hemi-Maxwellian distribution as that of the injection velocity; and θ increases with the increasing importance of the fast carriers through an extended tail of the distribution profile. In a similar way leading to (1), the drain current in the presence of factor θ can be derived as follows:

$$I_D = Q_{inv}\upsilon_{\text{inj}}\frac{(1-\theta r_C)}{(1+r_C)}. \tag{7}$$

As described in detail above, a single υ_{inj} as a first-order approximation appears to work well, suggesting $\theta \approx 1$ in our work.

Therefore, we can now reasonably claim that the separated components, as well as their dependencies on temperature and bias, can be adequately used to describe the operation of the device within the framework of the channel backscattering theory. For example, at operating conditions of 25 °C and $V_G = V_D = 1$ V the conduction band from the injection point of the channel is bent down by a thermal energy of 25.7 meV to a distance of $l = 6.7$ nm (see Fig. 8). Then a bending of approximately 1 eV is subsequently developed across the remainder of the channel. The mean-free-path λ is 10.1 nm (also see Fig. 7) for backscattering in 6.7-nm-wide k_BT layer, effectively producing a backscattering coefficient r_C of 0.4. The mean-free-path is larger than the width of the layer, confirming the quasiballistic transport. The injected charge density from the source is 0.72 $\mu\text{C/cm}^2$ with the injection velocity of 1.48×10^7 cm/sec. The incident flux stream multiplied by the transmission probability ($= 1 - r_C$) constitutes the drain current of 0.64 mA/μm. A similar argument can apply to other biases and temperatures.

VII. Conclusion

Separation of channel backscattering coefficients in 68-nm gate length bulk n-channel MOSFETs has been systematically performed. Consistent evidence has confirmed the validity of the separation procedure and has corroborated channel backscattering as the origin of the assessed coefficients. Other interpretations and clarifications have been determined with respect to the backscattering by the drain, the injection and reflection velocity distributions, and the non-Ohmic property in the drain. The separated components have eventually been used to describe the operation of the underlying device within the framework of the channel backscattering theory.

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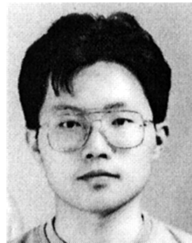

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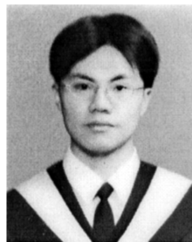
His research interests are focused on device physics and modeling of silicon nano CMOS.



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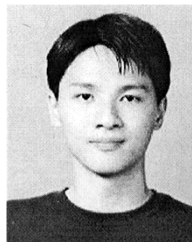

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Dr. Diaz served in the International Conference on Simulation of Semiconductor Processes and Devices, the IEEE International Reliability Physics Symposium, and the EOS/ESD Symposium program committees. Currently, he is a member of the VLSI Technology Symposium, and a member of the technical program committees for Solid State Devices and Materials and the International Electron Devices Meeting. He was the recipient of two Semiconductor Research Corporation (SRC) inventor awards.