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A new small-signal MOSFET model and parameter extraction method for RF IC's application

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Abstract

In this paper, an accurate and simple small signal model of RF MOSFETs accounting for the distributed gate effect, the substrate parasitics and charge conservation is proposed. Meanwhile, a direct and accurate extraction method using linear regression approach for the components of the equivalent circuit of the MOSFET with *S*-parameters analysis is also proposed. The proposed model and extraction method are verified with the experimental data and an excellent agreement is obtained up to 10 GHz. The extraction results from the measured data for various bias conditions are presented. Also, the extracted parameters, such as transconductance g_m, match well with those obtained from DC measurements. Besides, it is shown that a significant error in circuit performances would be found if the charge conservation is not properly considered.

Keywords: Gate resistance; RF MOSFET modeling; Substrate resistance; Nonreciprocal capacitance

1. Introduction

The majority of the radio-frequency integrated circuits (RFICs) are typically implemented by GaAs or silicon bipolar technologies [1,2]. Due to their high unity-gain cutoff frequency (f_t), GaAs devices and BJTs have been generally used in high frequency applications. However, continuously scaling down of the minimum channel length and the consequent increase of f_t have made CMOS technology become an attractive one in applications for analog and RFICs [3]. With another advantage (i.e. high integration level and low cost budget, etc.) over GaAs and silicon bipolar technologies, CMOS technology is a good candidate to meet the demand of wireless telecommunication system in the future.

As circuitry operates at higher frequency (GHz frequency range) and lower voltages, a major requirement for RF circuit design is the availability of RF MOS transistor model to describe the circuit behavior accurately. Besides, the establishment of an accurate parameters extraction method relevant to the RF model is essential.

In order to meet the requirement for an accurate RF model, several fundamental analyses on MOSFETs high frequency characteristics have been developed, as described in Refs. [4–6]. As MOSFETs operation frequency approaches VHF and beyond, the parasitic components geometry-related (e.g. inductance, capacitance and resistance) play important roles in their high frequency performance. Therefore, the nature of gate region—RLC distributed network and substrate parasitics should be considered in the development of RF MOS model. Some conventional models [7–9] replaced the gate region with a single resistance, and this would cause inaccuracy in predicting the gate related noise at high frequency [10]. Besides, in several models [10–12], the substrate parasitics were not taken into account, and this would hurt their accuracy in the prediction of output characteristics (i.e. output impedance [13]). In addition, several conventional models [13–15] excluded the nonreciprocal capacitance considering the charge conservation [16], and this would result in a significant error in predicting the imaginary parts of Y_{12} and Y_{21}.

Except for the development of an accurate RF model, a related parameters extraction methodology is indispensable. Several methods of extracting small-signal equivalent

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circuit parameters from the *S*-parameter measurement data have been reported [14,17,18]. However, most of them require complex curve fitting and optimization steps.

In this paper, we propose a high frequency analytical MOSFETs model well describing the distributed effects of the gate region and including substrate parasitics and nonreciprocal capacitance. Besides, a direct and accurate parameter extraction method for the proposed model including gate-related parameters, substrate-related parameters and nonreciprocal capacitor is also proposed. This study focuses on the development of a physics-based small signal MOSFETs model and an accurate parameter extraction approach by *Y*-parameter analysis from measured *S*-parameters.

This paper is organized in the following manners. In Section 2, a new and accurate high frequency MOS transistor model is briefly described. This section begins with the assumptions and definitions, which are useful for the model development, and follows by describing the closed-form modeling equations. In Section 3, an accurate and direct method for the extractions of the parameters of small signal equivalent circuit is presented and explained in detail. In Section 4, the proposed model and related extraction method are verified by the experimental data. Finally, the conclusions are summarized in Section 5.

2. Small signal RF MOSFET model

In this section, a new and analytical small signal RF MOSFET model including distributed gate network, substrate parasitics and nonreciprocal capacitance is proposed. At first, the relative approaches and assumptions are briefly described and defined, respectively. Then, the derivation details of model equations will be described.

2.1. Approaches and assumptions

To accurately describe the fact that the signal travels across the gate in the form of incident and reflected EM waves [10], we use the concept of transmission line theorem to model the distributed nature of the gate region and the delay it causes in charging the gate capacitance. In addition, for the sake of simplicity and calculation efficiency, we add a lumped resistance to the bulk terminal to account for the substrate coupling effect. We also use the nonreciprocal capacitance to take into account the different effects of the gate and drain on each other in terms of charging currents [16]. In order to describe the distributed nature of the gate region, a MOS transistor is viewed as an array of discrete transistors connected in parallel via gate resistances along the gate region, as illustrated in Fig. 1. The related small signal equivalent circuit is shown in Fig. 2 which is based on the three-terminal configuration. In a three-terminal

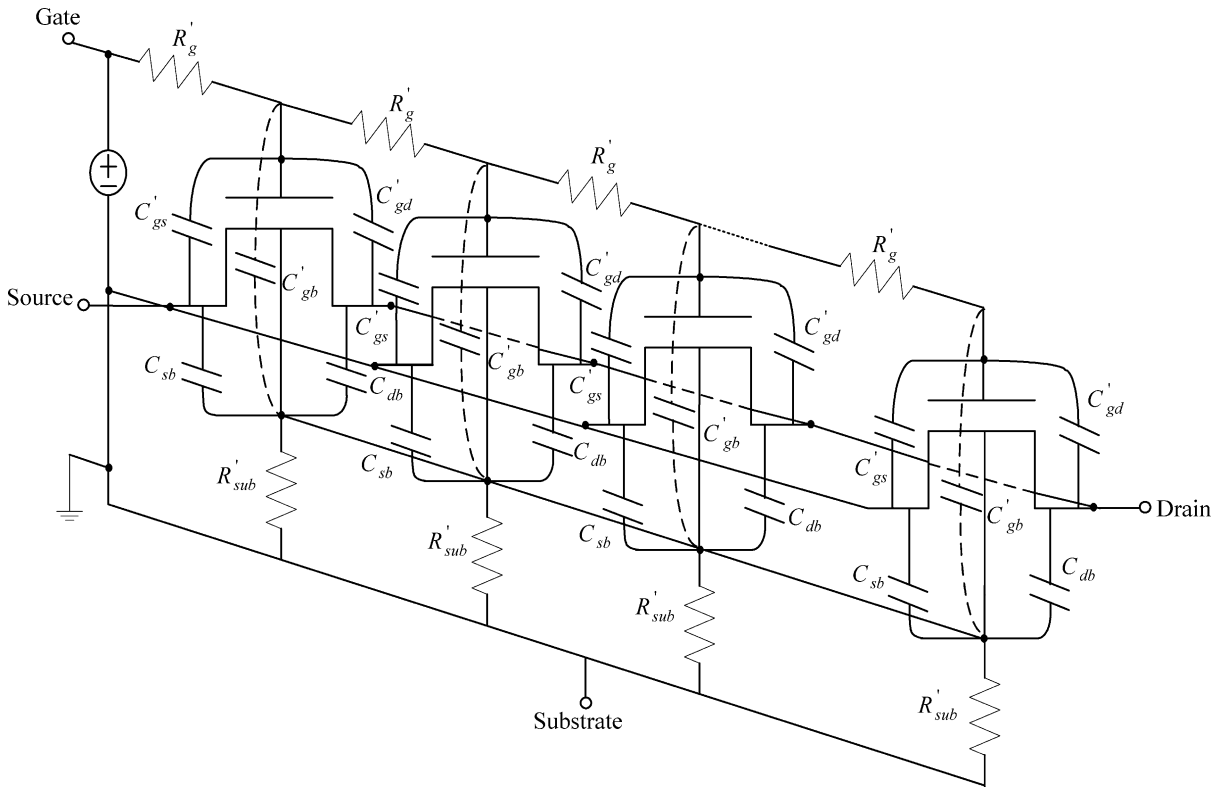

Fig. 1. Pictorial view of the distributed elements within a MOS transistor along the gate width.

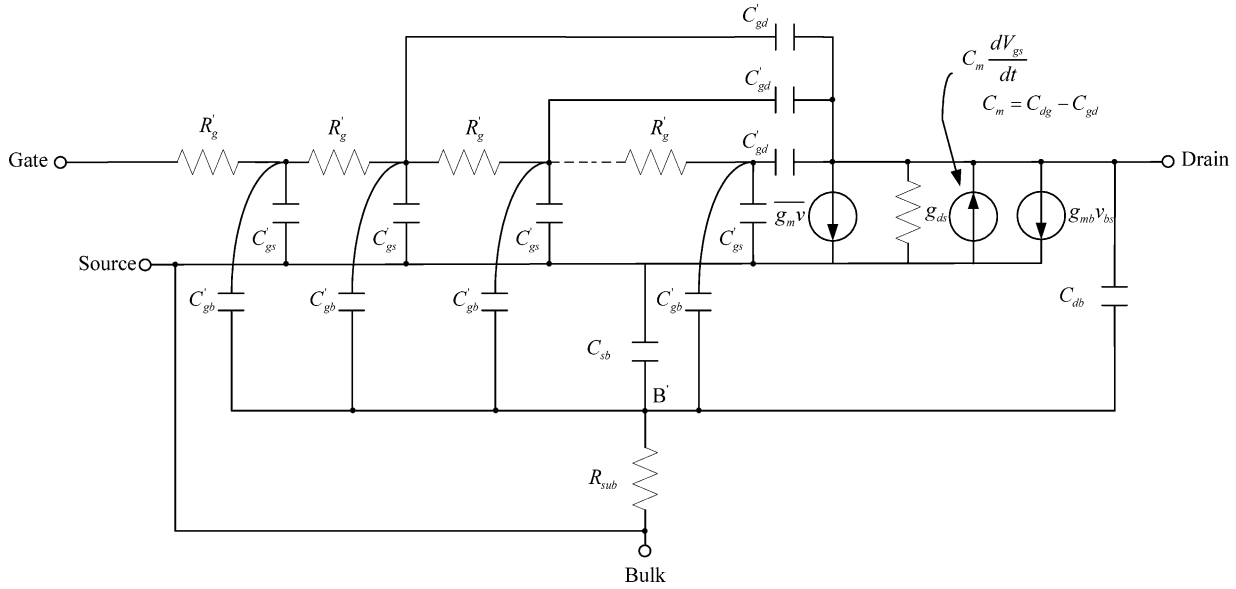

Fig. 2. Small signal equivalent circuit of an MOSFET for RF modeling.

configuration, the substrate is tied to the source, as in most high frequency applications [9,19]. This model is suitable for the case of zero source–substrate bias in circuit. Before developing expressions for the *Y*-parameters of the MOS transistors, the following assumptions have to be made:

Assumption 1. It is assumed that the DC bias condition remains the same along the gate width. This means that only AC small signals applied at the gate region needed to be considered. With this assumption, the discrete MOS transistors illustrated in Fig. 1 have the same small signal parameters (e.g. transconductance g_m; drain-bulk transconductance g_{mb}, etc.). To make the model equations clearly, we use the prime-notation to stand for the parameters per width (i.e. X' is used to represent the variable X per unit width)

$$R'_g = \frac{R_g}{W} \tag{1}$$

$$C'_{gd} = \frac{C_{gd}}{W} \tag{2}$$

$$C'_{gs} = \frac{C_{gs}}{W} \tag{3}$$

$$g'_m = \frac{g_m}{W} \tag{4}$$

where W is the channel width, R_g is the gate resistance, C_{gd} and C_{gs} are the gate-to-drain capacitance and gate-to-source capacitance, respectively, and g_{mb} is the transconductance of substrate.

Assumption 2. This assumption states that the electric field along the width of the device is significantly less than the fields existing along the channel length. Note that this condition is valid in most devices used for RF applications where the gate width W is normally larger with respect to the gate length L.

Assumption 3. In order to develop an analytical model easily, the average voltage at the gate region is expressed as

$$\bar{v} = \frac{1}{W}\int_0^W v(x)\mathrm{d}x \tag{5}$$

where $\bar{v}$ is the average voltage at the gate region, and $v(x)$ is the voltage at the location x along the gate region. Thus, the total current flowing in the channel can be expressed as:

$$\overline{g_m v} = \int_0^W g'_m v(x)\mathrm{d}x \tag{6}$$

2.2. Analysis for new RF MOSFET model

In the primary step, we will decouple the feedback loops and find the loadings caused by the feedback networks at the input and output terminals. Then, the derivation of *Y*-parameters of MOSFETs will be expressed in the secondary step.

Step 1. The circuit configuration shown in Fig. 2 is too complicated to be analyzed directly. Nevertheless, if the circuit is viewed as a dual-feedback circuit in which ΔC_{gd} is the local shunt–shunt feedback element forms the first feedback loop (i.e. loop A), where $\Delta C_{gd} = C'_{gd}\Delta x$ represents the gate–drain capacitance of the section Δx at the gate region, and C_{db}, C_{sb}, R_{sub} and $C'_{gb}\Delta x$ are the local shunt–shunt feedback elements form the second feedback loop (i.e. loop B), where $\Delta C_{gb} = C'_{gb}\Delta x$ represents the gate–substrate capacitance of the section Δx at the gate region, then the circuit becomes much easier to solve. The feedback loops A and B are illustrated in Fig. 3, where V_1 and V_2 represent the output voltage relative to ground (e.g. V_{ds}) and the voltage

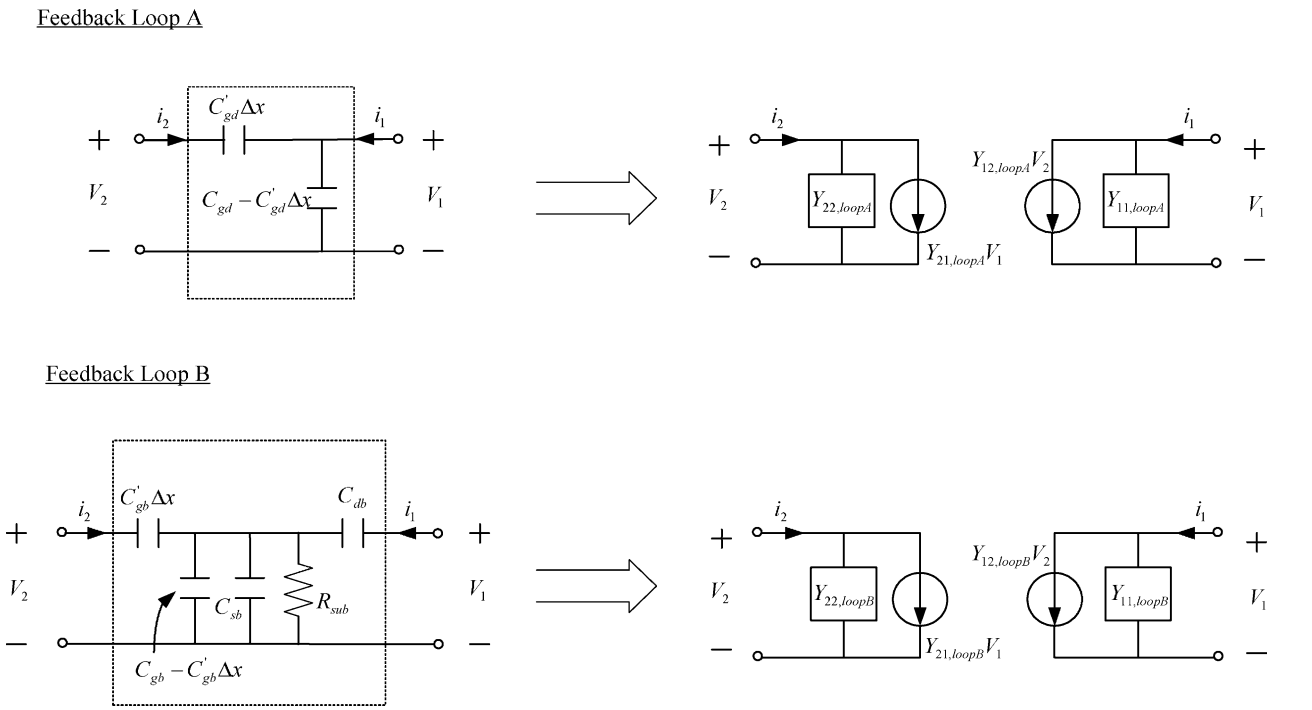

Fig. 3. Equivalent circuits of shunt–shunt feedback loops are presented. By feedback theorem [20], feedback loops A and B can be transformed into equivalent loadings on the input and output nodes.

along the gate width shown in Fig. 2, respectively. By local shunt–shunt feedback theory [20], the loading effects at the input and output terminals caused by the feedback networks shown in Fig. 3 can be expressed in the Y-parameter representation as follows

$$Y_{11,\mathrm{loopA}} = sC_{\mathrm{gd}} \tag{7}$$

$$Y_{12,\mathrm{loopA}} = Y_{21,\mathrm{loopA}} = -sC'_{\mathrm{gd}}\Delta x \tag{8}$$

$$Y_{22,\mathrm{loopA}} = sC'_{\mathrm{gd}}\Delta x \tag{9}$$

$$Y_{11,\mathrm{loopB}} = \frac{sC_{\mathrm{db}}(1+sR_{\mathrm{sub}}(C_{\mathrm{sb}}+C_{\mathrm{gb}}))}{1+sR_{\mathrm{sub}}C_{\mathrm{b}}} \tag{10}$$

$$Y_{12,\mathrm{loopB}} = Y_{21,\mathrm{loopB}} = -\frac{s^2R_{\mathrm{sub}}C_{\mathrm{db}}C'_{\mathrm{gb}}\Delta x}{1+sR_{\mathrm{sub}}C_{\mathrm{b}}} \tag{11}$$

$$Y_{22,\mathrm{loopB}} = \frac{sC'_{\mathrm{gb}}\Delta x(1+sR_{\mathrm{sub}}(C_{\mathrm{sb}}+C_{\mathrm{db}}+C_{\mathrm{gb}}-C'_{\mathrm{gb}}\Delta x))}{1+sR_{\mathrm{sub}}C_{\mathrm{b}}} \tag{12}$$

where C_{db}, C_{sb} and C_{gb} are the drain-to-substrate capacitance, source-to-substrate capacitance and gate-to-substrate capacitance, respectively, C'_{gd} and C'_{gb} are the gate-to-drain capacitance per unit width and gate-to-substrate capacitance per unit width, R_{sub} is the substrate resistance, and C_{b} is the sum of C_{gb}, C_{db} and C_{sb}.

Then, with the local shunt–shunt feedback theory mentioned above, the circuit in Fig. 2 can be transformed into the one in Fig. 4. In Fig. 4, some components (i.e. $Y'_{12,\mathrm{loopA}}$, $Y'_{21,\mathrm{loopA}}$, $Y'_{22,\mathrm{loopA}}$, $Y'_{12,\mathrm{loopB}}$, $Y'_{21,\mathrm{loopB}}$ and $Y'_{22,\mathrm{loopB}}$) in the Blocks A and B are referred to as the per-unit width components and expressed as

$$Y'_{12,\mathrm{loopA}} = Y'_{21,\mathrm{loopA}} = -sC'_{\mathrm{gd}} \tag{13}$$

$$Y'_{22,\mathrm{loopA}} = sC'_{\mathrm{gd}} \tag{14}$$

$$Y'_{12,\mathrm{loopB}} = Y'_{21,\mathrm{loopB}} = -\frac{s^2R_{\mathrm{sub}}C_{\mathrm{db}}C'_{\mathrm{gb}}}{1+sR_{\mathrm{sub}}C_{\mathrm{b}}} \tag{15}$$

$$Y'_{22,\mathrm{loopB}} = \frac{sC'_{\mathrm{gb}}(1+sR_{\mathrm{sub}}(C_{\mathrm{sb}}+C_{\mathrm{db}}+C_{\mathrm{gb}}-C'_{\mathrm{gb}}\Delta x))}{1+sR_{\mathrm{sub}}C_{\mathrm{b}}} \approx \frac{sC'_{\mathrm{gb}}(1+sR_{\mathrm{sub}}(C_{\mathrm{sb}}+C_{\mathrm{db}}+C_{\mathrm{gb}}))}{1+sR_{\mathrm{sub}}C_{\mathrm{b}}} = sC'_{\mathrm{gb}} \tag{16}$$

where Δx is an infinitesimal section of the gate width.

Step 2. In the derivation procedure of Y-parameters, the complete small-signal equivalent circuit of Fig. 4 is analyzed as a two-port circuit with input at the gate and output at the drain and both the source and substrate terminals are grounded. Then, due to the distributed RC network along the gate region, the equivalent circuit can be analyzed by transmission line theory. Along the gate width, we have the transmission line equations in frequency domain as follows

$$-\frac{\partial v(x)}{\partial x} = R'_g i(x) \tag{17}$$

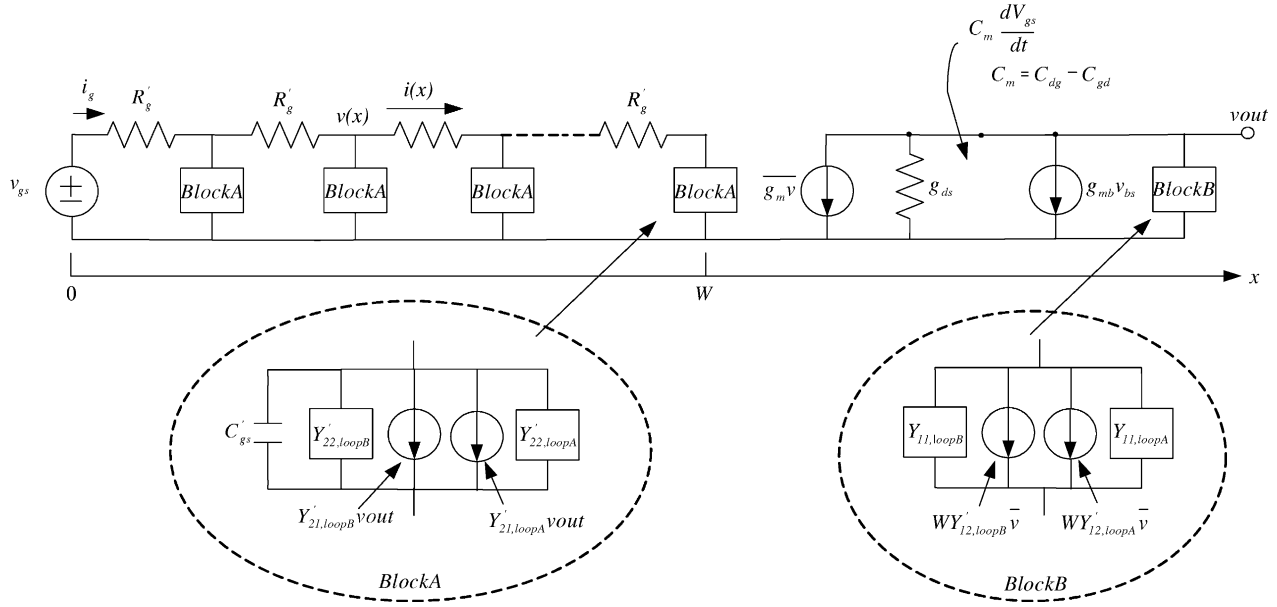

Fig. 4. Small signal equivalent circuit of an MOSFET after feedback loops transformation.

$$-\frac{\partial i(x)}{\partial x} = (sC'_{gs} + Y'_{22,loopA} + Y'_{22,loopB})v(x) + (Y'_{21,loopA} + Y'_{21,loopB})v_{out} = (sC'_{gs} + sC'_{gd} + sC'_{gb})v(x) + \left(-sC'_{gd} - \frac{s^2 R_{sub} C_{db} C'_{gb}}{1 + sR_{sub} C_b}\right)v_{out} \quad (18)$$

which are subject to the boundary conditions $i(W) = 0$ and $v(0) = v_{gs}$. Solving these equations for $v(x)$ and $i(x)$ yields

$$v(x) = \left(v_{gs} - \frac{B}{A}\right)\frac{\cosh(\sqrt{A}(W - x))}{\cosh(\sqrt{A}W)} + \frac{B}{A} \quad (19)$$

$$i(x) = \left(v_{gs} - \frac{B}{A}\right)\frac{\sqrt{A}}{R'_g}\frac{\sinh(\sqrt{A}(W - x))}{\cosh(\sqrt{A}W)} \quad (20)$$

where

$$A = R'_g(sC'_{gs} + Y'_{22,loopA} + Y'_{22,loopB}) = R'_g(sC'_{gs} + sC'_{gd} + sC'_{gb}) = sR'_g C'_g \quad (21)$$

$$B = -R'_g(Y'_{21,loopA} + Y'_{21,loopB})v_{out} = R'_g\left(sC'_{gd} + \frac{s^2 R_{sub} C_{db} C'_{gb}}{1 + sR_{sub} C_b}\right)v_{out} \quad (22)$$

where R'_g is the gate resistance per unit width and $C'_g = C'_{gs} + C'_{gd} + C'_{gb}$. With the assumption (3), the average voltage at the gate region and total current in the channel can be expressed as:

$$\bar{v} = \left(v_{gs} - \frac{B}{A}\right)\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} + \frac{B}{A} \quad (23)$$

$$\overline{g_m v} = g_m \bar{v} = g_m\left[\left(v_{gs} - \frac{B}{A}\right)\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} + \frac{B}{A}\right] \quad (24)$$

Then, according to the two-port circuit model, the Y-parameters of the equivalent small signal circuit can be solved as follows

$$Y_{11} = \left[\frac{i_g}{v_{gs}}\right]_{v_{out}=0} = W[sC'_{gs} + Y'_{22,loopA} + Y'_{22,loopB}]\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} = sC_g\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} \quad (25)$$

where i_g is expressed as the current at location $x = 0$ and C_g is the sum of C_{gb}, C_{gs} and C_{gd}. The above result clearly indicates that three coupling paths influence the input admittance Y_{11}. They are the ways from gate to source, gate to drain and gate to substrate through C_{gs}, C_{gd} and C_{gb}, respectively. Then, the parameter Y_{12} can be expressed as:

$$Y_{12} = \left[\frac{i_g}{v_{out}}\right]_{v_{gs}=0} = W\left(\underbrace{Y'_{21,loopA}}_{TermM} + \underbrace{Y'_{21,loopB}}_{TermN}\right)\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} = -\left(sC_{gd} + \frac{s^2 R_{sub} C_{db} C_{gb}}{1 + sR_{sub} C_b}\right)\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} \quad (26)$$

Eq. (26) provides useful insight on the coupling paths of drain voltage to gate current. Two terms (term M and term N) in Eq. (26) describe the paths. Term M: the voltage applied to the drain couples to the distributed gate region through C_{gd}. Term N: the drain voltage couples to the distributed substrate region and makes current flow through C_{gb} into gate region. In addition, the parameter Y_{21} can be expressed as

$$\begin{aligned} Y_{21} &= \left[\frac{i_d}{v_{gs}}\right]_{v_{out}=0} = \Bigg[\underbrace{(g_m + WY'_{12,loopA} - sC_m)}_{TermO} \\ &\quad + \underbrace{g_{mb}\frac{sR_{sub}C_{gb}}{1+sR_{sub}C_b}}_{TermP} + W\underbrace{Y'_{12,loopB}}_{TermQ}\Bigg]\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} \\ &= \left(g_m - sC_{dg} + \frac{sg_{mb}R_{sub}C_{gb} - s^2R_{sub}C_{db}C_{gb}}{1+sR_{sub}C_b}\right) \\ &\quad \times \frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} \end{aligned} \tag{27}$$

where C_m is the transcapacitance (i.e. $C_m = C_{dg} - C_{gd}$) and C_{dg} is the drain-to-gate capacitance. Similarly, the signal coupling paths are described by three terms expressed in Eq. (27). Term O: the voltage applied to the gate makes the current flowing in the channel, but due to the existence of C_{gd}, the current flowing from the drain end must subtract the current flowing through C_{gd} from gate region. Term P: the gate voltage makes current flow through C_{gb} and voltage drop across R_{sub}, v_{bs}, which is multiplied by g_{mb} to make current flowing into the channel. Term Q: the gate voltage makes the current flow through C_{gb} and voltage drop on R_{sub}, v_{bs}, which makes current flowing through C_{db} into the drain end in the opposite direction of i_d. Finally, the parameter Y_{22} can be expressed as

$$\begin{aligned} Y_{22} &= \left[\frac{i_d}{v_{out}}\right]_{v_{gs}=0} = \left(\underbrace{g_m + W(Y'_{12,loopA} + Y'_{12,loopB}) - sC_m}_{TermR}\right) \\ &\quad \times\left(1 - \frac{\tanh(\sqrt{A}W)}{\sqrt{A}W}\right)\frac{(-1)R'_g(Y'_{21,loopA} + Y'_{21,loopB})}{A} \\ &\quad + g_{ds} + \underbrace{Y_{11,loopA}}_{TermS} + \underbrace{Y_{11,loopB}}_{TermT} + \underbrace{g_{mb}\frac{sR_{sub}C_{db}}{1+sR_{sub}C_b}}_{TermU} \\ &= \left(g_m - sC_{dg} - \frac{s^2R_{sub}C_{db}C_{gb}}{1+sR_{sub}C_b}\right)\left(1 - \frac{\tanh(\sqrt{A}W)}{\sqrt{A}W}\right) \\ &\quad \times\left(\frac{sC'_{gd} + \dfrac{s^2R_{sub}C_{db}C'_{gb}}{1+sR_{sub}C_b}}{sC'_g}\right) + g_{ds} + sC_{gd} \\ &\quad + \frac{sC_{db}[1 + g_{mb}R_{sub} + sR_{sub}(C_{sb} + C_{gb})]}{1+sR_{sub}C_b} \end{aligned} \tag{28}$$

where g_{ds} is the conductance of drain-to-source. In Eq. (28), four terms describe the signal coupling paths. Term R: the voltage applied to the drain makes current flow into the distributed gate region through loops A and B, and voltage drop on the gate region, v_{gs}, which makes current flow out of the drain end through feedback loops A and B. Term S: the drain voltage makes current flow through loop A. Term T: the drain voltage makes current flow through C_{db} and voltage drop across R_{sub}, C_{sb} and C_{gb}, v_{bs}, which makes current flow out of the drain end. Term U: the voltage drop v_{bs} due to the coupling effect as described in Term T is multiplied by g_{mb} to make current flow into the channel. From the expressions of Y-parameters derived, how signal-coupling occurring through capacitive and resistive elements contained in Fig. 2 has been clearly explained.

3. Parameter-extraction method

In this section, a direct extraction method for RF equivalent circuit parameters of MOS transistors is presented. The method is based on the linear regression approach and the Y-parameters obtained from S-parameters analysis. All components in the equivalent circuit are extracted by the Y-parameters analysis and the relative analytical equations are derived from the real and imaginary parts of Y-parameter expressions mentioned in Section 2. The details of the equivalent circuit parameters extraction are described as follows.

Due to the fact that g_m and g_{ds} are DC parameters, they can be obtained from the y-intercept of $\mathrm{Re}[Y_{21}]$ versus w^2 and y-intercept of $\mathrm{Re}[Y_{22}]$ versus w^2 at low frequency, respectively, and shown as:

$$g_m = \mathrm{Re}[Y_{21}]_{w^2=0} \tag{29}$$

$$g_{ds} = \mathrm{Re}[Y_{22}]_{w^2=0} \tag{30}$$

Then, at low frequency, with the assumption that the first term in the parentheses of Eq. (26) dominates, Y_{12} can be approximated as follows:

$$\begin{aligned} Y_{12} &= -\left(sC_{gd} + \frac{s^2R_{sub}C_{db}C_{gb}}{1+sR_{sub}C_b}\right)\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} \\ &\approx -sC_{gd}\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} \end{aligned} \tag{31}$$

Similarly, with the assumption that the first two terms in the parentheses of Eq. (27) dominate, Y_{21} can be approximated as follows:

$$\begin{aligned} Y_{21} &= \left(g_m - sC_{dg} + \frac{sg_{mb}R_{sub}C_{gb} - s^2R_{sub}C_{db}C_{gb}}{1+sR_{sub}C_b}\right)\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} \\ &\approx (g_m - sC_{dg})\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W} \end{aligned} \tag{32}$$

Then, due to the fact that the real part of term $\tanh(\sqrt{A}W)/(\sqrt{A}W)$ is almost equal to 1 at low frequency,

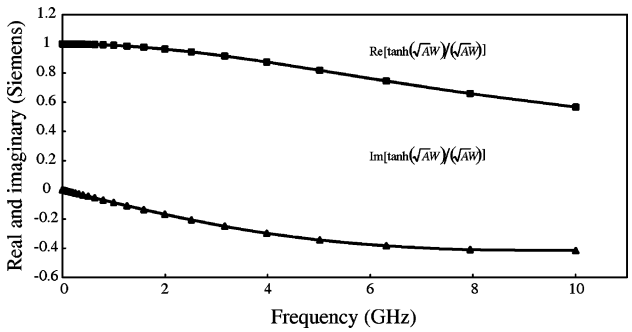

Fig. 5. Real and imaginary parts of $\tanh\sqrt{A}W/(\sqrt{A}W)$ as a function of frequency.

as shown in Fig. 5, C_{gd} can be obtained as:

$$C_{gd}=-\mathrm{Im}[Y_{12}]/\left(\mathrm{Re}\left[\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W}\right]w\right)=\mathrm{Im}[Y_{12}]/w \tag{33}$$

In addition, C_g can be obtained from Y_{11} at low frequency and shown as follows:

$$C_g=\mathrm{Im}[Y_{11}]/\left(\mathrm{Re}\left[\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W}\right]w\right)=\mathrm{Im}[Y_{11}]/w \tag{34}$$

With the extracted parameters C_g, we can obtain R_g by optimization to fit Eq. (25) to the experimental data Y_{11}. Then, in order to extract the transcapacitance C_m, C_{dg} has to be extracted first. At low frequency, from Eq. (32), C_{dg} can be obtained as:

$$C_{dg}=\mathrm{Im}[Y_{21}]/\left(\mathrm{Re}\left[\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W}\right]w\right)=\mathrm{Im}[Y_{21}]/w \tag{35}$$

Besides, based on the assumption that the term $s^2R_{sub}C_{db}C_{gb}/(1+sR_{sub}C_b)$ is extremely small for frequency up to 10 GHz, Eq. (28) can be re-expressed as

$$\begin{aligned}Y_{22}&\approx(g_m-sC_{dg})\left(1-\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W}\right)\left(\frac{C'_{gd}}{C'_g}\right)+g_{ds}\\&\quad+sC_{gd}+\frac{sC_{db}[1+g_{mb}R_{sub}+sR_{sub}(C_{sb}+C_{gb})]}{1+sR_{sub}C_b}\\&=Y_A+\frac{sC_{db}[1+g_{mb}R_{sub}+sR_{sub}(C_{sb}+C_{gb})]}{1+sR_{sub}C_b}\end{aligned} \tag{36}$$

where

$$Y_A=(g_m-sC_{dg})\left(1-\frac{\tanh(\sqrt{A}W)}{\sqrt{A}W}\right)\left(\frac{C'_{gd}}{C'_g}\right)+g_{ds}+sC_{gd}$$

Additionally, at low frequency, with the assumption $w^2R_{sub}^2C_b^2\ll1$, Eq. (36) can be approximated as [22]:

$$\begin{aligned}Y_{22}&\approx Y_A+w^2R_{sub}[C_b(C_{db}+g_{mb}R_{sub}C_{db})-C_{db}(C_{sb}+C_{gb})]\\&\quad+\mathrm{j}w[(C_{db}+g_{mb}R_{sub}C_{db})+w^2R_{sub}^2C_bC_{db}(C_{sb}+C_{gb})]\\&\approx Y_A+w^2R_{sub}C_{db}^2+\mathrm{j}wC_{db}\end{aligned} \tag{37}$$

In the Eq. (37), in order to obtain initial values of C_{db} and R_{sub}, we assume that $g_{mb}R_{sub}\ll1$. This assumption may slightly overestimate the values of C_{db} and R_{sub}, so they have to be corrected by optimization after substrate-related components (i.e. C_{gb}, C_b and g_{mb}) extracted. At first, we determine the initial values of C_{db} and R_{sub} from the imaginary and real parts of Y_{22} in Eq. (37) at low frequency, respectively, and shown as follows:

$$C_{db}=(\mathrm{Im}[Y_{22}]-\mathrm{Im}[Y_A])/w \tag{38}$$

$$R_{sub}=(\mathrm{Re}[Y_{22}]-\mathrm{Re}[Y_A])/(w^2C_{db}^2) \tag{39}$$

For the extraction of substrate-related components, C_{gb}, C_b and g_{mb}, Y_{sub} is first defined as follows

$$\begin{aligned}Y_{sub}&=Y_{22}-Y_A\approx\mathrm{j}w\frac{C_{db}(1+g_{mb}R_{sub})}{1+w^2R_{sub}^2C_b^2}\\&\quad+w^2\frac{R_{sub}C_{db}(g_{mb}R_{sub}C_b+C_{db})}{1+w^2R_{sub}^2C_b^2}\end{aligned} \tag{40}$$

where w^3-terms are negligible compared with the w-terms for operation frequency up to 10 GHz. The parameter g_{mb} can be obtained from the intercept of the relationship for $w/\mathrm{Im}[Y_{sub}]$ versus w^2 by Eq. (41) as follows:

$$\frac{w}{\mathrm{Im}[Y_{sub}]}=\frac{1}{C_{db}(1+g_{mb}R_{sub})}+w^2\frac{R_{sub}^2C_b^2}{C_{db}(1+g_{mb}R_{sub})} \tag{41}$$

Then, C_b is obtained from the slope of the relationship for $w^2/\mathrm{Re}[Y_{sub}]$ versus w^2 and shown as:

$$\begin{aligned}\frac{w^2}{\mathrm{Re}[Y_{sub}]}&=\frac{1}{R_{sub}C_{db}(R_{sub}g_{mb}C_b+C_{db})}\\&\quad+w^2\frac{R_{sub}^2C_b^2}{R_{sub}C_{db}(R_{sub}g_{mb}C_b+C_{db})}\end{aligned} \tag{42}$$

The remaining parameter C_{gb} is determined by optimization to fit Eq. (36) to the experimental data Y_{22}. The validity of the assumptions mentioned above (i.e. $w^2R_{sub}^2C_b^2\ll1$ at low frequency; $s^2R_{sub}C_{db}C_{gb}/(1+sR_{sub}C_b)$ is extremely small for frequency up to 10 GHz) will be checked after all parameters are extracted.

4. Verification with experiments and results discussion

In this section, the proposed direct extraction approach was applied to determine the parameters of the test device, which were n-MOSFETs fabricated by 0.18-μm technology. To obtain the Y-parameters of RF MOSFETs, S-para-meters were measured in the common-source configuration using an Agilent 8510C vector network analyzer and an on-wafer RF probe station. Before starting the measuring procedure, the calibration was performed on a ceramic calibration substrate using a SOLT calibration method. Besides, the measured data had to be corrected for parasitic capacitance of input/output pads and the resistances and inductances of

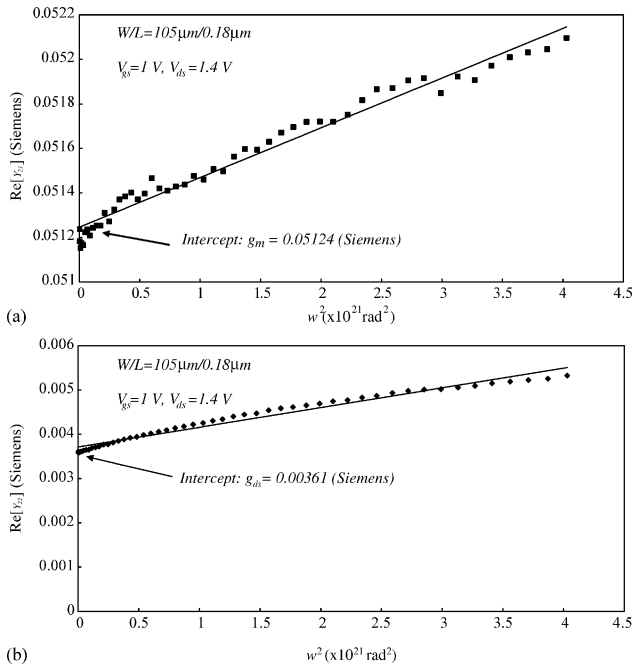

Fig. 6. The extraction results of transconductance g_m and channel conductance g_{ds} : (a) g_m is obtained from the y-intercept of Re[Y_{21}] versus $w2$ at low frequency, (b) g_{ds} is obtained from the y-intercept of Re[Y_{22}] versus w^2 at low frequency.

connection lines using two-step de-embedding technique [21]. The parameter extraction approach had been performed on the n-MOSFETs with 0.18-μm length and 105-μm width.

Fig. 6 shows the extraction results of transconductance g_m and channel conductance g_{ds} for an n-MOSFET device

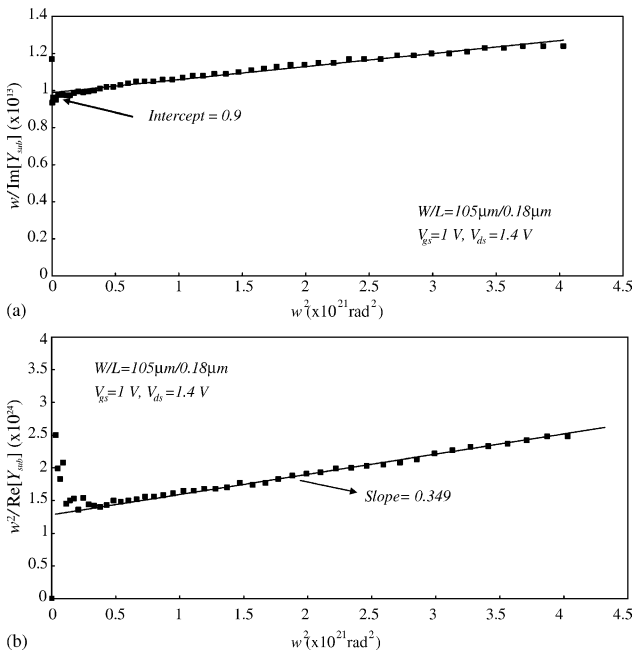

Fig. 7. (a) The extraction results of w/Im[Y_{sub}] as a function of w^2, where g_m can be determined from the y-intercept. (b) The extraction result of w^2/Re[Y_{sub}] as a function of w^2, where the C_b can be determined from the slope.

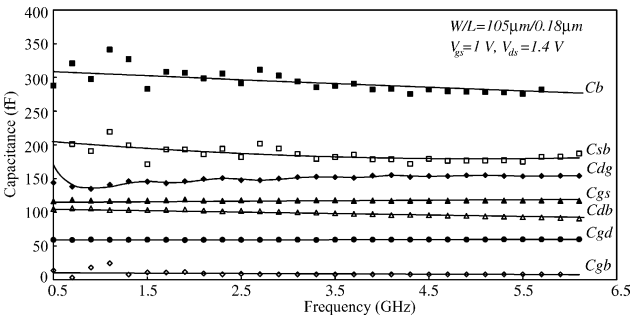

Fig. 8. Frequency dependence of the extracted capacitances for an n-MOSFET with 105 μm width and 0.18 μm length biased at $V_{gs} = 1$ V and $V_{ds} = 1.4$ V. The extracted capacitances remain almost constant with frequency and thus verify that the extraction method is reliable and accurate.

$W/L = 105/0.18$-μm biased at $V_{gs} = 1$ V and $V_{ds} = 1.4$ V. The transconductance g_m was obtained from the y-intercept of Re[Y_{21}] versus w^2 at low frequency, as shown in Fig. 6(a). In similarity, the channel conductance g_{ds} was obtained from the y-intercept of Re[Y_{22}] versus w^2 at low frequency, as shown in Fig. 6(b). In Fig. 7(a), g_{mb} can be obtained from the y-intercept of linear fit straight line of w/Im[Y_{sub}] versus w^2. In Fig. 7(b), C_b can be obtained from the slope of linear fit straight line of w^2/Re[Y_{sub}] versus w^2. Figs. 8 and 9 show the extracted parameters C_{gb}, C_b, C_{sb}, C_{db}, C_{gd}, C_{dg}, C_{gs}, R_g and R_{sub} as a function of frequency. They show that the extracted resistances and capacitances are frequency-independent and this result verifies that the proposed extraction approach is accurate and reliable. Furthermore, due to the charge-conservation and nonreciprocity, C_{dg} is larger than C_{gd}, as shown in Fig. 8. The extracted values of all parameters are summarized in Table 1. From the extracted parameters, the value of $w^2R_{sub}^2C_b^2$ is calculated to be 0.012 at 1 GHz, and the real and imaginary parts of $s^2R_{sub}C_{db}C_{gb}/(1 + sR_{sub}C_b)$ are calculated to be 8×10^{-5} and -8.6×10^{-5} at 10 GHz, respectively, which are much smaller than the ones of $g_m - jwC_{dg}$ and jwC_{gd}. Besides, for the extracted parameters listed in Table 1, the assumptions used in the approximations of Y_{12} and Y_{21} in the Eqs. (31) and (32)

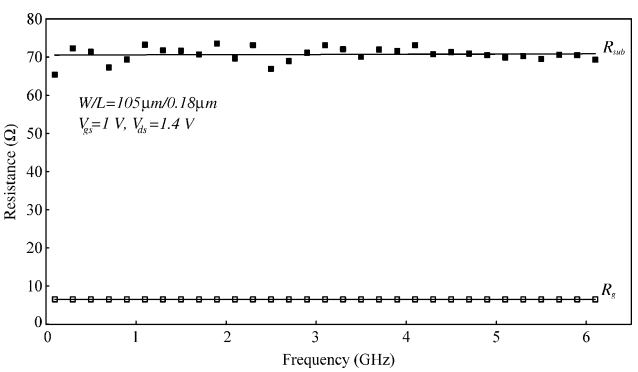

Fig. 9. Frequency dependence of the extracted resistances for an n-MOSFET with 105 μm width and 0.18 μm length biased at $V_{gs} = 1$ V and $V_{ds} = 1.4$ V.

Table 1
Table of the extracted small signal parameters for an *n*-MOSFET with 105 μm width and 0.18 μm length biased at $V_{ds} = 1.4$ V and different V_{gs}

V_{gs} (V)	0.6	1
C_{gs} (fF)	102	118.9
C_{gd} (fF)	58.5	60.45
R_g (Ω)	6.5	6.4
g_m (mS)	26.626	51.238
C_{dg} (fF)	85	140.3
R_{sub} (Ω)	59	60.7
C_{gb} (fF)	8.3	8
g_{mb} (mS)	3.543	3.92
C_{db} (fF)	80.1	90
C_{sb} (fF)	185	188
g_{ds} (mS)	1.3433	3.608

are valid for frequency up to 10 GHz. These results verify the validity of the assumptions made in the extraction approach.

In Fig. 10, the *Y*-parameters calculated with the extracted parameters are compared with measured data for two bias conditions: (1) $V_{gs} = 1$ V, $V_{ds} = 1.4$ V; and (2) $V_{gs} = 0.6$ V, $V_{ds} = 1.4$ V. It is shown that a good agreement was obtained between the simulation results and measured data. From Eq. (27), it is known that nonreciprocal capacitance C_{dg} contributes the accuracy in $\mathrm{Im}[Y_{21}]$ prediction. In Fig. 10(c), excluding the nonreciprocal capacitance C_{dg} resulting in a significant error in matching $\mathrm{Im}[Y_{21}]$ is observed, especially for larger V_{gs}. This is because C_{dg} increases with V_{gs}, being discussed latter.

Fig. 11(a) shows the gate bias dependence of the extracted capacitances for an *n*-MOSFET biased at $V_{ds} = 1.4$ V. As gate bias increases for constant V_{ds}, C_{gb} decreases due to the fact that the inversion status is getting stronger as V_{gs} increases. In other words, the ability of the inversion layer to protect the gate from the influence of the substrate is increasing as V_{gs} increases. In saturation region, C_{db} is dominated by junction capacitance and almost constant at fixed V_{ds}. C_{gd} and C_{gs} are composed of intrinsic capacitances C_{gdi}, C_{gsi} and overlap capacitances C_{gdo}, C_{gso}. C_{gd} is dominated by intrinsic capacitance C_{gdi} in the saturation region because the communication from the drain to the rest of the device is cut off owing to the pinch-off region. Furthermore, C_{dg} and C_m increase with V_{gs} due to the increase of intrinsic capacitance. Fig. 11(b) shows the gate bias dependence of the extracted resistances for an *n*-MOSFET biased at $V_{ds} = 1.4$ V. From the figure, it is shown that R_g and R_{sub} remain almost constant as V_{gs} increases.

The drain bias dependence of the extracted capacitances for an *n*-MOSFET biased at $V_{gs} = 1$ V. is shown in Fig. 12(a). As V_{ds} increases, C_{gb} increases because the influence of the substrate bias on the gate charge is increasing. Due to the increasing reverse bias between drain and substrate, C_{db} decreases as V_{ds} increases. In the saturation, C_{gs} and C_{gd} are dominated by the overlap capacitances C_{gdo}, C_{gso} and remain constant. Fig. 12(b) shows the drain bias dependence of the extracted resistances for an *n*-MOSFET biased at $V_{gs} = 1$ V. The extracted resistances R_g and R_{sub} are almost constant as V_{ds} increases. The bias dependence of transconductance g_m obtained

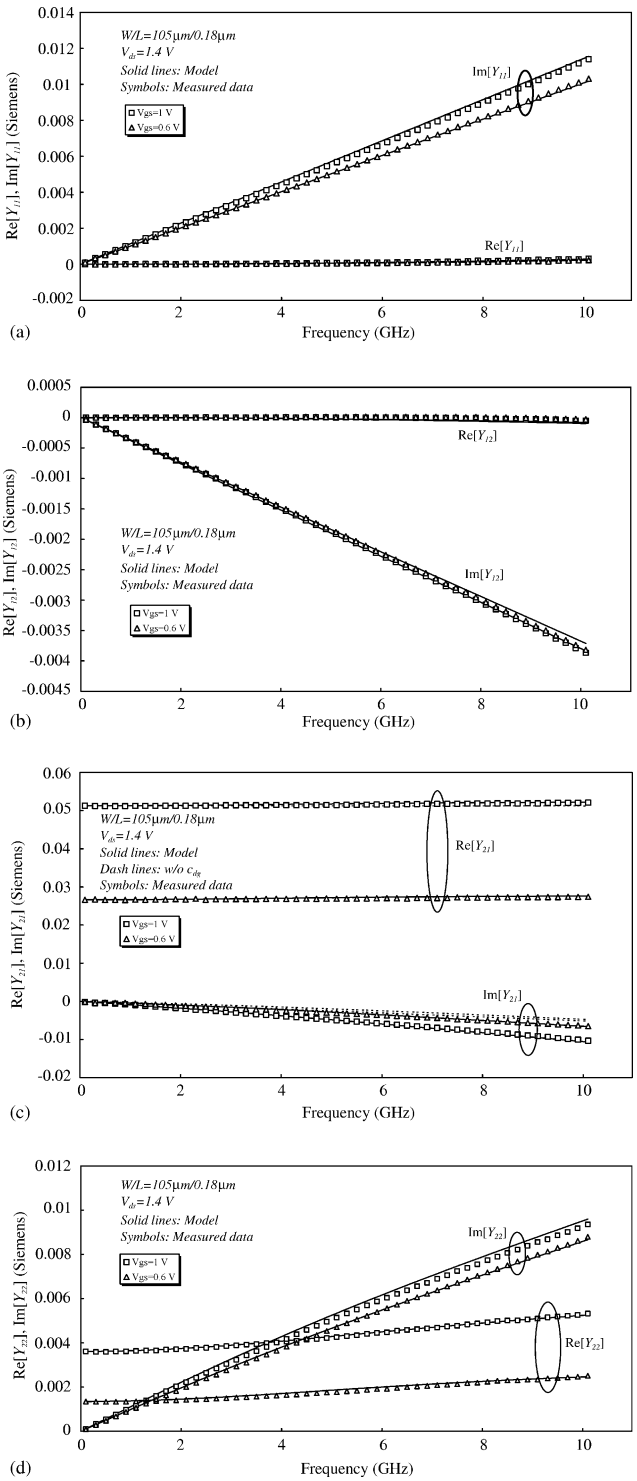

Fig. 10. Real and imaginary parts of *Y*-parameters: (a) Y_{11}; (b) Y_{12}; (c) Y_{21}; and (d) Y_{22} as a function of frequency for a device with 105 μm width and 0.18 μm length biased at $V_{gs} = 1$ V and $V_{ds} = 1.4$ V. The simulation results obtained by proposed model have a good agreement to the experimental data.

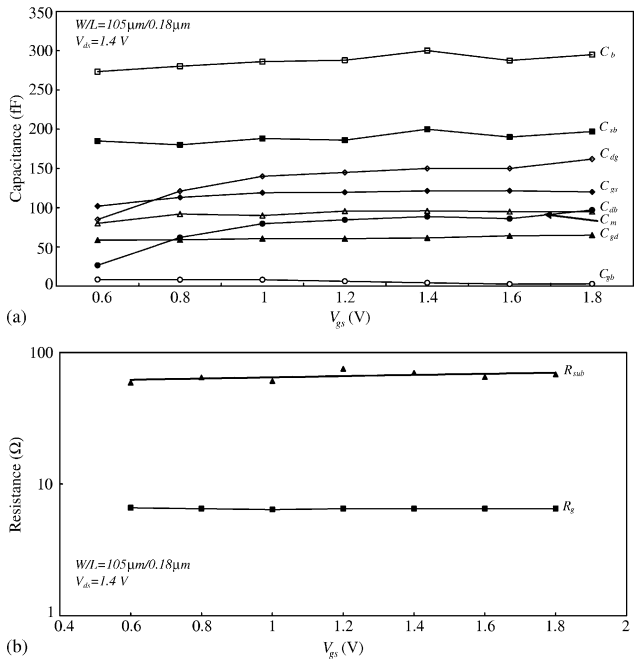

Fig. 11. Gate bias dependence of small-signal parameters for an *n*-MOSFET with 105 μm width and 0.18 μm length biased at $V_{ds} = 1.4$ V: (a) capacitances and (b) resistances.

from *Y*-parameters measurement and conventional DC measurement for an N-MOSFET is shown in Fig. 13. It can be seen that there is a good agreement between these two measurements. The results demonstrate that the DC- and AC-related parameters can be extracted by the proposed method in the HF analysis simultaneously. This extraction method avoids the possible error occurring in

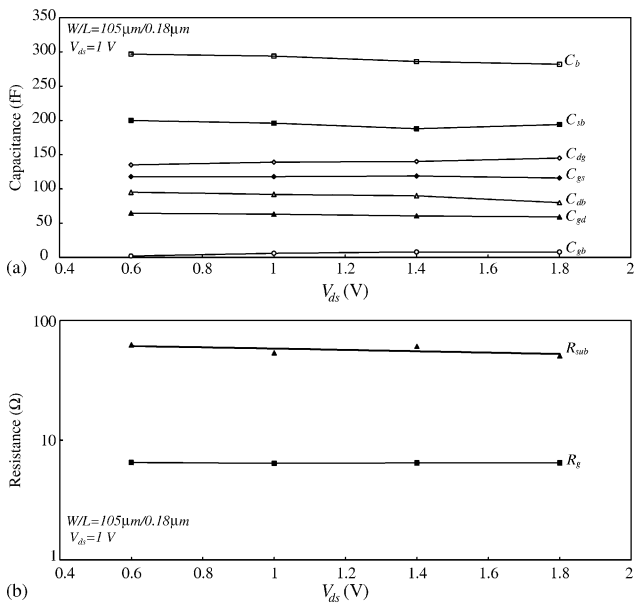

Fig. 12. Drain bias dependence of small-signal parameters for an *n*-MOSFET with 105 μm width and 0.18 μm length biased at $V_{gs} = 1$ V: (a) capacitances and (b) resistances.

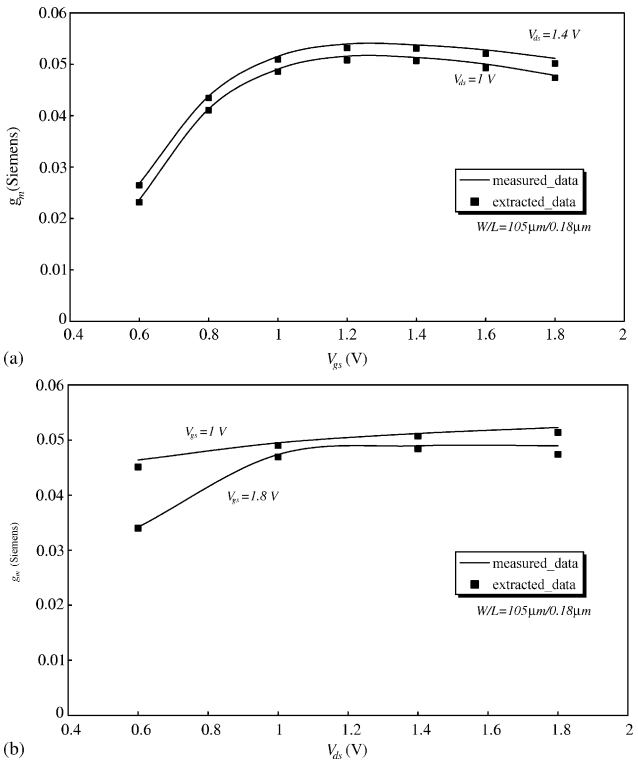

Fig. 13. The bias dependence of transconductance g_m obtained from *S*-parameters measurement by the proposed extraction method and from the conventional DC measurement for an *n*-MOSFET with 105 μm width and 0.18 μm length: (a) gate bias dependence and (b) drain bias dependence.

the conventional DC extraction method for transconductance g_m. This is because that conventional DC extraction method extracts g_m by differentiation of the I–V curves and this may cause a significant error.

5. Conclusions

In this paper, a new and accurate small signal model including distributed gate network, substrate network and nonreciprocal capacitance has been developed. Meanwhile, a direct extraction method for the parameters of the new model is also proposed. This model uses transmission line theorem to describe the distributed gate region, a single substrate resistance and relative capacitances to model the distributed substrate network and accounts for the nonreciprocal capacitance. In addition, an examination has done by using the measured data to verify the model and parameter extraction method. The extracted parameters are physical meaning and good agreements have been obtained between the simulation results and measured data. Furthermore, the extraction method was used to extract the transconductance g_m by *Y*-parameters analysis and verified by DC measurement data. The results demonstrated that the proposed extraction method is accurate and reliable.

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