A TaN–HfO_2–Ge pMOSFET With Novel SiH_4 Surface Passivation

Nan Wu, Qingchun Zhang, Chunxiang Zhu, *Member, IEEE*, D. S. H. Chan, *Senior Member, IEEE*, Anyan Du, N. Balasubramanian, M. F. Li, *Senior Member, IEEE*, Albert Chin, *Senior Member, IEEE*, Johnny K. O. Sin, *Senior Member, IEEE*, and D.-L. Kwong

***Abstract*—In this letter, we demonstrate a novel surface passivation process for HfO_2 Ge pMOSFETs using SiH_4 surface annealing prior to HfO_2 deposition. By using SiH_4 passivation, a uniform amorphous interfacial layer is formed after device fabrication. Electrical results show that the HfO_2 Ge MOSFET with Si-passivation exhibits less frequency dispersion, narrower gate leakage current distribution, and a $\sim 140\%$ higher peak mobility than that of the device with surface nitridation.**

***Index Terms*—Germanium, HfO_2, high-κ, MOSFET, surface passivation.**

I. Introduction

Germanium MOSFETs with high-κ gate dielectrics have received more and more attention for the future ultra-large scale integration (ULSI). Ge offers significant enhancements in bulk electron and hole mobility relative to Si. At the same time, it is also a candidate for supply voltage scaling due to its narrower band-gap than that of silicon. H. Shang *et al.* has recently reported germanium pMOSFETs [1] with up to 40% mobility enhancement compared to Si universal data. However, the gate dielectric used was GeON and the equivalent oxide thickness (EOT) is ~ 8 nm, which is not suitable for future ULSI. Besides, several works on Ge MOSFETs or MOS-CAPs [2]–[5] with sub-2-nm EOT have been reported by using HfO_2 recently. Because the deposition of high-κ material usually occurs in an oxidation ambient [6], [7], where germanium substrate could be oxidized and form the unstable germanium oxide [5], [8], it is a challenge to fabricate high-quality gate dielectrics on germanium substrate. NH_3 surface annealing prior to the HfO_2 deposition is a key step in recent demonstrations. However, the incorporation of nitrogen at the oxide/semiconductor interface has the potential of degrading the channel mobility [9]. In this letter, we demonstrate an alternative and robust surface passivation for HfO_2–Ge MOSFETs using SiH_4 annealing prior to the deposition of HfO_2.

Manuscript received June 3, 2004. This work was supported by a Singapore ASTAR R-263-000-267-305 grant. This review of this letter was arranged by Editor K. De Meyer.

N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, and M. F. Li are with the Silicon Nano Device Labpratory, Department of Electrical and Computer Engineering, National University of Singapore, Singapore, 119260 (e-mail: elezhucx@nus.edu.sg).

A. Du and N. Balasubramanian are with the Institute of Microelectronics, Singapore 117685.

A. Chin is with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 30050, Taiwan, R.O.C.

J. K. O. Sin is with the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Kowloon, Hong Kong.

D.-L. Kwong is with the Department of Electrical and Computer Engineering, University of Texas, Austin, TX 78712 USA.

Digital Object Identifier 10.1109/LED.2004.833842

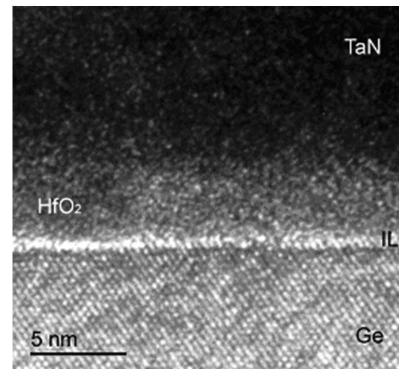

Fig. 1. High-resolution cross section TEM image of the TaN–HfO_2–Ge gate stack with Si-passivation. A uniform amorphous interface layer is observed due to SiO_x formation at the surface.

II. Fabrication

Ring-type pMOSFETs were fabricated on (100) n-type wafers (Sb doped, 0.04–0.08 Ω-cm). Wafers were first cleaned by diluted HF (1 : 50) and rinsed by DI water [2]. Wafers were then passivated in SiH_4 ambient [400 °C, with different duration, SiH_4 passivation, (SP)] [10]. To compare the effects of this surface treatment, the control wafers were annealed in NH_3 ambient [600 °C, 30-s surface nitridation (SN)] instead. After that, samples were transferred through loadlock into a metal-organic chemical vapor deposition (MOCVD) chamber under vacuum. The HfO_2 gate dielectric was then deposited in $O_2 + N_2$ using Hf tert-butoxide as the precursor at the temperature of 400 °C. Post-deposition anneal (PDA) was then performed in N_2 ambient at 550 °C (200 Torr) for several minutes. TaN gate electrode was deposited by reactively sputtering of Ta in N_2 + Ar ambient. Following that, lithography process and Cl_2 plasma dry etching were employed to define and pattern the gate stack. Wafers were then implanted with boron (35 keV, 1×10^{15} cm^{-2}) to form self-aligned source/drain (S/D). Dopant activation anneal was done in N_2 ambient at 420 °C. Finally, forming gas annealing was carried out at 300 °C.

III. Results and Discussion

Physical analysis has shown that the SiH_4 surface passivation on Ge is effective to meet the following criteria [10]: 1) Ge surface is fully covered by Si and free of germanium oxide forma-

0741-3106/04$20.00 © 2004 IEEE

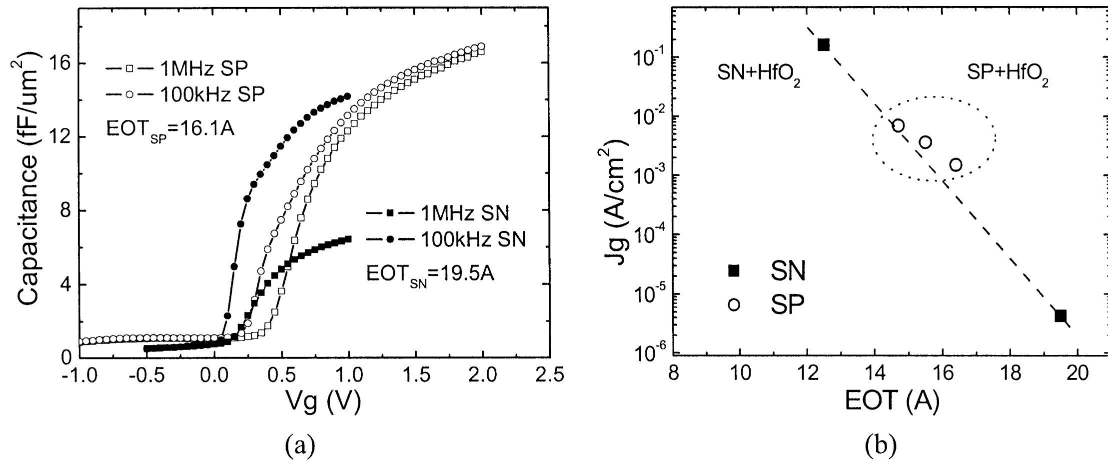

Fig. 2. (a) Typical *C–V*characteristics of Ge MOS capacitors with SN and SP processes at different frequencies. The SP processed device shows much improved frequency dispersion than the SN processed device. (b) Jg versus EOT of Ge MOS capacitors with different surface passivation.

tion; 2) comparable surface roughness between the as-cleaned sample and the passivated sample is observed; and 3) the Si passivation layer can be thin enough and consumed during the following HfO_2 deposition so that the MOSFET channel is still kept in Ge.

Fig. 1 shows the high-resolution transmission electron microscope (TEM) image of the TaN–HfO_2–Ge gate stack with 60-s Si-passivation. A uniform amorphous interfacial layer (IL) is observed. This is due to the fact that the Ge surface is fully covered with a very thin ($\sim$ a few monolayers) uniform elemental Si layer, and hence leads to SiO_x formation during the HfO_2 MOCVD and the subsequent thermal process [10]. It is also observed that the HfO_2 remains amorphous after device fabrication.

Typical capacitance–voltage (*C–V*) measurement results of the Ge MOS capacitors are shown in Fig. 2(a). For the device with SN process, the capacitance measured at 1 MHz drops almost to the half of that measured at 100 kHz in the accumulation region. On the contrary, the device with SP process exhibits much less frequency dispersion. This implies that the SP process could result in lower density of interface states [11]. EOT is extracted based on the 100-kHz result with quantum-mechanical corrections [12]. The EOTs for SP and SN MOS capacitors are 16.1 and 19.5 Å, respectively. Fig. 2(b) plots the $\mathrm{J_g at V_g} = 1\mathrm{V} + \mathrm{V_{fb}}$ versus the extracted EOT for different MOS capacitors. The SP processed devices have comparable oxide scaling capability with the SN processed devices.

The gate leakage currents of Ge MOS capacitors with different SP at 1-V gate bias were then measured and compared across the whole wafers. Devices were randomly selected and the accumulative probabilities were then plotted in Fig. 3. It is observed that the devices without any surface treatment are of large distribution in leakage current, which could be due to the formation of the unstable germanium oxide during the HfO_2 deposition. Post-deposition annealing leads to initial breakdown of the devices when there was no surface treatment. This is illustrated in Fig. 3 as the distribution with the highest leakage currents. The devices with SN exhibit an improved distribution. However, it is noticed that there is a tail in the distribution at low leakage region, where the tail has a similar slope as the de-

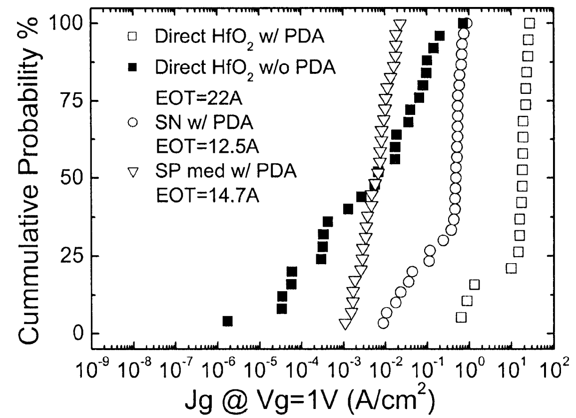

Fig. 3. Cumulative probabilities of the gate leakage currents of Ge MOS capacitors at $+1$ V gate bias. The SP processed devices show narrower leakage current distribution than the SN processed device.

vices with direct HfO_2 deposition (without post-deposition annealing). On the other hand, the devices with SP process show the narrowest distribution in leakage current, indicating that the SP process is more robust than the SN process. The improved leakage distribution is believed to be resulted from the significant suppression of the unstable germanium oxide formed at the interface [10], as well as the uniform amorphous interfacial layer after the SP process.

Typical output characteristics of the pMOSFETs with both SP and SN processes are compared in Fig. 4. The EOTs are 15.5 and 12.5 Å for the devices with SP and with SN, respectively. The SP processed pMOSFET shows a $\sim 56.4\%$ higher drive current than the device with SN at bias of $\mathrm{V_{gs} - V_{th}} = -1.2$ V and $\mathrm{V_{ds}} = -1.5$ V. The effective mobility (μ_{eff}) was extracted using the split *C–V* technique [1]. The channel current under different gate bias was estimated by $(I_D + I_S)/2$, with the $\mathrm{V_{DS}} = -50$ mV [13]. The charge was extracted from *C–V* measurement at 100 kHz. The effective electric field normal to the channel was then estimated as $\mathrm{E_{eff}} = (\mathrm{Q_B} + \mathrm{Q_n}/3)/(\varepsilon_{\mathrm{Ge}}\varepsilon_0)$, where $\mathrm{Q_B}$ is the depletion charge and $\mathrm{Q_n}$ is the inversion charge. Fig. 5 plots the μ_{eff} versus the $\mathrm{E_{eff}}$ for both the SN and SP processed devices. The SP processed device exhibits a much higher effective hole mobility than that of the SN pro-

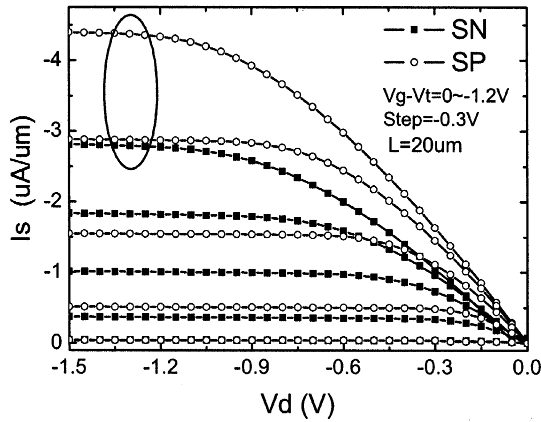

Fig. 4. I_d–V_d characteristics of the pMOSFETs with different surface passivation.

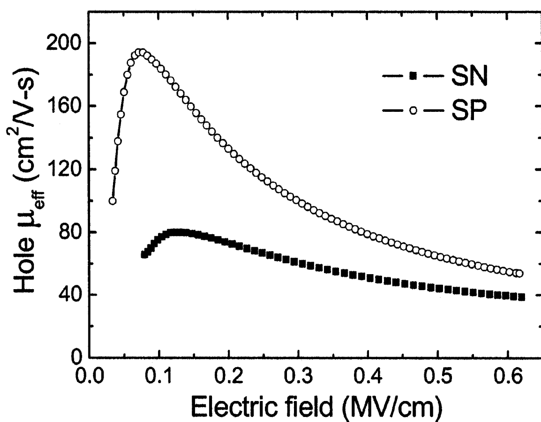

Fig. 5. Measured hole mobility of the pMOSFETs with different surface passivation.

cessed device. The peak hole mobility for SN and SP processed MOSFET are 79.9 cm^2/V-s and 194.1 cm^2/V-s, respectively. An $\sim$ 140% improvement in peak hole mobility was achieved in SP processed Ge MOSFET compared to the SN processed Ge MOSFET.

IV. Conclusion

In summary, TaN–HfO_2–Ge pMOSFETs with a novel surface passivation using SiH_4 have been demonstrated. Improved electrical performance of the MOS capacitors can be obtained by using SiH_4 passivation instead of SN in terms of frequency dispersion and gate leakage distribution. In addition, the SP processed device shows a $\sim$ 140% higher peak mobility of holes than the SN processed device does.

References

[1] H. Shang, H. Okorn-Schimdt, J. Ott, P. Kozlowski, S. Steen, E. C. Jones, and H.-S. P. Wong, "Eletrical characterization of germanium p-channel MOSFETs," *IEEE Electron Device Lett.*, vol. 24, pp. 245–247, May 2003.

[2] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, "Ge MOS characteristics with CVD HfO_2 dielectrics and TaN gate electrode," in *Proc. 2003 Symp. VLSI Technology*, 2003, pp. 121–122.

[3] A. Ritenour, S. Yu, M. L. Lee, N. Lu, W. Bai, A. Pitera, E. A. Fitzgerald, D. L. Kwong, and D. A. Antoniadis, "Epitaxial strained germanium p-MOSFET's with HfO_2 gate dielectric and TaN gate electrode," in *IEDM Tech. Dig.*, 2003, pp. 433–436.

[4] C. O. Chui, H. Kim, P. C. McIntyre, and K. C. Saraswat, "A germanium NMOSFET process integrating metal gate and improved hi-k dielectrics," in *IEDM Tech. Dig.*, 2003, pp. 437–440.

[5] N. Wu, Q. Zhang, C. Zhu, C. C. Yeo, S. J. Whang, D. S. H. Chan, M. F. Li, B. J. Cho, A. Chin, D.-L. Kwong, A. Y. Du, C. H. Tung, and N. Balasubramanian, "Effect of surface NH_3 anneal on the physical and electrical properties of HfO_2 films on Ge substrate," *Appl. Phys. Lett.*, vol. 84, pp. 3741–3743, 2004.

[6] M. Cho, J. Park, H. B. Park, C. S. Hwang, J. Jeong, and K. S. Hyun, "Chemical interaction between atomic-layer-deposited HfO_2 thin films and the Si substrate," *Appl. Phys. Lett.*, vol. 81, pp. 334–336, 2002.

[7] J. Park, B. K. Park, M. Cho, C. S. Hwang, K. Oh, and D. Y. Yang, "Chemical vapor deposition of HfO_2 thin films using a novel carbon-free precursor: Characterization of the interface with the silicon substrate," *J. Electrochem. Soc.*, vol. 149, pp. G89–G94, 2002.

[8] Y. Z. Hu, J.-T. Zettler, S. Chongsawangvirod, Y. Q. Wang, and E. A. Irene, "Spectroscopic ellipsometric measurements of the dielectric function of germanium dioxide films on crystal germanium," *Appl. Phys. Lett.*, vol. 61, pp. 1098–1100, 1992.

[9] H.-J. Cho, C. S. Kang, K. Onishi, S. Gopalan, R. Nieh, R. Choi, E. Dharmarajan, and J. C. Lee, "Novel nitrogen profile engineering for improved TaN/HfO_2/Si MOSFET performance," in *IEDM Tech. Dig.*, 2001, pp. 30.2.1–30.2.4.

[10] N. Wu, Q. Zhang, C. Zhu, D. S. H. Chan, M. F. Li, N. Balasubramanian, A. Chin, and D.-L. Kwong, "An alternative surface passivation process on germanium for metal–oxide–semiconductor applications with high-κ gate dielectric," *Appl. Phys. Lett.*, submitted for publication.

[11] H. Kim, C. O. Chui, K. C. Saraswat, and P. C. McIntyre, "Local epitaxial growth of ZrO_2 on Ge (100) substrates by atomic layer epitaxy," *Appl. Phys. Lett.*, vol. 83, pp. 2647–2649, 2003.

[12] T. Low, Y. T. Hou, M. F. Li, C. Zhu, D.-L. Kwong, and A. Chin, "Germanium MOS: An evaluation from carrier quantization and tunneling current," in *Proc. 2003 Symp. VLSI Technology*, 2003, pp. 117–118.

[13] S.-i. Takagi and M. Takayanagi, "Experimental evidence of inversion-layer mobility lowering in ultrathin gate oxide metal-oxide-semiconductor field-effect-transistors with direct tunneling current," *Jpn. J. Appl. Phys.*, vol. 41, pp. 2348–2352, 2002.