Suppression of the Floating-Body Effect in Poly-Si Thin-Film Transistors With Self-Aligned Schottky Barrier Source and Ohmic Body Contact Structure

Po-Yi Kuo, Tien-Sheng Chao, Senior Member, IEEE, and Tan-Fu Lei

Abstract—In this letter, we developed a new self-aligned Schottky barrier source and ohmic body contact (SSOB) method that can effectively suppress the floating-body effect in poly-Si thin-film transistors (TFTs). Experimental results show that the SSOB-TFTs give higher output resistance, less threshold voltage variation, improved subthreshold characteristics, and larger breakdown voltage compared with conventional TFTs. The characteristics of the SSOB-TFTs are suitable for high-performance driving TFTs with a high output resistance and large breakdown voltage.

Index Terms—Floating-body effect, kink effect, ohmic body contact, poly-Si TFTs, Schottky barrier source.

I. INTRODUCTION

OLYCRYSTALLINE silicon thin-film transistors (poly-Si TFTs) are key devices in active-matrix liquid crystal displays (AMCLDs). Due to the relatively-large field-effect mobilities in both n- and p-channel devices, poly-Si TFTs can be used to incorporate the integrated driving circuits in AMLCDs [1]. Recently, poly-Si TFTs are suitable for the pixel driving elements of active matrix organic light-emitting diode (AM-OLED) [2], and the driving TFTs with a high output resistance are desirable. However, the output characteristics exhibit an anomalous current increase in the saturation regime, often called a "kink" effect [3], [4] due to an analogy with silicon-on-insulator (SOI) devices [5]. This phenomenon can be attributed to the floating-body effect [6] and the avalanche multiplication enhanced by grain boundary-traps [7]. The avalanche multiplication is caused by the high drain electric field and the presence of grain boundaries and traps enhances the kink effect in poly-Si TFTs [7]. The added drain current enhances impact ionization which leads to a premature breakdown in return [6]. Several structures, such as lateral body terminal (LBT) [8], low-barrier body-contact (LBBC) [9], and Schottky body contact [10] have been reported in order to reduce the kink current. However, LBT needs an additional terminal for the body bias; LBBC needs additional implantation

Manuscript received June 14, 2004. This work was supported by the National Science Council of Taiwan, R.O.C. under Contract NSC-92-2215-E-009-060. The review of this letter was arranged by Editor J. Sin.

P.-Y. Kuo and T.-F. Lei are with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 30050, Taiwan, R.O.C.

T.-S. Chao is with the Department of Electrophysics, National Chiao-Tung University, Hsinchu 30050, Taiwan, R.O.C. He is also with the National Nano Device Laboratory, National Chiao Tung University, Hsinchu 30050, Taiwan, R.O.C.

Digital Object Identifier 10.1109/LED.2004.834635

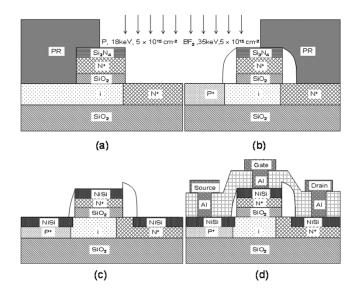


Fig. 1. Key processes of the SSOB-TFTs: (a) $\rm n^+$ drain-side implantation; (b) $\rm p^+$ body-contact implantation; (c) Ni-salicidation and Schottky barrier source formation; and (d) poly-Si TFTs with SSOB after contact and metallization processes.

processes and thicker channel thickness for the body contact; and the high-forward-bias turn-on voltage of the Schottky diode was reported using Schottky body contact. Among these structures, Schottky barrier MOSFETs (SB-MOSFETs) are thought to have some advantages over conventional MOSFETs, such as the reduction of parasitic resistance and capacitance, and the immunity to the short channel [11], latch-up, or SOI floating-body effects [12].

In this letter, we have developed a self-aligned Schottky barrier source and ohmic body contact (SSOB) method for contacting the body terminal of poly-Si TFTs and forming the silicided source applicable to technologies that incorporate self-aligned silicide cladded junctions. The new structure provides a very effective body contact to suppress all undesirable floating-body effects. Various device parameters, such as subthreshold characteristics, output characteristics, and breakdown voltage, are compared with conventional poly-Si TFTs.

II. EXPERIMENT

The key processes to fabricate the SSOB-TFTs are shown in Fig. 1. First, a 50-nm amorphous silicon (a-Si) layer was deposited by low-pressure chemical vapor deposition (LPCVD) at 550 °C on oxidized silicon wafers. Next, the a-Si layer was then recrystallized by solid-phase crystallization (SPC) at 600 °C

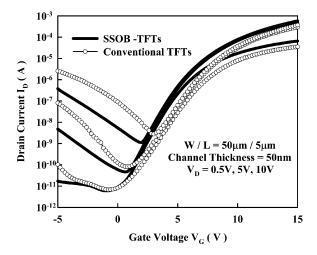


Fig. 2. Transfer characteristics of the conventional and the SSOB-TFTs with $W/L=50~\mu{\rm m}/5~\mu{\rm m}$.

for 24 h. After the active region patterning, a 50-nm gate oxide layer was deposited by high-density plasma chemical vapor deposition at 350 °C. Subsequently, a 150-nm in situ n⁺ doped a-Si layer and a 150-nm Si₃N₄ hard mask layer were deposited by LPCVD. After defining gate electrode, the remaining oxide on source/drain regions was removed by diluted HF. A mask was used to perform the n⁺ drain-side implantation with P⁺ to dose 5×10^{15} cm⁻² and energy 18 keV [Fig. 1(a)]. A 250-nm oxide sidewall spacer was formed by deposition and etching of TEOS oxide. A similar mask was used to perform the p⁺ doped body-contact BF₂ implantation with dose 5×10^{15} cm⁻² and moderate energy 35 keV. This implantation serves to form a p⁺ junction below the Schottky barrier source for ohmic body contact and also improves the conductivity at the bottom of the source for better body current collection simultaneously [Fig. 1(b)]. Meanwhile, only source- side oxide spacer was removed by buffered oxide etch (BOE). After removing the photoresist of body-contact mask, the Si₃N₄ hard mask layer was then selectively etched in a hot phosphoric acid bath. A second 25-nm oxide sidewall spacer was again formed by deposition and etching of TEOS oxide. Dopants were activated by rapid thermal annealing (RTA) at 750 °C for 20 s. A Ni film of about 10 nm was deposited by sputtering after a dilute HF-dip and then Ni-salicidation was carried out at 500 °C for 30 s by one-step RTA in the N_2 ambient. Unreacted Ni was removed in H_2SO_4 : H₂O₂ solution. The Schottky barrier source was formed by the Ni-salicidation [Fig. 1(c)]. After contact and the metallization processes, the resultant poly-Si TFT with SSOB was shown in Fig. 1(d). Conventional devices with self-aligned n⁺ source/drain and without Ni-salicidation were also fabricated to serve as control ones. No further hydrogenation procedures were implemented after sintering at 400 °C for 30 min.

III. RESULTS AND DISCUSSION

The measured transfer characteristics of the conventional and the SSOB-TFTs with $W/L=50~\mu\mathrm{m}/5~\mu\mathrm{m}$ are shown in Fig. 2. The off-state leakage currents in the conventional TFTs are slightly higher than that in the SSOB-TFTs. Fig. 2 also displays that the threshold voltage V_{TH} (defined as

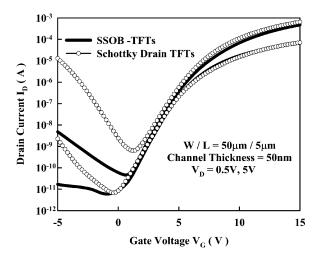


Fig. 3. Transfer characteristics of the Schottky drain and the SSOB-TFTs with $W/L=50~\mu{\rm m}/5~\mu{\rm m}$.

 $I_D = W/L \times 100 \text{ nA}$) is 6.9 V and 6.1 V for the conventional TFTs at $V_{\rm DS} = 0.5~{\rm V}$ and $V_{\rm DS} = 10~{\rm V}$, respectively. However, $V_{\rm TH}$ is 5.4 V and 5.2 V in the SSOB-TFTs at $V_{\rm DS}=0.5$ V and $V_{\rm DS}=10~{\rm V}$, respectively. Since the hole accumulation at the channel increases the body potential and lowers the junction barrier at the source region, a large number of hole carriers may be collected by the source. The leakage current is the sum of the electron current by field-emission at the drain region and the hole current caused by p-n forward bias at source [8]. With this ohmic body contact, the hole accumulation in the body and parasitic bipolar effects can be eliminated, resulting in a stable $V_{\rm TH}$ [9], [13] and lower off-state leakage current in the SSOB-TFTs [14]. The benefit of the SSOB-TFTs also can be found on subthreshold swing (S.S.). The S.S. of the conventional and the SSOB-TFTs are about 1230 mV/dB and 1100 mV/dB, respectively. We believe that it may be due to the shallow silicided source junction and p⁺ junction in the SSOB-TFTs.

To prove asymmetric S/D embedded in our SSOB structure, devices were measured again with interchanged S/D, i.e., Schottky drain TFTs with Schottky barrier drain and n⁺ source. Fig. 3 shows the transfer characteristics of the Schottky drain and the SSOB-TFTs with $W/L=50~\mu\text{m}/5~\mu\text{m}$. Notably, the subthreshlod and on-state transfer characteristics for both devices are almost the same, except for gate-induced-drain-leakage (GIDL)-like currents when V_G was at negative bias. Normally, GIDL-like currents were often found for Schottky drain TFTs due to holes tunneling to the channel from drain metal silicide [15]. The GIDL-like currents become significant at the stronger accumulation region and higher drain voltage in the Schottky drain TFTs. This GIDL-like current can be three orders of magnitude reduced by the n⁺ drain in the SSOB-TFTs.

The measured output characteristics of the conventional, the Schottky drain and the SSOB-TFTs are shown in Fig. 4. The kink effect of the SSOB-TFTs is considerably reduced compared with the conventional and the Schottky drain TFTs. Under high drain voltage, excessive holes are accumulated at the body region and the drain breakdown is reduced by the floating-body

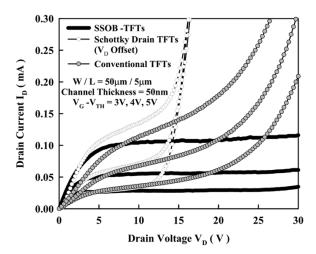


Fig. 4. Output characteristics of the conventional, the Schottky drain, and the SSOB- TFTs with $W/L=50~\mu\mathrm{m}/5~\mu\mathrm{m}$.

effect in the conventional TFTs [16], [17]. This hole accumulation causes a profound kink effect, which in turn deteriorates the output characteristics and induces parasitic bipolar transistor action [18], [19]. Since the SSOB-TFTs effectively collect the hole current generated by impact ionization, the floating-body effect is significantly suppressed and breakdown voltage is increased. Fig. 4 also indicates that the output characteristics of the Schottky drain TFTs have a finite drain voltage offset which is considered to arise from the Schottky barrier formed between the Schottky barrier drain and $\rm n^+$ inversion layer [20]. The low breakdown voltage $(V_D \sim 15~\rm V)$ and kink-like current for Schottky drain TFTs may result from the inherent p-i-n diode forward biased at $V_D > 0~\rm V$.

IV. CONCLUSION

We have developed a self-aligned SSOB structure for poly-Si TFTs to provide an effective body contact and suppress the floating-body effect. The GIDL-like currents occurred in the Schottky drain TFTs are reduced by the SSOB-TFTs. These SSOB-TFTs show a reduced kink effect and increased breakdown voltage and are suitable for driving circuit applications for high-voltage gain.

ACKNOWLEDGMENT

The authors would like to thank the Nano Facility Center (NFC) of National Chiao-Tung University and the National Nano Device Laboratory (NDL) for providing process equipment.

REFERENCES

- [1] S. D. Brotherton, "Polycrystalline silicon thin film transistors," *Semiconduct. Sci. Technol.*, vol. 10, pp. 721–738, 1995.
- [2] T. Shimoda, H. Ohshima, S. Miyashita, M. Kimura, T. Ozawa, I. Yudasaka, H. Kobayashi, R. H. Friend, J. H. Burroughes, and C. R. Towns, "High resolution light emitting polymer display driven by low temperature polysilicon thin film transistor with integrated driver," in *Proc. ASID*, Seoul, Korea, 1998, pp. 217–220.
- [3] G. A. Armstrong, S. D. Brotherton, and J. R. Ayres, "A comparison of the kink effect in polysilicon thin film transistors and silicon on insulator transistors," *Solid-State Electron.*, vol. 39, no. 9, pp. 1337–1346, Sept. 1996
- [4] C. Reita, P. Migliorato, A. Pecora, G. Fortunato, and L. Mariucci, "Analysis of short channel effects in poly-Si thin-film transistors: A new method," *Microelectron. Eng.*, vol. 19, pp. 183–186, 1992.
- [5] J. P. Colinge, "Reduction of kink effect in thin-film SOI MOSFETs," IEEE Electron Device Lett., vol. 9, pp. 97–99, May 1988.
- [6] M. Valdinoci, L. Colalongo, G. Baccarani, G. Fortunato, A. Pecora, and I. Policicchio, "Floating body effects in polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 44, pp. 2234–2241, Dec. 1997.
- [7] M. Hack and A. G. Lewis, "Avalanche-induced effects in polysilicon thin-film transistors," *IEEE Electron Device Lett.*, vol. 12, pp. 203–205, May 1991.
- [8] J. S. Yoo, C. H. Kim, M. C. Lee, M. K. Han, and H. J. Kim, "Reliability of low temperature poly-Si TFT employing counter-doped lateral body terminal," in *IEDM Tech. Dig.*, 2000, pp. 217–220.
- [9] M. Chan, B. Yu, Z. J. Ma, C. T. Nguyen, C. Hu, and P. K. Ko, "Comparative study of fully depleted and body-grounded non fully depleted SOI MOSFET's for high performance analog and mixed signal circuits," *IEEE Trans. Electron Devices*, vol. 42, pp. 1975–1981, Nov. 1995.
- [10] J. W. Sleight and K. R. Mistry, "DC and transient characterization of a compact Schottky body contact technology for SOI transistors," *IEEE Trans. Electron Devices*, vol. 46, pp. 1451–1456, July 1999.
- [11] J. R. Tucker, C. Wang, and P. S. Carney, "Silicon field-effect transistor based on quantum tunneling," *Appl. Phys. Lett.*, vol. 65, pp. 618–620, 1994.
- [12] M. Nishisaka and T. Asano, "Reduction of the floating body effect in SOI MOSFET's by using Schottky source/drain contacts," *Jpn. J. Appl. Phys.*, vol. 37, pp. 1295–1299, 1998.
- [13] T. Ichimori and N. Hirashita, "Fully-depleted SOI CMOSFET's with the fully-silicided source/drain structure," *IEEE Trans. Electron Devices*, vol. 49, pp. 2296–2300, Dec. 2002.
- [14] H. F. Wei, J. E. Chung, N. M. Kalkhoran, and F. Namavar, "Suppression of parasitic bipolar effects and off-state leakage in fully-depleted SOI n-MOSFET's using Ge-implantation," *IEEE Trans. Electron Devices*, vol. 42, pp. 2096–2103, Dec. 1995.
- [15] Y. Zhang, J. Wan, K. L. Wang, and B. Y. Nguyen, "Design of 10-nm-scale recessed asymmetric Schottky barrier MOSFETs," *IEEE Electron Device Lett.*, vol. 23, pp. 419–421, July 2002.
- [16] S. Yamada, S. Yokoyama, and M. Koyanagi, "Two-dimensional device simulation for avalanche induced short channel effect in poly-Si TFT," in *IEDM Tech. Dig.*, 1990, pp. 859–862.
- [17] M. Yoshimi, M. Takahashi, T. Wada, K. Kato, S. Kambayashi, M. Kemmochi, and K. Natori, "Analysis of the drain breakdown mechanism in ultra-thin-film SOI MOSFET's," *IEEE Trans. Electron Devices*, vol. 37, pp. 2015–2021, Sept. 1990.
- [18] A. G. Lewis, T. Y. Huang, R. H. Bruce, M. Koyanagi, A. Chiang, and I. W. Wu, "Polysilicon thin film transistor for analogue circuit applications," in *IEDM Tech. Dig.*, 1988, pp. 264–267.
- [19] K. P. A. Kumar, J. K. O. Sin, C. T. Nguyen, and P. K. Ko, "Kink-free polycrystalline silicon double-gate elevated-channel thin-film transistors," *IEEE Trans. Electron Devices*, vol. 45, pp. 2514–2520, Dec. 1998.
- [20] K. Uchida, K. Matsuzawa, J. Koga, S. Takagi, and A. Toriumi, "Enhancement of hot-electron generation rate in Schottky source metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 76, pp. 3992–3994, 2000.