Lateral Migration of Trapped Holes in a Nitride Storage Flash Memory Cell and Its Qualification Methodology

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***Abstract*—The negative threshold voltage (V_t) shift of a nitride storage flash memory cell in the erase state will result in an increase in leakage current. By utilizing a charge pumping method, we found that trapped hole lateral migration is responsible for this V_t shift. Hole transport in nitride is characterized by monitoring gate induced drain leakage current and using a thermionic emission model. The hole emission induced V_t shift shows a linear correlation with bake time in a semi-logarithm plot and its slope depends on the bake temperature. Based on the result, an accelerated qualification method for the negative V_t drift is proposed.**

***Index Terms*—Lateral migration, MXVAND, NBit, nitride storage, NROM, trapped hole.**

I. Introduction

By UTILIZING channel hot electron injection and band-to-band hot hole injection as programming and erasing methods, respectively, injected electrons and holes will be locally trapped in a nitride layer of an *"NBit"* cell in a multiplex virtual ground AND (MXVAND) array [1], and two bits per cell operation is therefore achieved [2]. Since the charge storage material of *Nbit* cells is different from that of conventional floating gate flash devices, the understanding of data retention loss mechanisms in these nitride storage devices is critical to the improvement of the device reliability. Though the cells have been demonstrated to possess excellent intrinsic electron retention [3], the data retention loss caused by electron leakage via stress created oxide traps is still a reliability concern after program/erase (P/E) cycling. A V_g acceleration method [1] and a temperature acceleration test [4] are proposed for qualification of the *NBit* devices in its program state. In contrast to electrons, we observe a stronger temperature dependence of hole-lateral transport in the nitride layer in an over-erased cell [5]. This lateral spread of trapped holes results in channel shortening, thus causing a negative threshold voltage (V_t) shift and an increase of leakage current in a memory array [5]. Since the negative V_t shift is related to the short-channel effect, this issue becomes more serious in a scaled device. In this paper, the hole lateral migration effect is demonstrated by using charge pumping measurement. In addition, by monitoring the band-to-band tunneling current, trapped hole emission is investigated at various temperatures. Finally, an accelerated qualification methodology is proposed for such negative V_t drift. An *NBit* cell with $L_g = 0.46$ μm and $W_g = 0.38$ μm was used in this study. The thickness of each ONO layer is 9 (top oxide), 6 (nitride), and 5 nm, respectively.

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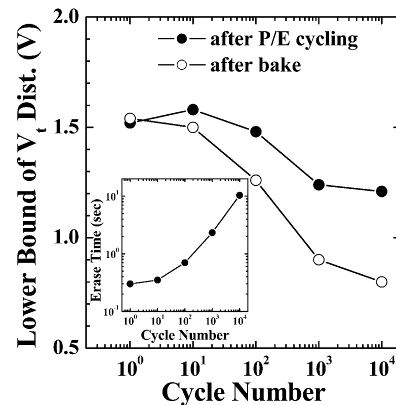

Fig. 1. Lowest bound of erase state V_t distribution versus cycle number before and after bake at 150 °C for 168 h. The required erase time to pass erase-verify is plotted in the inset.

II. Experimental

In Fig. 1, the lowest bound of erase state V_t distribution versus cycle number was shown before and after bake at 150 °C for 168 h. The test sample size is a sector of 512 K cells, which are at "all 1 pattern," i.e., all in erase state. It is found that the V_t drifts toward a more negative value as cycling number increases. In the inset of Fig. 1, we plot the required erase time for the entire sector to pass erase-verify. The increase of erase time with cycle number is due to the location mismatch of injected electrons and holes [6]. In order to compensate for stored electrons far in the channel region, more hole injection is needed in erase operation. In other words, to obtain a similar erase V_t, more holes are accumulated in the nitride layer as cycle number increases. This implies that the larger negative V_t drift in an erased cell after P/E cycling is related

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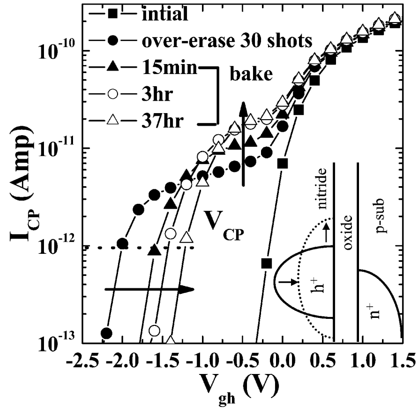

Fig. 2. Charge pumping characteristics of a fresh memory cell, after 30 erase shots, and subsequently after bake of 15 min, 3 h, and 37 h at 150 °C, respectively. Schematic drawing of hole lateral spread is also drawn.

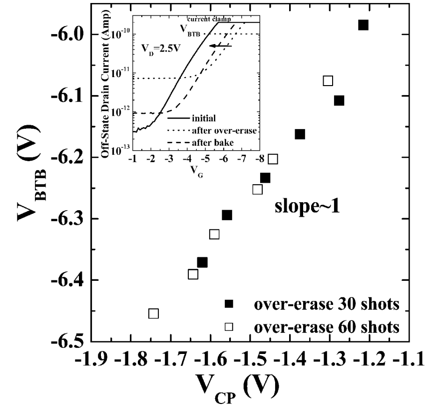

Fig. 3. $V_{\rm BTB}$ is plotted against $V_{\rm cp}$. A positive correlation is found between them. In the inset, the evolution of $V_{\rm BTB}$ is shown. The $V_{\rm BTB}$ is defined as gate voltage to have an off-state drain current of 100 pA at $V_{\rm d} = 2.5$ V.

to trapped holes in the nitride layer. To further characterize the negative drift of V_t, a charge pumping method [7], which is able to probe the lateral distribution of trapped charges, is used. A trapezoidal pulse train with a fixed low level ($V_{\rm gl}$) and successively increasing high levels ($V_{\rm gh}$) is applied to the gate. The pulse frequency is 2.5 MHz. The substrate, the source, and the drain are grounded. The charge pumping current $I_{\rm cp}$ versus $V_{\rm gh}$ is measured. The $V_{\rm gl}$ is sufficiently low to ensure that the entire channel is in accumulation. By varying $V_{\rm gh}$, only the part of the channel that undergoes inversion-accumulation-inversion over a pulse cycle can contribute to $I_{\rm cp}$. To emulate the erase time effect as shown in Fig. 1 and to avoid excess interface trap generation after P/E cycling and their annealing during bake, a fresh cell is intentionally over-erased by 30 erase-shots instead. The charge-pumping result is shown in Fig. 2. The generated interface traps during erase are negligible since the $I_{\rm cp}$ at $V_{\rm gh} = 1.5$ V is almost unchanged. Because a considerable amount of holes are trapped in the nitride after erase, a leftward shift of the low $V_{\rm gh}$ portion (for $V_{\rm gh} < 0$ V) of the $I_{\rm cp}$ characteristic [7] is observed. The local threshold voltage in the hole injection region is reduced to around -2 V. Here, we also define a parameter $V_{\rm cp}$, which is the $V_{\rm gh}$ corresponding to $I_{\rm cp} = 1$ pA. $V_{\rm cp}$ reflects the maximum hole density in the nitride. The cell is then baked at 150 °C. A crossover of the $I_{\rm cp}$ characteristics before and after bake is observed. The $V_{\rm cp}$ shifts rightward with bake time. In addition, $I_{\rm cp}$ between $V_{\rm gh} = -1.5$ V and $V_{\rm gh} = -0.5$ V increases. This increased $I_{\rm cp}$ is opposed to interface trap annealing effect. To explain the observed $I_{\rm cp}$ characteristics, the lateral movement of holes is depicted in the figure. After bake, the peak trapped hole density decreases and thus the $V_{\rm cp}$ shifts rightward. On the other hand, the trapped hole region extends due to the hole lateral spread in the nitride. Thus, the corresponding $I_{\rm cp}$ for $V_{\rm gh} < -0.5$ V increases due to a larger channel region contributing to $I_{\rm cp}$. In short, the negative V_t shift can be explained in the following. Holes are firstly thermally emitted from the traps to the valence band (or conducting shallow states) and then laterally drifted by an internal field and re-captured by other nitride traps during bake. The spreading of holes enlarges the low V_t region and causes channel length shortening. The cells' V_t is therefore reduced.

III. Qualification Methodology

A. Measurement

Since the V_t loss depends on both hole lateral spreading and the change of the local trapped hole density, which is a complicated two-dimensional (2-D) effect, it is not a suitable indicator to investigate the acceleration method. For example, with the same extent of hole lateral migration, the cell V_t is not affected in a long-channel device while it is significantly reduced in a short-channel device. Therefore, the $V_{\rm BTB}$ [8], [9] and the $V_{\rm cp}$ are adopted to monitor the temporal evolution of trapped hole density instead. The $V_{\rm BTB}$ is defined as the gate voltage when the band-to-band tunneling current is 100 pA at $V_{\rm d} = 2.5$ V, as illustrated in the inset of Fig. 3. Regardless of number of over-erase shots, a positive correlation is found between $V_{\rm cp}$ and $V_{\rm BTB}$ in Fig. 3. In other words, a consistent result is obtained from these two methods.

B. Model

According to the thermionic emission model, the emission time constant τ_ϕ of a hole in a trap with trap energy ϕ above the nitride valence band can be described as [10], [11]

$$\tau_\phi(T) = \frac{1}{AT^2}\exp\left(\frac{\phi}{kT}\right)$$
$$A = 2\sigma_{\rm h}\left(\frac{3k_B}{m_{\rm h}^*}\right)^{1/2}\left(\frac{2\pi m_{\rm h}^* k_B}{h^2}\right)^{3/2} \quad (1)$$

where $\sigma_{\rm h}$ is the capture cross-section of the hole trap and $m_{\rm h}^*$ is the effective hole mass in the nitride. Other variables have their usual definitions. It follows from (1) that

$$\phi = \ln[AT_1^2\tau_\phi(T_1)]^{kT_1} = \ln[AT_2^2\tau_\phi(T_2)]^{kT_2}$$
$$\tau_\phi(T_1) = \frac{1}{AT_1^2}[AT_2^2\tau_\phi(T_2)]^{kT_2/kT_1}. \quad (2)$$

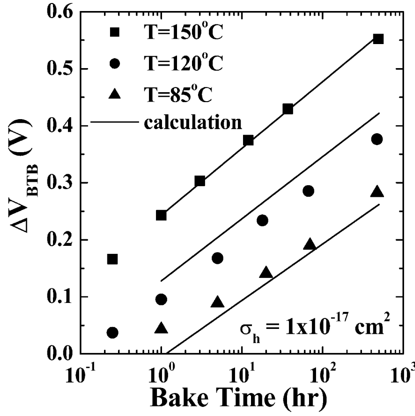

Fig. 4. $\Delta V_{\rm BTB}$ versus bake time at various temperatures. All curves follow a straight line on a semi-log scale. The solid lines represent calculation result.

Assuming the trapped holes have a continuous distribution in energy and the trapped hole density is a constant, the emitted positive charge $\mathrm{Q_h}$ is then derived as

$$Q_{\rm h}=\int_0^t J dt'=\int_0^t\int_0^{E_G} \frac{qN_{\rm h}\exp\left(\frac{-t'}{\tau_\phi}\right)}{\tau_\phi} d\phi dt' \propto qN_{\rm h}kT\log(t) \quad (3)$$

where $\mathrm{N_h}$ is the volumetric trapped hole density in the nitride layer, J is the current density resulting from the emitted holes, and E_G is the band gap value of the nitride film. Equation (3) indicates that the time-dependence of the trapped holes density due to the thermionic emission should follow a straight line on a semi-log scale and the slope is proportional to the temperature. In measurement, the variation of $\mathrm{Q_h}$ is monitored by the $\Delta V_{\rm BTB}$ due to a positive correlation between them [8], [9].

C. Model Result

In Fig. 4, the $\Delta V_{\rm BTB}$ versus bake time at various temperatures is plotted. All curves follow a straight line on a semi-log scale. The solid lines represent calculation result with $\sigma_{\rm h}$ in (1) and the proportionality constant in (3) as fitting parameters. The extracted capture cross-section $\sigma_{\rm h}$ of holes is about $1\times10^{-17}\ \mathrm{cm}^2$. In calculation, $\mathrm{m_h^*} = 0.5\mathrm{m_0}$ is used. Based on this result, the temperature dependence and the time dependence can be predicted. In practice, the acceleration test for the negative V_t drift at $\mathrm{T} = 150\,^\circ\mathrm{C}$ is required to pass 114 h to meet the ten years of data retention at $\mathrm{T} = 85\,^\circ\mathrm{C}$.

IV. Conclusion

In this paper, the hole lateral migration effect of an *NBit* cell in erase state is investigated. A negative V_t shift is found to increase with cycling number and will be a potential issue for future device scaling. According to the thermionic emission model, the hole emission effect should exhibit a logarithm dependence on bake time and a linear dependence on bake temperature. The extracted hole capture cross section is about $1\times10^{-17}\ \mathrm{cm}^2$. Therefore, to achieve ten years of data retention at $\mathrm{T} = 85\,^\circ\mathrm{C}$, acceleration test at $\mathrm{T} = 150\,^\circ\mathrm{C}$ for 114 h is required.

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