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Interface-blocking mechanism for reduction of threading dislocations in SiGe and Ge epitaxial layers on Si(100) substrates

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A mechanism of interface blocking was proposed to reduce the threading dislocations in the SiGe and Ge layers on Si(100) substrates. In this work, epitaxial $Si_{1-x}Ge_x/Si_{1-(x-y)}Ge_{x-y}$ and Ge/Si_yGe_{1-y} layers were grown by UHV/CVD. It was surprisingly found that if the variation of the Ge composition, y, across the interface of $Si_{1-x}Ge_x/Si_{1-(x-y)}Ge_{x-y}$ or Ge/Si_yGe_{1-y} is higher than a certain value, most of the threading dislocations appear to be blocked and confined in the underlying $Si_{1-(x-y)}Ge_{x-y}$ or Si_yGe_{1-y} layer by the interface. It implies that this finding can provide a simple way to grow high-quality relaxed SiGe and Ge layers on the Si substrates. © *2004 American Vacuum Society.* [DOI: 10.1116/1.1781188]

I. INTRODUCTION

Heterostructures of SiGe and Ge epitaxial layers on Si substrates have attracted considerable attention due to their potential device applications[1] and compatibility with Si-based technology. In particular, strain-relaxed SiGe and Ge layers provide a virtual substrate for the growth of high-electron-mobility structures and for the integration of III–V devices on Si. In addition, the integration of Ge with Si is of much importance for the application of Ge photodetectors. The major problems of these relaxed layers are the high density of threading dislocations and the high surface roughness arising from the 4.2% lattice mismatch between Ge and Si. Various growth techniques and treatments have been developed to solve these problems. It has been reported that the compositionally graded buffer (CGB) layers,[2] low-temperature Si buffer layers,[3] compliant silicon-on-insulator (SOI) substrate,[4] two-step procedure,[5] and selective area growth combined with thermal cycle annealing[6] can be used to grow high-quality strain-relaxed SiGe and Ge layers. Among them, the CGB layers are the most practically and widely used ones today. However, the CGB layers still have two major challenges. First, these CGB layers often suffer from a thickness of ~ 10 μm with a Ge composition grading from 0 to 1.0, which increases crucially the price of SiGe devices and hinders their integration with conventional Si-based circuits. Second, the CGB layers often exhibit a cross-hatch pattern, which makes the surfaces very rough.[7]

It has been[8] reported earlier that the strained isoelectronically In-doped GaAs layer grown on GaAs wafers allow one to reduce the dislocations density drastically, where the authors found that the interface formed between the In-doped GaAs layer and GaAs substrate can bend the dislocations. We believe that a similar mechanism can be easily used to grow SiGe and Ge layers with reduced dislocation densities on the Si(100) substrates.

II. EXPERIMENT

In our laboratory, the epitaxial SiGe and Ge layers were grown by UHV/CVD equipment using silane and germane as the Si and Ge sources. Usually, growth temperature of 550 °C was used to grow $Si_{1-x}Ge_x$ layers with $x<0.3$, and 420 °C was used to grow Ge layer and $Si_{1-x}Ge_x$ layer with $x>0.8$. The samples in this work were grown based on two structures (see Fig. 1). For the structure (a), a $Si_{1-(x-y)}Ge_{x-y}$ was first grown. After *in situ* annealing it at 950 °C for 5 min for strain relaxation, a second layer $Si_{1-x}Ge_x$ was then grown. For the structure (b), a Si_yGe_{1-y} was first grown. After *in situ* annealing it at 750 °C for 15 min for strain relaxation, a Ge layer was subsequently grown. Finally, an annealing of 750 °C for 15 min was performed again for removing of defects that possibly generate in the Ge layer grown at low temperature. Transmission electron microscopy (TEM) was used to observe the dislocation distribution and

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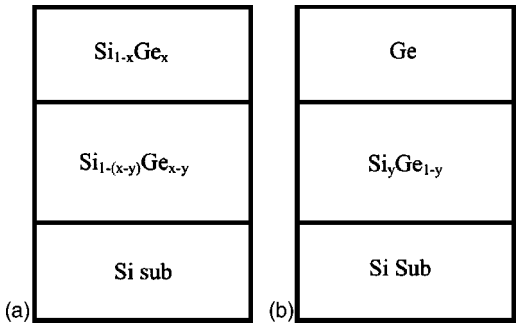

FIG. 1. Samples structures (a) and (b); their detail growth conditions were described in context.

interaction with the interfaces. These TEM measurements were carried out on a Philips Tecnai 20 microscope. The crystalline quality of Ge layer was additionally evaluated by the double-crystal x-ray diffraction (DCXD) measurement.

III. RESULTS AND DISCUSSION

Figure 2 is a cross-sectional TEM (XTEM) image of a sample on which was grown directly a $Si_{0.8}Ge_{0.2}$ layer about 7500 Å. No measure was taken to control the dislocations. This sample was also annealed at 950 °C for 5 min for its full relaxation. From the image, a large number of threading dislocations are observed to generate from the interface of $Si_{0.8}Ge_{0.2}/Si$ and continue through the entire epitaxial layer to the surface.

Figure 3 is an XTEM image of a sample on which was grown an epitaxial structure of $Si_{0.76}Ge_{0.24}/Si_{0.8}Ge_{0.2}$ in which the first $Si_{0.8}Ge_{0.2}$ layer is about 1.2 μm thick, and the second $Si_{0.76}Ge_{0.24}$ layer is about 0.5 μm thick. It is seen that some threading dislocations that generate within the first $Si_{0.8}Ge_{0.2}$ layer are blocked by the interface of $Si_{0.76}Ge_{0.24}/Si_{0.8}Ge_{0.2}$, but others still penetrate through the interface to the top layer.

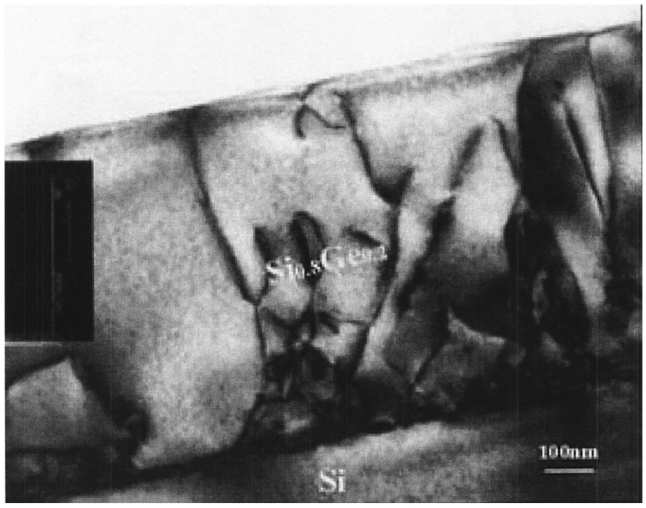

FIG. 2. XTEM image of $Si_{0.8}Ge_{0.2}/Si$; dislocations distribute in the entire epitaxial layer.

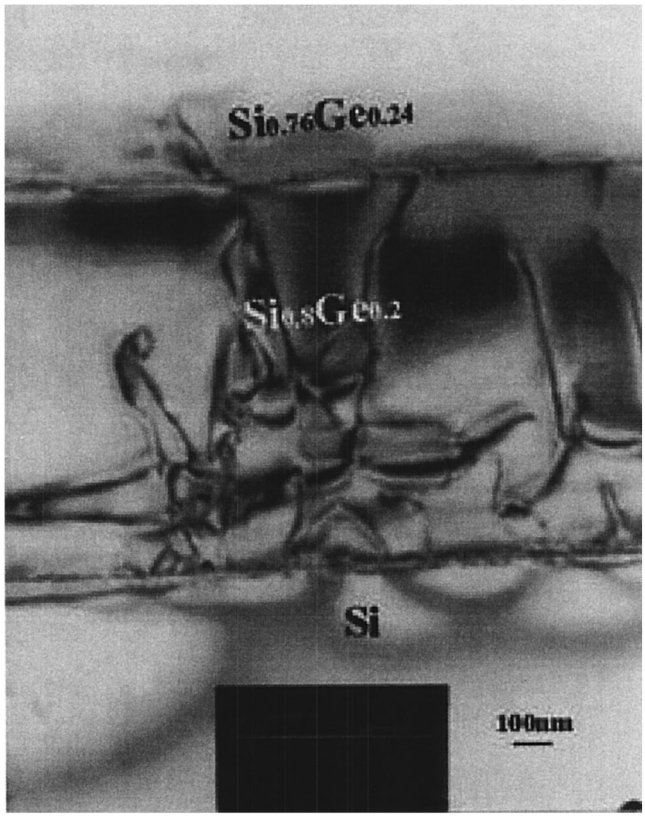

FIG. 3. XTEM image of $Si_{0.76}Ge_{0.24}/Si_{0.8}Ge_{0.2}/Si$; some dislocations are blocked by the interface, but the other dislocations penetrate the interface.

However, for the sample on which was grown an epitaxial structure of $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}$ in which the first $Si_{0.8}Ge_{0.2}$ layer is about 1.2 μm thick, and the second $Si_{0.7}Ge_{0.3}$ layer is about 0.6 μm thick, it is seen that the dislocations that generate within the first $Si_{0.8}Ge_{0.2}$ layer are remarkably blocked by the interface of $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}$. The threading dislocations that can penetrate through the interface are much reduced (see Fig. 4).

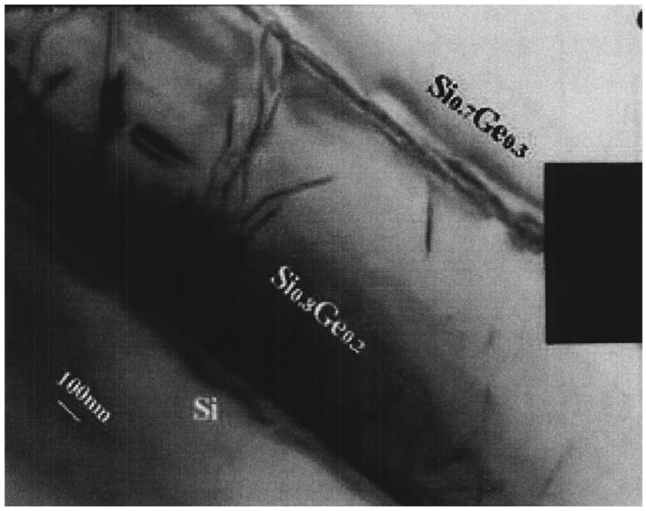

FIG. 4. XTEM image of $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}/Si$ almost all the dislocations are blocked by the interface of $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}$.

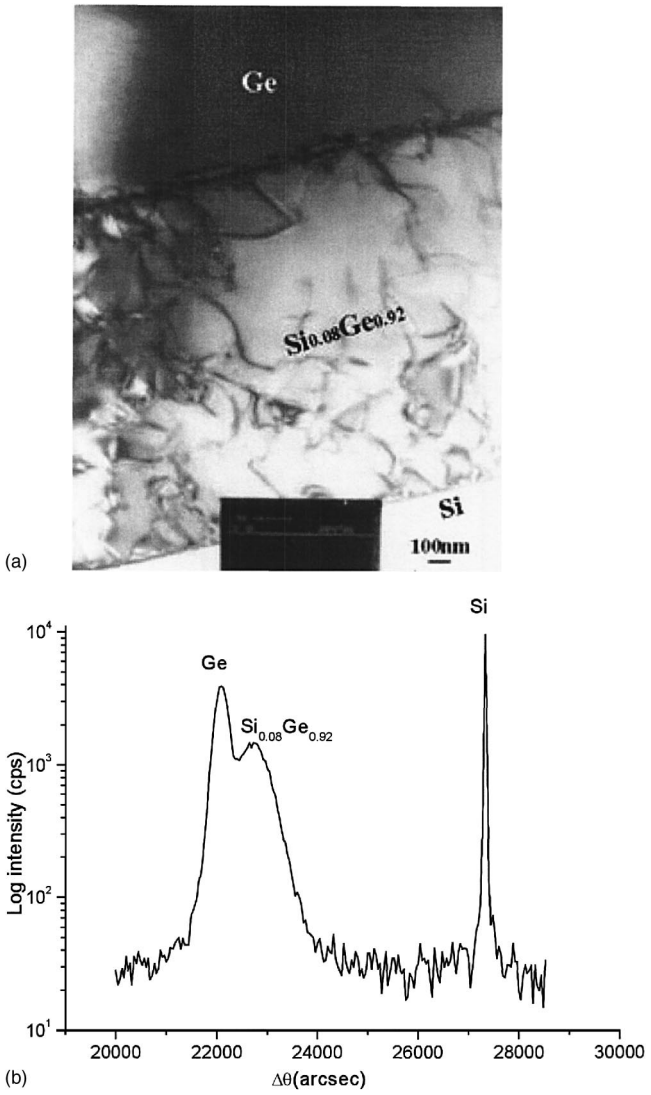

FIG. 5. (a) XTEM image of $Ge/Si_{0.08}Ge_{0.92}/Si$; high-density of dislocations are blocked effectively by the interface of $Ge/Si_{0.08}Ge_{0.92}$; (b) double-crystal x-ray diffraction result for this sample.

Figure 5(a) is an XTEM of a sample on which the first layer is a 1.5 μm thick $Si_{0.08}Ge_{0.92}$ layer, and the second layer is a 1.0 μm thick Ge layer. It is surprisingly found that the high-density dislocations that generate within the $Si_{0.08}Ge_{0.92}$ layer are also blocked drastically by the interface of $Ge/Si_{0.08}Ge_{0.92}$. The top Ge layer exhibits a good crystalline quality with a low threading dislocation density. Under the optical microscope, by counting the etch pits that were selectively etched by solution of $CH_3COOH:HNO_3:HF:I_2 = 67\ ml:20\ ml:10\ ml:30\ mg$ for 10 s, we estimated that the dislocation density in this top Ge layer is about $6 \times 10^6/cm^2$. Figure 5(b) is the DCXD result for this sample. The peak of Ge is sharp, which also implies that the crystalline quality of the top Ge layer is superior. Moreover, the total thickness of these two layers is only about 2.5 μm, which is much less than that of traditional CGB structure.

The mechanism of interface blocking of dislocations is considered to be due to the dislocation bending behavior under the stress field. When the stress field around the interface is strong enough, the dislocation can be bent and traverse along the interface. From the XTEM images, it can be found that the interfaces of $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}$ and $Ge/Si_{0.08}Ge_{0.92}$ (see Figs. 4 and 5) are rough. It implies that a strong nonuniform stress field exists at these interfaces. When the dislocations in these two samples meet the interfaces, they can be blocked very effectively. The phenomenon of dislocation bending under the stress can also be found in other material structures such as the GaN lateral overgrowth on the sapphire substrate reported by Ref. 9 recently, where the authors observed many dislocations bend at the edges of the GaN ridge due to the stress distributed there.

IV. CONCLUSION

In conclusion, a mechanism of interface blocking was proposed to reduce the threading dislocations in the SiGe and Ge layers on Si(100) substrates. When the variation of the Ge composition, y, across the interface of $Si_{1-x}Ge_x/Si_{1-(x-y)}Ge_{x-y}$ or Ge/Si_yGe_{1-y} is higher than a certain value, most of the threading dislocations appear to be blocked and confined in the underlying $Si_{1-(x-y)}Ge_{x-y}$ or Si_yGe_{1-y} by the interface. For samples of $Si_{0.7}Ge_{0.3}/Si_{0.8}Ge_{0.2}/Si$ ($y=0.1$) and $Ge/Si_{0.08}Ge_{0.92}/Si$ ($y=0.08$), both top layers show low dislocation densities. It implies that the mechanism of interface blocking can be easily used to control the dislocations for growth of the relaxed SiGe and Ge layers on the Si substrates.

[1] D. J. Paul, Adv. Mater. (Weinheim, Ger.) **11**, 191 (1999).
[2] S. B. Samavedam and E. A. Fitzgerald, J. Appl. Phys. **81**, 3108 (1997).
[3] C. S. Peng, H. Chen, Z. Y. Zhao, J. H. Li, D. Y. Dai, Q. Huang, J. M. Zhou, Y. H. Zhang, C. H. Tung, T. T. Sheng, and J. Wang, J. Cryst. Growth **201**, 530 (1999).
[4] Y. H. Luo, J. L. Liu, G. Jin, J. Wan, K. L. Wang, C. D. Moore, M. S. Goorsky, C. Chih, and K. N. Tu, Appl. Phys. Lett. **78**, 1219 (2001).
[5] A. Sakai, K. Sugimoto, T. Yamamoto, M. Okada, H. Ikeda, Y. Yasuda, and S. Zaima, Appl. Phys. Lett. **79**, 3398 (2001).
[6] H. C. Luan, D. R. Lim, K. K. Lee, K. M. Chen, J. G. Sandland, K. Wada, and L. C. Kimerling, Appl. Phys. Lett. **75**, 2909 (1999).
[7] S. Yu. Shiryaev, F. Jenson, and J. W. Peterson, Appl. Phys. Lett. **64**, 3305 (1994).
[8] H. Beneking, Cryst. Prop. Prep. **31**, 21 (1991).
[9] T. S. Kuan, C. K. Inoki, Y. Hsu, D. L. Harris, R. Zhang, S. Gu, and T. F. Kuech, MRS Internet J. Nitride Semicond. Res. **5S1**, W2.6 (2000).