Investigation on Device Characteristics of MOSFET Transistor Placed Under Bond Pad for High-Pin-Count SOC Applications

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***Abstract*—In the system-on-a-chip (SOC) era, chip layouts of integrated circuit (IC) products become more and more compact for cost reduction. To save layout area for SOC chips, on-chip electrostatic discharge (ESD) protection devices or input/output (I/O) transistors placed under bond pads is a good choice. To ensure that this choice is practicable, a test chip with large size NMOS devices placed under bond pads had been fabricated in a 0.35-μm 1P4M 3.3-V CMOS process for verification. The bond pads of this test chip had been drawn with different layout patterns on the interlayer metals for two purposes. One is to investigate the efficiency against bonding stress applied on the active devices under the bond pads. The other purpose is to reduce the parasitic capacitance of bond pads for high-speed or high-frequency circuit applications. DC characteristics of these devices placed under bond pads had been measured under three conditions: before wire bonding, after wire bonding, and after thermal reliability stresses. After assembled with wire bond package and thermal reliability stresses, the measured results show that there are only little variations between devices under bond pads and devices beside bond pads. This result can be applied to save layout area of IC products by realizing on-chip ESD protection devices or I/O transistors under the bond pads, especially for the high-pin-count SOC.**

***Index Terms*—Bond pad, leakage current, temperature cycling test, thermal shock test.**

I. Introduction

LAYOUT design on bond pads was often ignored in integrated circuit (IC) design flow in the past, because the chip design was not pushed to its limitation when using the conventional bond pad structure. As device feature sizes of IC technologies are shrunk more rapidly than the size of bond pad, and the number of input/output (I/O) pins increases for more complex interfaces, the layout area occupied by bond pads in a silicon chip is getting larger. The increasing I/O pins and their layout area lead to more complex interconnection and increase of die cost. If the active devices of a chip can be placed under bond pads, the I/O cell area would obviously be reduced and the design flexibility would be also improved.

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In general chip designs, active devices would not be placed under bond pads, because circuit designers cannot make sure whether the device characteristics are still acceptable, or not, after the stress of the packaging process. To make sure whether devices placed under bond pads are all right or not, there have been some reports done in the past [1]–[4]. Among those reports, studies of the bonding stress induced gate leakage current [1], reliability degradation indicated by increased failure percentage after reliability stresses [2], [3], and second breakdown voltage variation [4] of devices placed under bond pads had been investigated. Besides, bond pads have been designed with some change from the conventional bond pad structure [5], [6]. To improve the bonding reliability, the metal layer beneath the most top metal layer of bond pad is suggested to be patterned [5]. To reduce the parasitic effect for high-frequency I/O circuits, the low-capacitance bond pad structure had been reported with different layout patterns [6]. If the active devices can be safely placed under such low-capacitance bond pads, the I/O circuits can be drawn with more area efficiency for high-speed or high-frequency I/O interface applications.

In this paper, the active devices under such low-capacitance bond pad structures to save layout area are studied and experimentally verified in a 0.35-μm CMOS process.

II. Test Chip Design to Verify Devices Under Bond Pads

To understand whether if the NMOS transistor placed under bond pad would be damaged by the wire bonding process or not, one set of bond pad designs with NMOS transistors has been fabricated in a 0.35-μm 1P4M 3.3-V CMOS process [7]. Bond pads used in this verification are all with a passivation window size of 86×86 μm and top metal size of 96×96 μm. Besides, bond pad pitch in the silicon test chip is 116 μm. All the NMOS transistors in the silicon test chip are drawn with the same feature size and layout style. The layout of the NMOS transistor is drawn in 21 fingers with each unit finger width of 96 μm. The NMOS transistor has its total channel width of 2016 μm ($[96\ \mu\text{m/finger}] \times [21\ \text{fingers}] = 2016\ \mu\text{m}$) and channel length of 0.5 μm. Each terminal of the drain, gate, source, and bulk of the NMOS transistor is connected to a standalone bond pad in the silicon test chip.

The first bond pad device design, called as "Device-1" in this work, is constructed by four bond pads in line and a NMOS transistor placed between two of these bond pads. This conventional NMOS transistor layout, where the NMOS transistor is placed

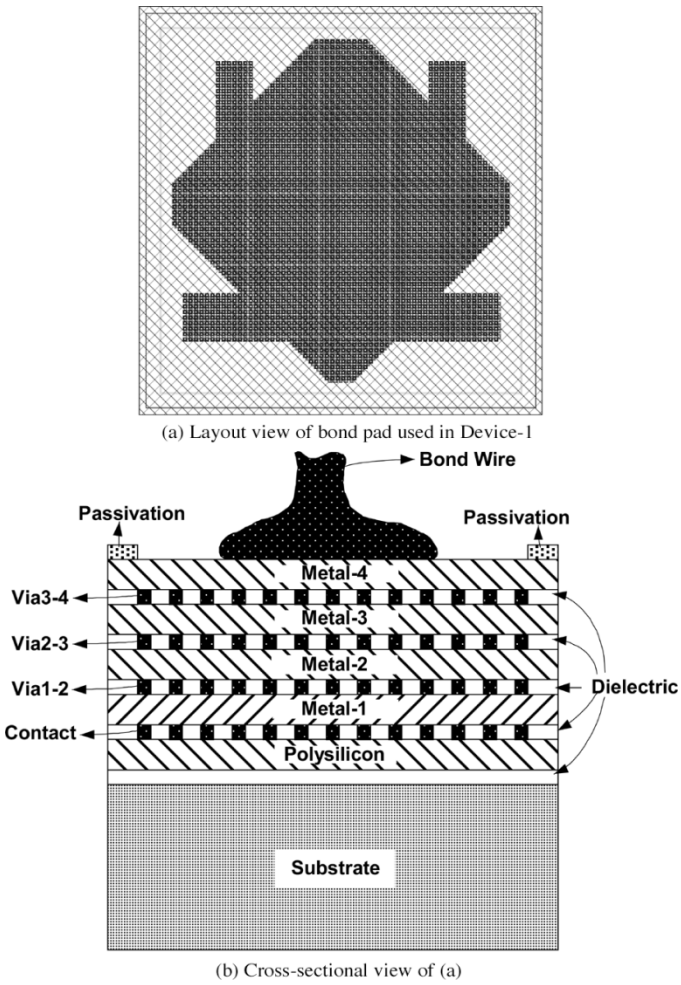


Fig. 1. NMOS transistor of Device-1 is placed beside conventional bond pads. (a) Layout top view of the conventional bond pad used in Device-1. (b) The corresponding cross-sectional view of the bond pad structure of (a), where no device is placed under the pad.

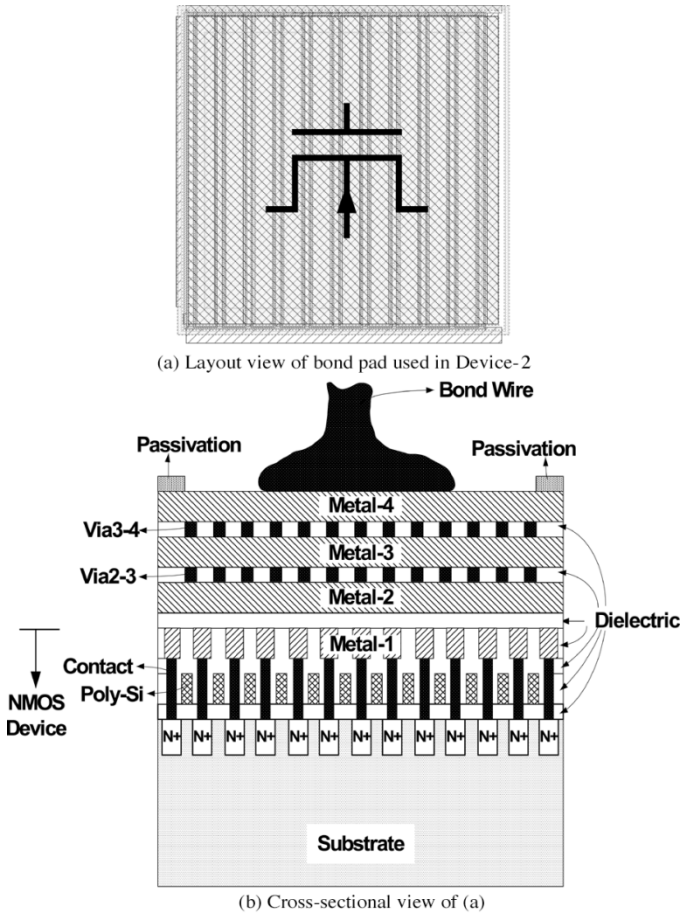


Fig. 2. NMOS transistor of Device-2 is placed under a conventional bond pad. (a) Layout pattern of the bond pad with a NMOS transistor under Metal-2 in Device-2 and (b) the corresponding cross-sectional view of the bond pad structure of (a). The NMOS device symbol in (a) indicates that there is a NMOS device beneath the Metal-2 layer of this bond pad.

beside bond pads instead of under bond pad, is used as a reference device in the test chip. The corresponding layout top view of the bond pad in this Device-1 and its cross-sectional view are shown in Fig. 1(a) and (b), respectively. The dark area in the center of Fig. 1(a) is shaped by a plurality of via plugs. From Fig. 1(b), it is clear that there is no active device under the bond pad structure.

The design of "Device-2" is constructed by four bond pads in line for the four terminals of a NMOS transistor, and the NMOS transistor is placed directly under one of these bond pads. The layout view of the bond pad with a NMOS device under it in "Device-2" is shown in Fig. 2(a). The NMOS device symbol within Fig. 2(a) indicates that there is a NMOS device beneath the Metal-2 layer of this bond pad. Its corresponding cross-sectional view is shown in Fig. 2(b). The layout drawings of the Metal-2 and Metal-3 layers are kept as flat planes (not patterned) for the bond pad with a NMOS device under it in the Device-2 test structure.

The third design of device group, which includes "Device-3," "Device-5," and "Device-7," is constructed by four bond pads in line for the four terminals of a NMOS transistor and the NMOS transistor placed directly under one of these bond pads. In the third design, it is constructed by a NMOS transistor placed under Metal-2 layer with a patterned Metal-3 layer. Metal-2 and Metal-4 layers of this designed bond pad are both in a large area of unpatterned plate. Its corresponding cross-sectional structure is shown in Fig. 3(a). The corresponding layout top views of the bond pads with a NMOS transistor under each of them in Device-3, Device-5, and Device-7 are shown in Fig. 3(b), (c), and (d), respectively. As shown in Fig. 3(b)–(d), the Metal-3 layout drawings are drawn with different patterns to investigate the relationship between different layout patterns and sustainable bonding stress [5]. The NMOS device symbols within the bond pad layout patterns indicate that there is a NMOS transistor under the patterned metal layer(s) for each of these bond pads.

The fourth design of device group, which includes "Device-4," "Device-6," and "Device-8," is also constructed by four bond pads in line for the four terminals of a NMOS transistor, and the NMOS transistor is placed directly under one of these bond pads. In the fourth design, the bond pad with a NMOS transistor placed under it is composed of a NMOS transistor beneath Metal-2 layer. The metal layers Metal-2 and Metal-3, are drawn with different layout patterns for each device. The Metal-4 layer of the designed bond pad is in a large area of an unpatterned plate. The cross-sectional view

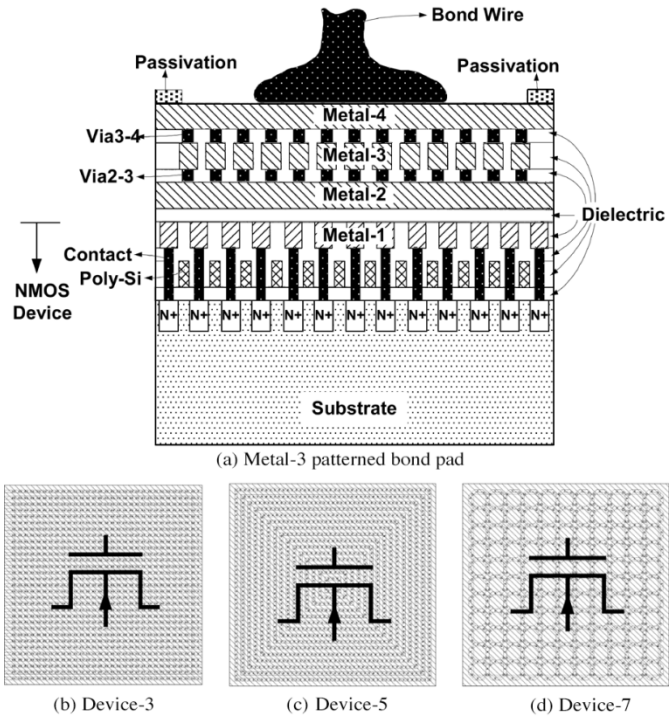


Fig. 3. Layout designs of the third design group. (a) Cross-sectional view of the bond pad structure with patterned Metal-3 and a NMOS transistor under Metal-2, and (b)–(d) show the pads realized with different patterned Metal-3 layout styles for Device-3, Device-5, and Device-7, respectively.

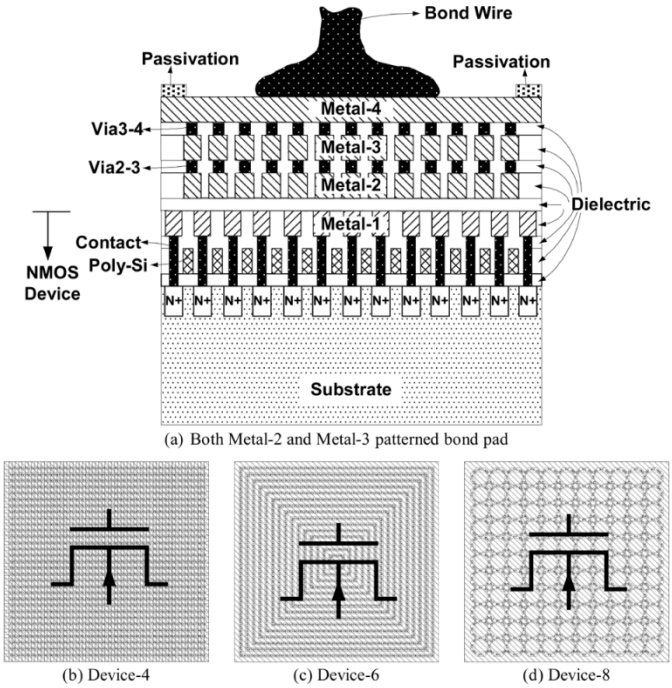


Fig. 4. Layout designs of the fourth design group. (a) Cross-sectional view of the bond pad structure with patterned Metal-2 and Metal-3 and a NMOS transistor under Metal-2 and (b)–(d) show the pads realized with different patterned Metal-2, and Metal-3 layout styles for Device-4, Device-6, and Device-8, respectively.

of the designed bond pad structure is shown in Fig. 4(a). The corresponding layout top views of the bond pads with a NMOS transistor under each of them in Device-4, Device-6, and Device-8 are shown in Fig. 4(b), (c), and (d), respectively. In Fig. 4(b)–(d), the NMOS device symbols within the bond pad layout patterns indicate that there is a NMOS transistor under the patterned metal layer(s) for each of these bond pads.

The designed patterns applied on Metal-2 and Metal-3 layers of the fourth design group are the same with the patterns applied on the Metal-3 layers of the third design group. In other words, the layout patterns of Metal-2 and Metal-3 layers in Device-4, Device-6, and Device-8 are the same with the layout patterns of the Metal-3 layer in Device-3, Device-5, and Device-7, respectively. These designed layout patterns on metal layers (Metal-2 and Metal-3) of bond pads are modified from the prior report on the low-capacitance bond pad for high-frequency circuit applications [6]. Therefore, except for saving the layout area of a silicon chip, the parasitic capacitance of the proposed bond pad design can be lowered when comparing with that of a conventional bond pad. Besides, to investigate the robustness against bonding stress applied on the bond pad with a NMOS transistor placed under it, the designed best layout pattern applied on Metal-2 and Metal-3 of the bond pad can be chosen after experimental measurements.

III. Experimental Results

The purpose of this work is to make sure whether the NMOS transistors placed under bond pads with different patterned Metal-2 and Metal-3 layout structures would be damaged by the assembly process steps, or not. The first step of the verification work is to measure the wafer-level dc characteristics of the NMOS transistors in the fabricated devices. By probing the four terminals of each NMOS transistor on the wafer, the NMOS dc characteristics before wire bonding can be measured by an HP4155 semiconductor parameter analyzer. The threshold voltage (Vt) of all the NMOS transistors on the test chips should be within the range listed on the process control management (PCM) specification released by foundry [7]. The off-state drain current (Ioff) with drain voltage (VD) biased at a VDD level of 3.3 V, and the gate leakage current (IG) with gate voltage (VG) biased at VDD level, should be both within the acceptable regions for different applications.

After the wafer-level measurements, the silicon dice of the designed test chip are then assembled by two different types of package: side-brazed dual inline (DIP) package and plastic DIP package. The side-brazed package is a kind of package with its leadframe uncovered by plastic molding compound. Thermal stress of the compound molding process and the mismatch of coefficients of thermal expansion (CTE) after compound molding could be the reasons for device performance degradation of the NMOS transistors placed under bond pads. Consequently, the purpose of performing these two types of package is to verify whether the performance of the NMOS transistors would be further degraded by the compound molding process, or not. The wire bonders for side-brazed package and plastic package are Panasonic HW22U-H and ESEC 3008, respectively. The dc I–V characteristics of the NMOS transistors after assembly for both types of packaged ICs were measured. While comparing with the wafer-level measured data, if the gate leakage current (IG), off-state drain current (Ioff), or the threshold voltage (Vt) of the NMOS transistor in the test chip are

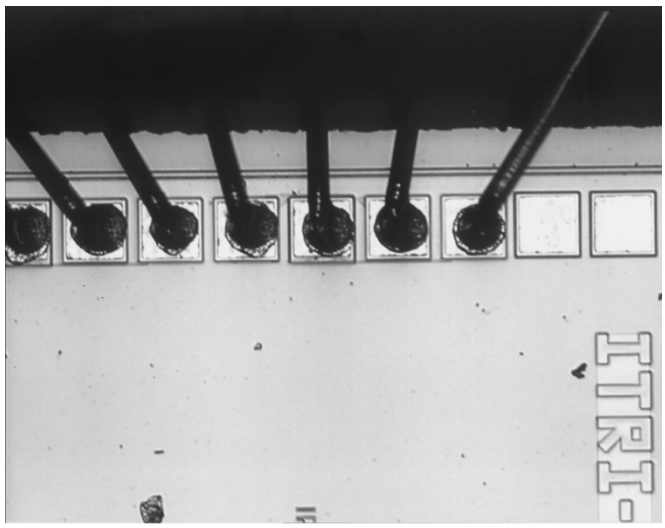
shifted obviously after assembly process steps, it can be judged that the device performance of a NMOS transistor placed under the bond pad is affected by the wire bonding process or the compound molding process.

For the samples with side-brazed DIP package, the normal bonding force of the corresponding wire bonder is 50 g, and the normal treated bonding power is 80 mW. The applied bond ball diameter under normal treated force and power is around 100 μm (or 4 mil), and the taken diameter of the golden bond wire is 25.4 μm (or 1 mil) in the experiments. To make sure whether the device performance of the NMOS transistor placed under the bond pad would be affected by the wire bonding force or not, the applied wire bonding force was controlled and split into several conditions. The split conditions of wire bonding force are 0.75×, 0.85×, 1×, 1.25×, 1.3×, 1.5×, and 1.75× of the normal wire bonding force of 50 g. In other words, the applied wire bonding forces are 37.5, 42.5, 50, 62.5, 65, 75, and 87.5 g for the split conditions. When the wire bonding force is increased, the bond ball on the bond pad would be spread into a more unexpected shape with a larger occupied area. For a wire bonding force larger than 87.5 g, the shape of bond ball would be spread into an unacceptable larger area, which could lead to the short circuit phenomenon of bond balls on adjacent bond pads. Fig. 5 shows the optical microscope (OM) photos of bond balls on bond pads applied with different wire bonding forces. As shown in Fig. 5(a), all the bond balls are shaped very well under the normal wire bonding force of 50 g. However, as shown in Fig. 5(b), the bond balls are spread into much larger areas to cause the unexpected layout shapes on the bond pads when a larger wire bonding force of 87.5 g is applied on the bond pad. Adjacent bond pads might be connected together into a "short circuit" condition by the dispersed bond balls caused by a larger bonding force. This is why the wire bonding force of 87.5 g is taken as the maximum force applied on the experimental bond pads for the results compared in Fig. 6.

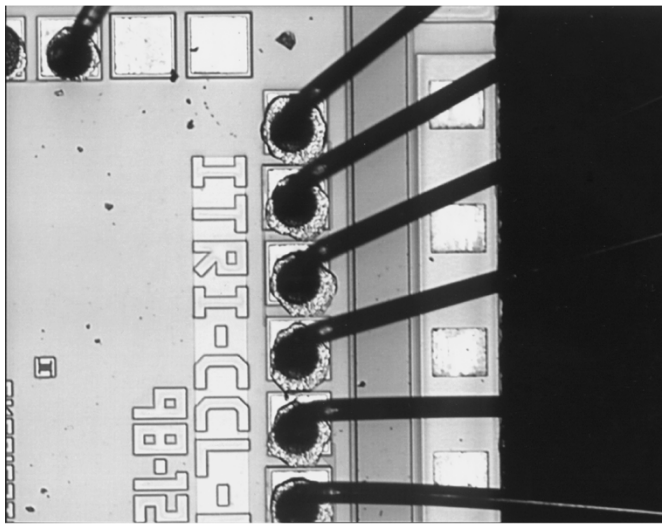
For the samples with plastic DIP package, the normal bonding force of the corresponding wire bonder is 51 g, and the normal treated bonding power is 850 mW. The applied bond ball diameter under normal treated force and power is about 80 μm (or 3.1 mil), and the taken diameter of golden bond wire is 30.5 μm (or 1.2 mil) for the experiments. The molding process temperature for these samples is 175 °C, which is a conventional temperature degree for compound molding process.

A. Measurements on Samples Without Compound Molding (Side-Brazed DIP Package)

Fig. 6 shows the dependencies of wire bonding force and the dc characteristics of NMOS transistors for different test structures in the test chip. Results in Fig. 6 are from the samples assembled by side-brazed packages, which are not treated with the compound molding process. In Fig. 6, the measured results of Device-1 design with NMOS transistor beside bond pads, are highlighted by the relatively larger size triangle symbol as a reference data. The x-axis of Fig. 6 is the normalized bonding force, which is the actually applied wire bonding forces normalized by a normal bonding force of 50 g. In other words, 1× of normalized bonding force equals to applied wire bonding force of 50 g; 0× of normalized bonding force



(a)



(b)

Fig. 5. Pictures on the bond pads with different bonding forces. (a) The bond pad is not dispersed by the normal bonding force of 50 g, and (b) the bond pad is dispersed obviously by a 1.75× of normalized bonding force, which is 87.5 g.

means device characteristics before applying any wire bonding force (the wafer-level measured results). Fig. 6(a) shows the relationship between threshold voltage (Vt) and normalized wire bonding force. The variation range of NMOS threshold voltage (Vt) is only from 0.54 to 0.58 V after wire bonding with different bonding forces. According to the foundry-released PCM specification [7], the threshold voltage of a 3.3-V NMOS device should be within the range of 0.49 to 0.69 V. From the measured results in Fig. 6(a), the variation of NMOS threshold voltage is still within the PCM specification.

Fig. 6(b) shows the relationship between off-state drain current (Ioff) and normalized wire bonding force. Although there is a larger variation on the results of applying 1.25× of normalized wire bonding force (62.5 g), the off-state drain current (Ioff) is still in the order of ∼1 nA, which is reasonable for a NMOS transistor with a large channel width of 2016 μm. Fig. 6(c) shows the relationship between the maximum transconductance (GMmax) and the normalized wire bonding force. When comparing with the Device-1 design, the measured results on GMmax of other

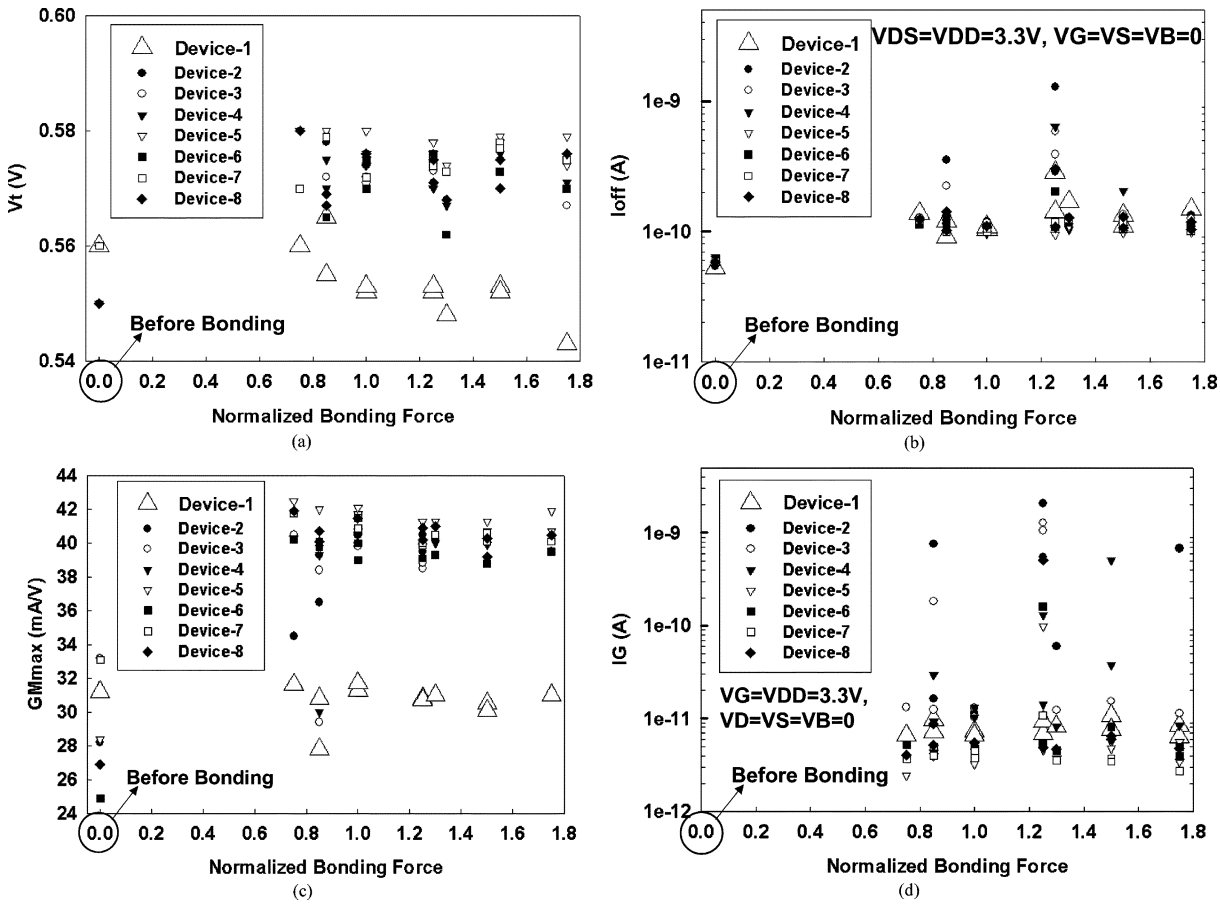


Fig. 6. Dependencies of wire bonding force on device dc characteristics of (a) threshold voltage (Vt), (b) off-state drain current (Ioff), (c) maximum gm (GMmax), and (d) gate leakage current (IG), of NMOS transistors beside bond pads (Device-1) or beneath patterned metal layers of bonding pads (Device-2 $\sim$ Device-8).

test structures in Fig. 6(c) are shifted about 50%. Fig. 6(d) shows the relationship between the gate leakage current (IG) and the normalized wire bonding force. Although the measured results in Fig. 6(d) vary from the order of $\sim$10 pA of Device-1 to the order of $\sim$1 nA of the other test devices, they are still smaller than 1 pA/μm channel width.

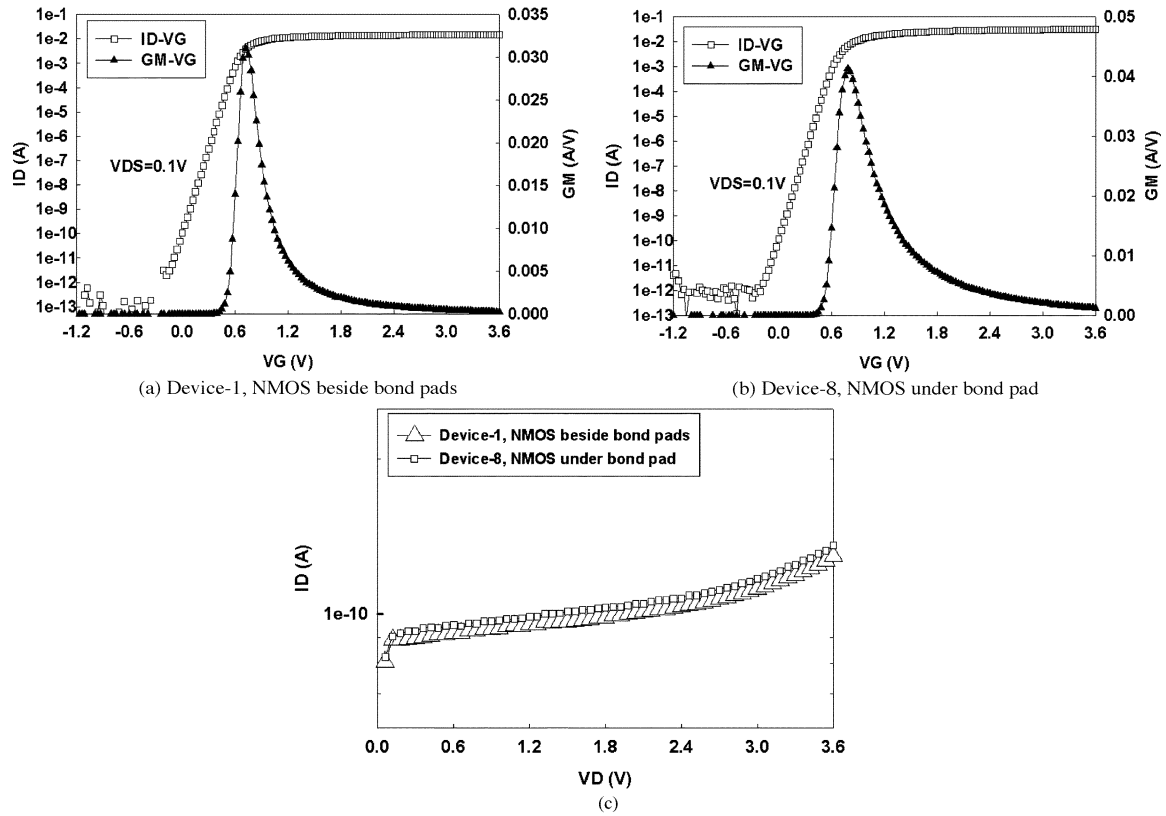
B. Measurements on Samples With Compound Molding (Plastic DIP Package)

Fig. 7 shows the measured data from the plastic DIP packaged samples. Both the dependences of the drain current (ID) and transconductance (GM) under drain-source voltage (VDS) biased at 0.1 V on the gate biased voltage (VG) after compound molding for Device-1 and Device-8 are shown in Fig. 7(a) and (b), respectively. In Fig. 7(a) and (b), the x-axis and the left-hand y-axis are the gate biased voltage (VG) and the measured drain current (ID) of the NMOS transistor, respectively. The right-hand y-axis is the transconductance (GM) of the NMOS transistor. Although the drain current (ID) under the gate voltage (VG) biased at -1.0 V is changed from several 0.1 pA of Fig. 7(a) to several pA of Fig. 7(b), the variation is within 1 fA/μm channel width for the NMOS transistor under bond pads. Besides, the related VG values at the GMmax are almost the same in Fig. 7(a) and (b). This indicates that the threshold voltage of the NMOS transistor is not shifted obviously for NMOS transistors placed beside or under the bond pads.

The I–V curve of drain current (ID) versus drain biased voltage (VD) between Device-1 and Device-8 NMOS with other terminals (gate, source, and bulk) shorted to ground after compound molding are shown in Fig. 7(c). The x-axis and y-axis of Fig. 7(c) are the drain biased voltage (VD) and the drain current (ID) of the NMOS transistor, respectively. In Fig. 7(c), the large size triangle symbol is from Device-1 with a NMOS transistor placed beside bond pads, and the rectangular symbol is from Device-8 with a NMOS transistor placed under the bond pad. So, the off-state drain current (Ioff), which is defined as the drain current under drain voltage bias of 3.3 V and all the other terminals connected to ground level of 0 V, is kept in the same order of $\sim$100 pA for NMOS transistors placed beside and under bond pads after compound molding process.

C. Measurements on Samples Before and After Thermal Tests (Plastic DIP Package)

Fig. 8 shows the measured results from the NMOS transistors of the test chip under different four conditions. These four conditions are known as wafer-level probing, after compound molding of plastic DIP package, after thermal shock test, and after temperature cycling test. As shown in Fig. 8, the wafer-level probing data were identified by the large triangle symbol

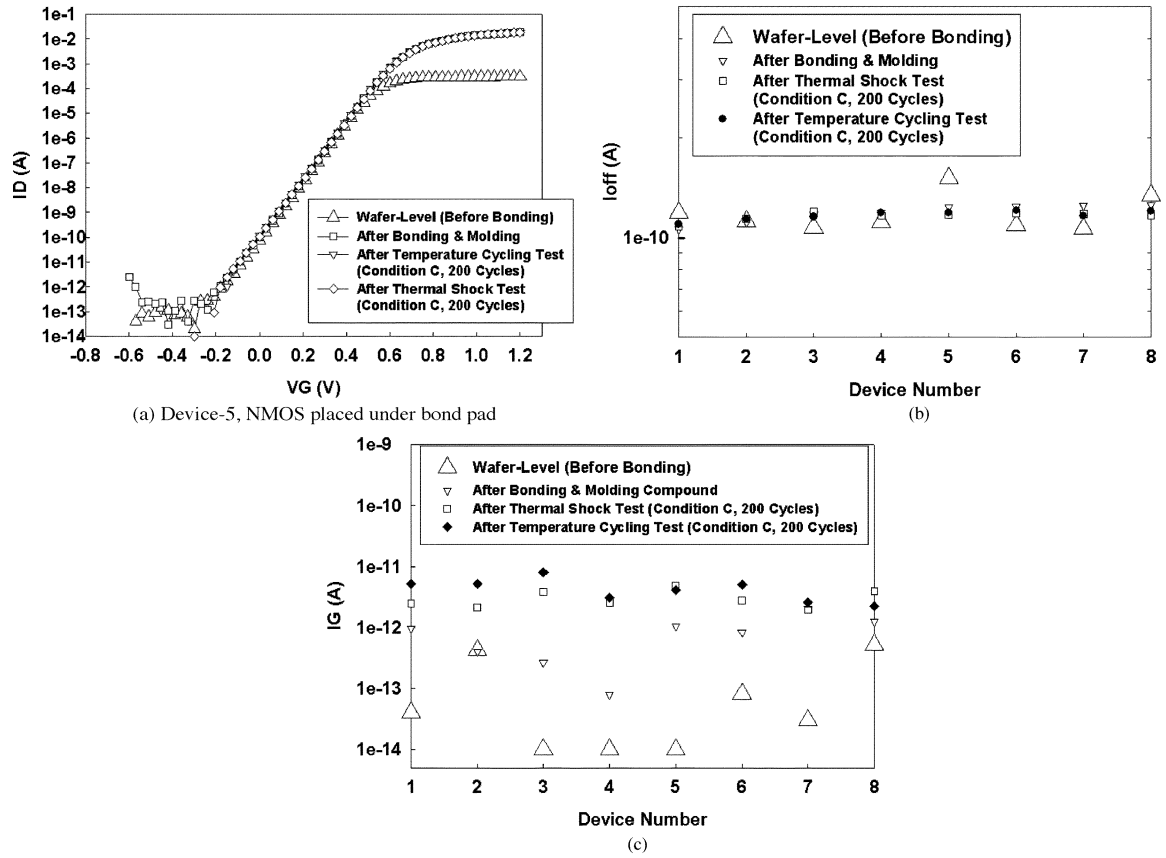


(a) Device-1, NMOS beside bond pads

(b) Device-8, NMOS under bond pad

(c)

Fig. 7. Comparison of device dc characteristics after compound molding: (a) ID-VG curve of Device-1, (b) ID-VG curve of Device-8, and (c) ID-VD curves of Device-1 and Device-8.



(a) Device-5, NMOS placed under bond pad

(b)

(c)

Fig. 8. DC characteristics of test devices after various assembly process steps: (a) drain current (ID) versus gate biased voltage (VG) of NMOS device placed under bond pad, (b) the off-state drain current (Ioff) versus different device numbers, and (c) the gate leakage current (IG) versus different device numbers.

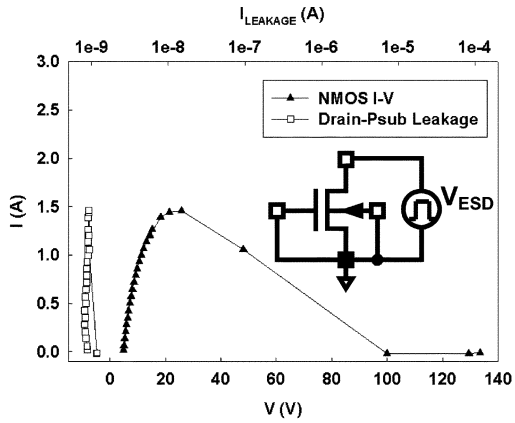
as a reference for comparing with the other three conditions. After assembly process steps applied on the test samples, both thermal shock and temperature cycling tests were then applied onto the samples. Both of these thermal tests were applied with 200 cycles for each test in condition C ($-65\,^{\circ}\mathrm{C} \sim 150\,^{\circ}\mathrm{C}$) of U.S. Military Standard MIL-STD-883E [8], [9].

Fig. 8(a) shows the relationship between the drain current (ID) and the gate biased voltage (VG) in the subthreshold region with 0.1-V drain biased voltage for Device-5 with a NMOS transistor placed under the bond pad. There are four curves in Fig. 8(a), which were measured from the samples at the mentioned four conditions. These four curves are almost overlapped into one curve in the subthreshold region of the NMOS transistors. This indicates that the switching speeds of the NMOS transistors were neither degraded by the assembly process steps, nor degraded by the thermal tests applied on the samples.

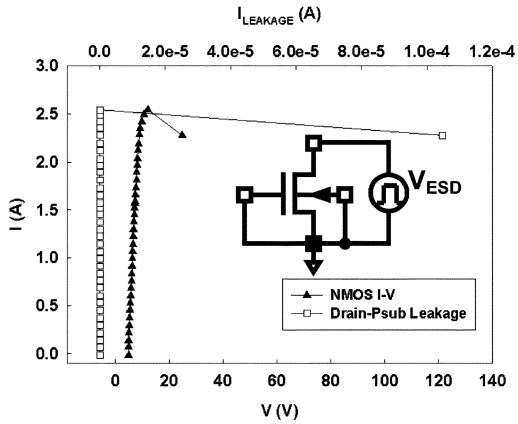
Fig. 8(b) shows the relationship between the off-state drain current (Ioff) and different devices in the test chip. The measured results indicate that there is no significant difference on Ioff of different devices under four split conditions. In other words, the off-state drain currents (Ioff) of the NMOS transistors on the samples of designed test chip were neither affected by the assembly process steps nor affected by the applied thermal tests. Fig. 8(c) shows the relationship between the gate leakage current (IG) and different devices in the test chip. From Fig. 8(c), the gate leakage currents (IG) after the assembly process steps were increased by $1 \sim 2$ orders when comparing with the wafer-level measurement data. The gate leakage currents (IG) after the thermal tests were increased by $2 \sim 3$ orders when comparing with the wafer-level measurement data. Although the gate leakage currents are increased, they are still smaller than the order of 10 pA for a NMOS transistor with its channel width of 2016 μm.

D. ESD Robustness

Fig. 9 shows the relationship between the I–V curves of Device-1 and Device-2, measured by transmission line pulse (TLP) [10], and device leakage currents after TLP stress. The TLP system has been a general tool to estimate the ESD robustness of semiconductor devices [11]. The TLP stress applied on the device was done after thermal shock test. The y-axis and bottom x-axis of Fig. 9(a) shows the TLP measured NMOS I–V curve of Device-1 with a NMOS transistor placed beside bond pads. The y-axis and upper x-axis of Fig. 9(a) shows the Device-1 drain leakage current after TLP stress with the NMOS gate, source, and bulk all connected to ground. With the same stress method and bias condition, the I–V curve and leakage current of NMOS transistor in Device-2 are shown in Fig. 9(b). With comparison between Fig. 9(a) and (b), the NMOS second breakdown current (It2) of Device-2 is obviously larger than that of Device-1, because the metal line width for NMOS drain site connection is only 5 μm in the layout drawing of Device-1. With such a narrow line width of 5 μm, the connection metal bus cannot sustain a large amplitude of current flow, such as ESD current, and it was broken by the current under TLP stress. This inference can be proved by the I–V curve of Device-1 in Fig. 9(a). As shown in Fig. 9(a), the device current is suddenly dropped from 1.46 A at 25.9 A to 1.06 A at 48.1 V, and then



(a) Device-1 (NMOS placed beside bond pads) with drain metal width of 5μm



(b) Device-2 (NMOS placed under bond pad) with drain metal width of 20.7μm

Fig. 9. TLP-measured I–V curves of (a) Device-1 with its NMOS placed beside bond pads and (b) Device-2 with its NMOS placed under a bond pad. The TLP pulsing tests were done after thermal shock test with the gate, source, and bulk of the NMOS transistor grounded.

to 0 A at 100 V, which indicates that the interconnection with a narrow line width has already been broken to open by the large TLP current of 1.46 A. For Device-2, the metal line width for NMOS drain site interconnection metal bus is 20.7 μm in the layout drawing, which can sustain larger current flow running through it.

The I–V curves of Device-5 before and after TLP measurement, which there is a NMOS placed under the bond pad, are shown in Fig. 10(a) and (b), respectively. The curves were measured by Tek370 Curve Tracer before and after TLP stress with the gate, source, and bulk of NMOS connected to ground. The TLP pulses applied on the device were done after thermal shock test. The NMOS I–V curve was obviously degraded after TLP stress, when comparing between Fig. 10(a) and (b). This indicates that the NMOS transistor was damaged by the TLP stressing.

Fig. 11 shows the ESD test results. Fig. 11(a) is about the dependence of It2 on different devices after thermal tests, and Fig. 11(b) is about the human body model (HBM) ESD test results for the devices under test. The x-axes and y-axes of Fig. 11 are the device number and the ESD levels for each device, respectively. For the TLP test, there are two samples under test for each thermal test condition, so there are four curves in Fig. 11(a). The It2 values of Device-1 with a NMOS beside bond pads are smaller than those of others. The reason is that the line

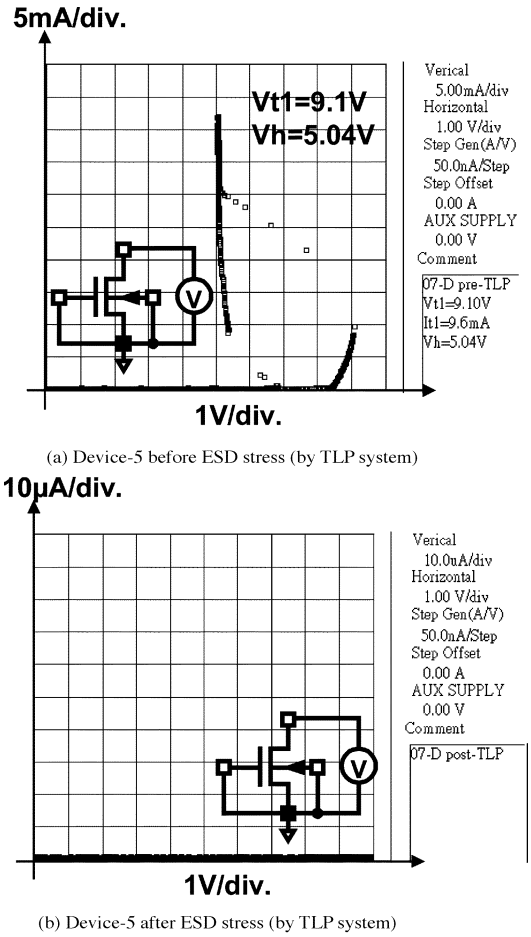


Fig. 10. Measured I–V curves of Device-5 with a NMOS transistor placed under the bond pad (a) before and (b) after TLP stress. The TLP pulses applied on the device were done after thermal shock test.

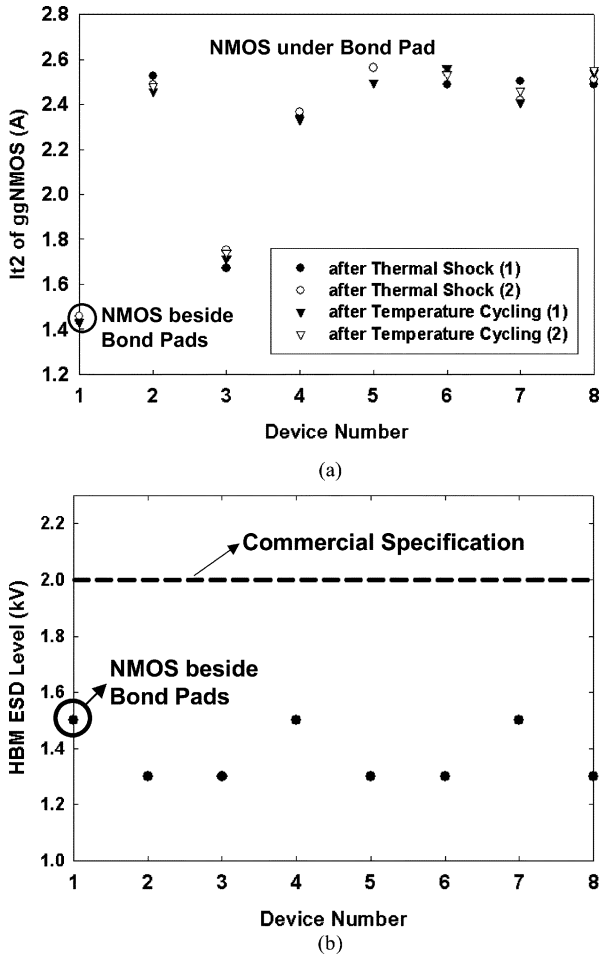


Fig. 11. ESD test results. (a) The comparison on It2 values among the test devices with different bond pad structures after thermal tests. The It2 values of Device-1 (NMOS beside bond pads) are smaller than those of the others, due to breaking of narrow metal line connected from the pad to the drain of NMOS beside the pad. (b) The HBM ESD test results for each of the devices. The HBM ESD tests were performed after thermal reliability tests for the devices under test.

width of the interconnection metal bus is too narrow to sustain the large current pulse. It indicates that if the NMOS transistor is placed directly under the bond pad, the NMOS drain connection is easily to be drawn with wider line width to the bond pad. On the other hand, if the NMOS is placed beside bond pads, the NMOS drain connection should be carefully drawn as wide as possible. This results in an increase on the I/O cell layout or pitch. So, the active devices (I/O transistor or ESD protection device) placed under the bond pad is helpful to ESD robustness and area efficiency.

The HBM ESD test results for devices in Fig. 11(b) are performed on the plastic DIP samples after their thermal tests by using a commercial ESD simulator: ZapMaster. According to Fig. 11(a) and (b), it is obvious that the HBM ESD test results do not show a close relationship with the TLP test results. This might be caused by the different waveforms generated from the TLP system and the ZapMaster, respectively.

IV. Discussion

When comparing the experimental results shown in Figs. 6–8, there is no obvious difference between the dc characteristics of the NMOS transistors placed under bond pads with their Metal-2 and Metal-3 layers drawn with different layout patterns. This indicates that the bond pads with various low-capacitance layout pattern designs have the same robustness against both the mechanical and thermal stresses, which were induced during the assembly process steps or thermal reliability tests. Therefore, the factor of various layout pattern designs on Metal-2 and Metal-3 layers can be ignored while discussing the degradation of device performance.

As shown in Fig. 6, there is no dependency between the wire bonding force and the variations of NMOS dc characteristics. This indicates that the wire bonding force applied on the bond pad is not the factor affecting the device performance degradation of the NMOS transistors placed under bond pads.

According to the measurement data shown in Fig. 6–8, the most obvious difference of the device dc characteristics of NMOS transistors placed beside and under bond pads is the device gate leakage current. According to Fig. 8(c), it can be concluded that the assembly process steps are the reasons of device performance degradation of the NMOS transistors placed under bond pads. Furthermore, the device performances of the NMOS transistors placed under bond pads were further degraded by the thermal reliability tests, which include thermal shock and temperature cycling tests.

V. Conclusion

The active devices placed under bond pads have been verified in a 0.35-μm 1P4M 3.3-V CMOS process. DC characteristics of test chips were measured for four major steps of assembly, which are wafer-level probing, after wire bonding (side-brazed DIP package), after compound molding (plastic DIP package), and after life time thermal tests (thermal shock and temperature cycling tests). By a series of experimental investigations (changing wire bonding force applied on bond pads, additional compound molding process, and thermal reliability tests) and dc characteristics measurements, the device performances of NMOS transistors placed under bond pads have been proven to have only little variations. Such variations are still acceptable for general CMOS IC products to save chip layout area. Therefore, the protection devices or I/O transistors can be placed under bond pads for different applications. The parasitic capacitance of the bond pad can be also reduced by the patterned metal layers and the N+ diffusion region beneath the bond pad. Without any extra process steps, the devices under the bond pads make the chip layout placement more flexible and with the advantage of saving the layout area. When the CMOS process is migrating to the 0.18-μm range with typical eight metal layers, the active devices placed under the bond pad will be more safe against bonding stress on the top metal pad. A new methodology to efficiently place the active devices under the bond pad in the I/O cells, and the analysis of the device ESD robustness will be the future work of this study.

References

[1] W. R. Anderson, W. M. Gonzalez, S. S. Knecht, and W. Fowler, "ESD protection under wire bonding pads," in *Proc. EOS/ESD Symp.*, 1999, pp. 88–94.

[2] G. Heinen, R. J. Stierman, D. Edwards, and L. Nye, "Wire bonds over active circuits," in *Proc. Electronic Components and Technology Conf.*, 1994, pp. 922–928.

[3] K.-Y. Chou, M.-J. Chen, C.-C. Lin, Y.-S. Su, C.-S. Hou, and T.-C. Ong, "Die cracking evaluation and improvement in ULSI plastic package," in *Proc. IEEE Int. Conf. Microelectronic Test Structures*, vol. 14, 2001, pp. 239–244.

[4] K.-Y. Chou and M.-J. Chen, "ESD protection under grounded-up bond pads in 0.13 μm eight-level copper metal, fluorinated silicate glass low-k international dielectric CMOS process technology," *IEEE Electron Device Lett.*, vol. 22, pp. 342–344, July 2001.

[5] M.-D. Ker and J.-J. Peng, "Fully process-compatible layout design on bond pad to improve wire bond reliability in CMOS ICs," *IEEE Trans. Comp. Packag. Technol.*, vol. 25, pp. 309–316, June 2002.

[6] M.-D. Ker, H.-C. Jiang, and C.-Y. Chang, "Design on the low-capacitance bond pad for high-frequency I/O circuits in CMOS technology," *IEEE Trans. Electron Devices*, vol. 48, pp. 2953–2956, Dec. 2001.

[7] TSMC 0.35 μm logic silicide SPQM 3.3 V process PCM specification, Tech. Rep., TSMC, Mar. 1998.

[8] *Temperature cycling*, MIL-STD-883E Method 1010.7, 1987.

[9] *Thermal shock*, MIL-STD-883E Method 1011.9, 1990.

[10] T. J. Maloney and N. Khurana, "Transmission line pulsing techniques for circuit modeling of ESD phenomena," in *Proc. EOS/ESD Symp.*, 1985, pp. 49–54.

[11] T.-Y. Chen and M.-D. Ker, "Investigation of the gate-driven effect and substrate-triggered effect on ESD robustness of CMOS devices," *IEEE Trans. Device Mater. Rel.*, vol. 1, no. 4, pp. 190–203, Dec. 2001.

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