Mobility Enhancement of MOSFETs on p-Silicon (111) With *In situ* HF-Vapor Pre-Gate Oxide Cleaning

Tien Sheng Chao, *Senior Member*, Yu Hsin Lin, and Wen Luh Yang

***Abstract*—In this paper, we grow and characterize in detail native-oxide-free ultrathin gate oxide on silicon (111) by an advance clustered vertical furnace with in situ HF-vapor stripping of the native oxide. Excellent results are demonstrated. Gate oxide integrity is significantly improved in terms of time-to-breakdown, drain current, and transconductance. *In-situ* HF-vapor cleaning by a clustered vertical furnace appears to be very promising to grow high-quality native-oxide-free gate oxide on silicon (111).**

***Index Terms*—*In situ* HF, MOSFETs, native oxide, silicon (111), vapor.**

I. INTRODUCTION

RECENTLY, silicon (111) has been attracting much attention since higher channel mobility of pMOSFETs can be achieved than that fabricated on conventional (100) substrates [1]. Similar result was also reported for the pMOSFETs with high-κ dielectrics, HfO_2 [2]. On the other hand, AlGaN–GaN HEMTs has been reported grown on Si (111) [3]. Using a buffered layer, silicon (111) can be used as the substrate for GaN growth for radio frequency (RF) and power applications. This is very attractive because of silicon's low cost, large size substrate available, good thermal conductivity. This success makes the integration of optical devices, high power and/or high-speed devices on silicon with advanced ULSI silicon technology possible. The requirements for gate oxide reliabilities become more and more stringent as the device size scales down to the deep-submicrometer era [4]. This is because the gate oxide thickness is fast approaching the physical limit imposed by the high leakage current due to direct tunneling. In general, the ultimate oxide thickness is believed to be around 1.5 nm. Beyond that, silicon dioxide would have to be replaced by high-κ materials [5], [6]. However, we face the serious mobility degradation when depositing high-κ directly on silicon. This degradation can be released if a buffered thin oxide exists before high-κ deposition. But this buffered layer is not easy to scale down, consequently equvilent oxide thickness (EOT) is too thick to use for high-speed applications. Under this condition, the removal of the native oxide prior to gate oxidation becomes very critical for oxide thickness less than 2 nm. This is because the native oxide is in general poor in quality with low density [7]. This native oxide on the silicon surface is known to grow very quickly in the open air. Thickness can reach 0.5–1.0 nm within 10 min in the laboratory ambient. That makes the growth of ultrathin oxide difficult. Huge ratio of native oxide in the final gate oxide cannot be tolerated in the preparation for ultrathin oxide. In addition, the effective dielectric constant of the stacked high-k structure would be significantly reduced as the native oxide thickness increases. Recently, the integrated circuit (IC) industries have begun to realize the advantage of dry cleaning technology in the cluster system. Among these, HF-vapor, instead of wet HF-dip, is attractive because of fluorine-terminated surface [8]. In this paper, we grow and characterize in detail native-oxide-free ultrathin gate oxide on silicon (111) by an advance clustered vertical furnace with *in situ* HF-vapor stripping of the native oxide. We found that the mobility of MOSFETs on silicon (111) can be significantly increased.

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II. EXPERIMENT

The clustered vertical system consists of three modules, i.e., HF-vapor cleaning, oxidation, and *in situ* n^+-doped poly-Si deposition. Wafers, 6-in p-type (111) of resistivity 3–6 Ω-cm, were processed through these three modules in sequence without exposure to the ambient, so as to obtain native-oxide-free poly-Si–SiO_2–Si MOS capacitors. To achieve this, the cabinet is filled with high purity nitrogen (with residual oxygen content of less than 4 ppm), to suppress any native oxide growth after the HF-vapor stripping of the original native oxide. Four kinds of samples, with oxide thickness of 3.5 nm (O_2) and 3.2 nm (N_2O), were obtained as follows: Wafers were split to receive either a conventional wet HF-dip or the *in situ* dry HF-vapor (HFV) cleaning, and then wafers were further split to receive either a conventional O_2 or N_2O oxidation. The oxidation temperature was at 800 °C. The oxide thickness was 3.5 nm for O_2 samples and 3.2 nm for N_2O, respectively. Uniformity of the gate oxide was found to be within ± 1 Å across the 6-in wafer. To investigate oxygen residual on the silicon surface, another testing experiment was executed. After loading into the cluster system, wafers were split to receive the HF-vapor treatment (HFV) or without the HFV (HF-Dip). Then wafers were directly deposited a poly-Si film in the same cluster system.

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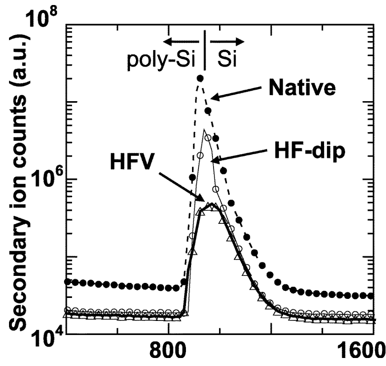

Fig. 1. SIMS profiles of oxygen. Native: without any HF treatment after RCA cleaning processes. HF-dip: with HF-H_2O (1:100) dip after RCA cleaning processes. HF-V: with HF-dip and clustered HF-vapor treatment after RCA cleaning processes. All samples skip the oxidation step in the cluster system and deposit poly-Si.

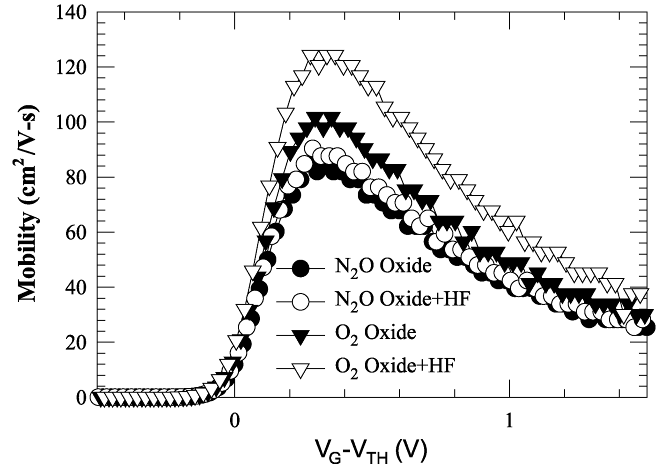

Fig. 3. Field-effect mobility deduced from transconductance and T_{ox} for four split conditions at the linear regime at $V_{DS} = 0.1$ V.

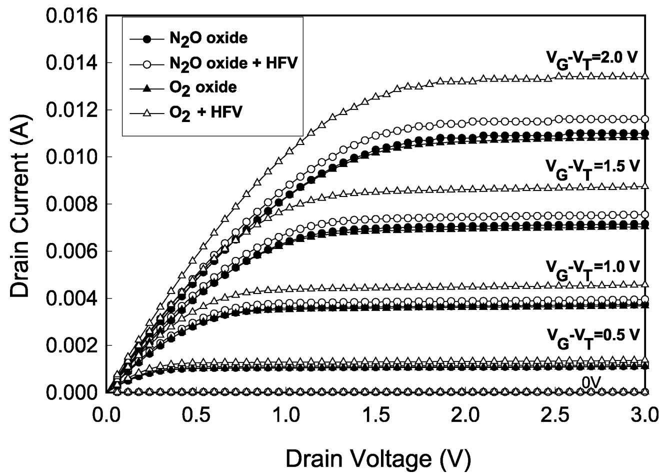

Fig. 2. I_D versus V_D curves under different $V_G - V_T = 0.5$, 1.0, 1.5, and 2.0 V. The gate oxide was split four conditions, i.e., O_2 versus N_2O oxide and with/without HF-vapor (HFV) treatment. The I_D is normalized for all condition by taking Cox into consideration.

III. Result and Discussion

Fig. 1 shows the resultant SIMS-profile at the interface of poly-Si/Si samples which skip oxidation step in cluster system. The sample without any HF-treatment after conventional RCA cleaning was also shown, which shows the largest oxygen counts at the interface. It is seen that the oxygen is significantly reduced (about one order of magnitude) using the *in situ* HFV treatment compared with the conventional HF-dip. This implies the native oxide can be precisely controlled. Fig. 2 shows the drain current versus drain voltage at $V_G - V_{TH} = 0.5$, 1.0, 1.5, and 2.0 V for $W/L = 100/1\ \mu m$. To eliminate the slight difference of oxide thickness among devices, the drain current is normalized for all conditions by taking C_{ox} of O_2 oxide ($T_{ox} = 3.5$ nm) into consideration. It can be seen that N_2O oxide (solid circles) with conventional HF-dip treatment is slightly larger than that of O_2 counterpart (solid triangle) at high field. This crossover phenomenon is similar to previous report on silicon (100) [9]. For both O_2 and N_2O devices with HFV-treatment, the drain current is increased. Increase of drain current for O_2 oxide (22% increase at $V_D = 3.0$ V, and $V_G = 2$ V) is higher than that of N_2O counterpart (7% increase). No crossover phenomenon was found again for samples with HFV treatments. Since it is believed that degradation of current in the high field is due to surface roughness, this implies the surface roughness can be improved by using HFV treatment, this is consistent with our previous report [10] and in [7]. The field-effect mobility μ_{FE} deduced from transconductance and C_{OX} at linear regime (V_{DS}at0.1 V) was plotted in Fig. 3. Both O_2 and N_2O devices exhibit increased field-effect mobility with HFV-treatment. The mobility of MOSFETs with N_2O-oxide increases 4% with HFV-treatment compared to the conventional HF-dip one; while 30% increase was found for O_2-oxide with HFV-treatment. The significant increase of mobility makes the crossover phenomenon disappear for N_2O oxide versus O_2 oxide. However, the maximum μ_{FE} of Si-(111) with HFV-treatment is still lower than that of Si-(100) [11]. Since the interfacial trap density exhibits strong relation with the device's mobility, as we have reported in [10] and also in Chin *et al.* [7], the interface trap density can be reduced by HF-vapor treatment on silicon (100). From the result of Fig. 3, we found that devices with HFV-treatment show significant improvement on mobility for Si-(111), which is similar to the report on Si-(100) in [10]. The charge pumping current (I_{CP}) for all samples were measured. The maximum Icp of O_2 oxide was 110 nA, which decreases to 70 nA with HFV-treatment; while Icp of N_2O oxide was 120 nA, which decreases to 90 nA with HFV-treatment. Based on these results, it can be clearly seen that the interface has been significantly improved with HFV-treatment. Time-to-breakdown test were executed on MOS capacitors at constant $E_{ox} = 10$ MV/cm, and result is shown in Fig. 4. It is clear that samples with HFV-treatment show an improved time-to-breakdown than counterparts for both O_2 and N_2O devices.

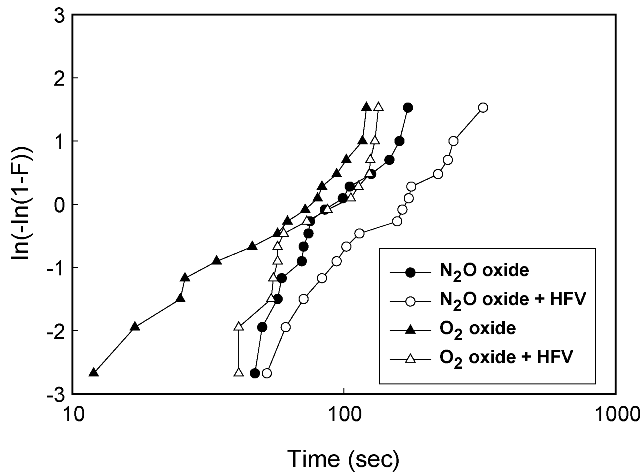

Fig. 4. The time-to-breakdown for samples with O_2 versus N_2O oxide and with/without HFV treatment under constant $E_{ox} = 10\ MV/cm$. The area of capacitor is $300 \times 300\ \mu m^2$.

IV. Conclusion

In summary, significant mobility enhancement was found for MOSFETs grown in p-silicon (111). Using an *in situ* HF-vapor stripping of the native oxide prior to gate oxidation has been demonstrated to improve the gate oxide integrity in terms of driving current, mobility, and time-to-breakdown, especially for the MOSFETs with conventional ultrathin O_2 gate oxide.

References

[1] H. S. Momose, T. Ohguro, S. Makamura, Y. Toyoshima, H. Ishiuchi, and H. Iwai, "Ultrathin gate oxide CMOS on (111) surface-orientated Si substrate," *IEEE Trans. Electron Devices*, vol. 49, pp. 1597–1605, Sept. 2002.

[2] K. Onishi, C. S. Kang, R. Choi, H. J. Cho, Y. H. Kim, S. Krishnan, M. Shahariar, and J. C. Lee, "Performance of polysilicon gate HfO2 MOSFET's on (100) and (111) silicon substrate," *IEEE Electron Device Lett.*, vol. 24, pp. 254–256, Apr. 2003.

[3] P. Javorka, A. Alam, M. Wolter, A. Fox, M. Marso, M. Heuken, H. Luth, and P. Kordos, "AlGaN/GaN HEMT's on (111) silicon substrates," *IEEE Electron Device Lett.*, vol. 23, pp. 4–6, Jan. 2002.

[4] Y. Taur, "CMOS design near the limit of scaling," *IBM J. Res. Develop.*, vol. 46, pp. 213–221, 2002.

[5] H. Y. Yu, J. F. Kang, C. Ren, J. D. Chen, Y. T. Hou, C. Shen, M. F. Li, D. S. H. Chan, K. L. Bera, C. H. Tung, and D. L. Kwong, "Robust high-quality HfN-HfO2 gate stack for advanced MOS device applications," *IEEE Electron Device Lett.*, vol. 25, pp. 70–72, Jan. 2004.

[6] R. Nieh, S. Krishnan, H. J. Cho, C. S. Kang, S. Gopalan, K. Onishi, R. Choi, and J. C. Lee, "Comparison between ultrathin ZrO_2 and ZrOxNy gate dielectric in TaN or poly-gated NMOSCAP and NMOSFET devices," in *VLSI Technol. 2002—Dig. Tech. Papers*, pp. 186–187.

[7] A. Chin, B. C. Lin, W. J. Chen, Y. B. Lin, and C. Thai, "The effect of native oxide of thin gate oxide integrity," *IEEE Electron Device Lett.*, vol. 19, pp. 426–428, Nov. 1998.

[8] C. Y. Chang and S. M. Sze, Eds., *ULSI Technology*. New York: McGraw-Hill, 1996, ch. 2.

[9] H. Hwang, W. Ting, D. L. Kwong, and J. C. Lee, "Improved reliability characteristics of submicrometer nMOSFET's with oxynitride gate dielectric prepared by rapid thermal oxidation in N_2O," *IEEE Electron Device Lett.*, vol. 12, pp. 495–497, 1991.

[10] C. L. Chen, T. S. Chao, C. S. Lai, and T. Y. Huang, "High-quality native-oxide-free ultrathin oxide grown by in situ vapor treatment," *Electron. Lett.*, vol. 36, pp. 981–982, 2000.

[11] M. Yang, E. P. Gusev, M. Ieong, O. Gluschenkov, D. C. Boyd, K. K. Chan, P. M. Kozlowski, C. P. D'Emic, R. M. Sicina, P. C. Jamison, and A. I. Chou, "Performance dependence of CMOS on silicon substrate orientation for ultrathin oxynitride and HfO_2 gate dielectrics," *IEEE Electron Device Lett.*, vol. 24, pp. 339–341, May 2003.