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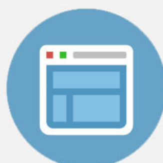

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Soft breakdown enhanced hysteresis effects in ultrathin oxide silicon-on-insulator metal-oxide-semiconductor field effect transistors

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The impact of oxide soft breakdown location on threshold voltage hysteresis in partially depleted silicon-on-insulator metal-oxide-semiconductor field effect transistors with an ultrathin oxide (1.6 nm) is investigated. Two breakdown enhanced hysteresis modes are identified. In a drain-edge breakdown device, excess holes result from band-to-band tunneling flow to the floating body, thus causing threshold voltage variation in drain bias switching. In contrast, in a channel breakdown device, enhanced threshold hysteresis is observed during gate bias switching because of increased valence band electron tunneling. Our findings reveal that soft breakdown enhanced hysteresis effect can be a serious reliability issue in silicon-on-insulator devices with floating body configuration. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1773384]

I. INTRODUCTION

Silicon-on-insulator (SOI) technology has emerged as a promising technology for system-on-a-chip applications, which require high-performance complementary metal-oxide-semiconductor field effect transistors (MOSFET), low power, embedded memory, and bipolar devices. The primary feature of a MOSFET with SOI configuration is that the local substrate of the device is floating electrically, and thus the substrate-source bias (V_{BS}) is not fixed. As V_{BS} changes, the device threshold voltage (V_t) will change due to the body effect. This "instability" in V_t resulting from floating body configuration becomes one of the most challenging tasks in bringing SOI devices into mainstream applications.[1–4] One manifestation of the V_t variation is the hysteresis effect. The V_t hysteresis as a result of various floating body charging/discharging mechanisms has been widely investigated.[2–4] In this work, the influence of gate oxide breakdown position on hysteresis effects in ultrathin oxide partially-depleted (PD) SOI MOSFETs will be explored.

Several causes of V_t hysteresis in PD SOI MOSFETs have been proposed.[5–8] Boudou *et al.*[5] reported that V_t hysteresis could be caused by positive feedback of impact ionization due to long time constants associated with body potential charging. Chen *et al.*[6] showed that at high drain biases the floating body effect can lead to hysteresis in the subthreshold $I_{ds}-V_{gs}$ characteristics even when the gate is biased well below its threshold voltage. Fung *et al.*[7] found that in ultrathin gate oxide devices the gate-to-body tunneling current modulates the body voltage and induces a hysteresis effect. All the above works investigate the hysteresis phenomenon in PD SOI MOSFETs without considering gate oxide soft breakdown (SBD). Recent studies[9–13] showed that in bulk CMOS the impact of gate oxide SBD is only manifested in a noticeable increase in gate leakage current without degrading other device characteristics in operation. Crupi *et al.*[14] showed that at high gate voltages the substrate current steeply increases after SBD due to localized effective thinning of gate oxide. Chan *et al.*[15] presented that in thinner oxides the post-SBD gate induced drain leakage (GIDL) current increases significantly because of the enhancement of band-to-band tunneling. Although the dependence of these excess substrate currents on the location of a SBD spot was widely explored, the influence of SBD location on V_t hysteresis in SOI devices has been rarely investigated.

II. DEVICE STRUCTURE AND CHARACTERIZATION

The devices in this work were made with a 0.13 μm standard CMOS process on *p*-type PD SOI substrate. The gate oxide was grown with rapid plasma nitridation (RPN) process. The gate length is 0.13 μm, the gate width is 10 μm and the oxide thickness is 1.6 nm. The test devices have an H-gate structure with an additional contact to facilitate the measurement of the body current and voltage. In this paper, all devices were stressed at high constant gate voltage with the source and drain grounded. The stress was stopped immediately after the first breakdown was detected. The current compliance for breakdown detection was chosen to be 10 μA. After breakdown, the device on-state characteristics were checked and no difference was observed.

TABLE I. The ratio of $I_d/(I_s+I_d)$ and $I_b/(I_s+I_d)$ before and after soft breakdown in four SOI MOSFETs. The measurement is in the accumulation region and $V_g=|1.5\text{ V}|$, $V_d=V_s=0$ V.

	*n*MOSFET		*p*MOSFET	
Acc. region	Device A (*c*-SBD)	Device B (*e*-SBD)	Device C (*c*-SBD)	Device D (*e*-SBD)
I_d/I_s+I_d before SBD	0.5078	0.5297	0.5174	0.5251
I_d/I_s+I_d after SBD	0.4482	0.9957	0.1368	0.9387
I_b/I_s+I_d before SBD	0.0287	0.0178	0.3202	0.1163
I_b/I_s+I_d after SBD	0.1426	0.0001	10.8680	0.0102

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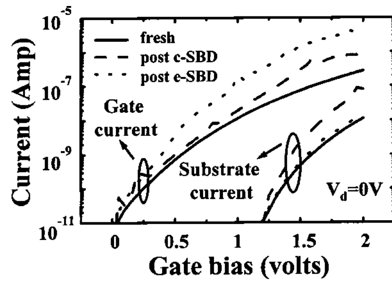

FIG. 1. Gate current and substrate current versus gate bias in *n*MOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

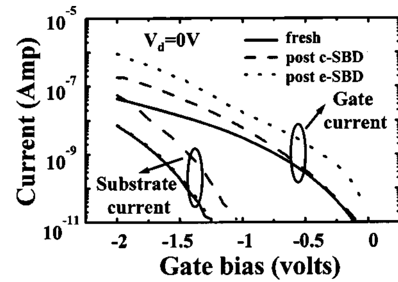

FIG. 3. Gate current and substrate current versus gate bias in *p*MOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

The breakdown position was examined by using the method proposed by Degraeve *et al.*[16] Table I shows the ratio of I_d to (I_s+I_d) before and after SBD in four SOI devices. The measurement is in accumulation region and $|V_g|=1.5$ V and $V_d=V_s=0$ V. A significant increase of $I_d/(I_s+I_d)$ in device B and device D indicates that breakdown is located at the drain edge, while in device A and device C the moderate change in $I_d/(I_s+I_d)$ implies that the SBD position is in the channel. Aside from $I_d/(I_s+I_d)$, $I_b/(I_s+I_d)$ was measured (also shown in Table I). In the channel SBD (*c*-SBD) devices, the valence band tunneling leakage in the channel region (I_b) was enhanced, resulting in a larger $I_b/(I_s+I_d)$. In the case of edge SBD (*e*-SBD), the breakdown was above the drain edge. As a result, the tunneling leakage current in the channel region remains almost the same as in pre-SBD, and the increased edge leakage current makes I_s+I_d larger and thus a smaller $I_b/(I_s+I_d)$. In short, the results in Table I shows that we can use the change of $I_d/(I_s+I_d)$ or $I_b/(I_s+I_d)$ to determine the breakdown location in the channel or in the drain edge region.

By utilizing the above technique, the device electrical behavior in *c*-SBD and *e*-SBD devices were characterized. In Fig. 1, the gate current and the substrate current as a function of V_g in a fresh, *c*-SBD, and an *e*-SBD *n*MOSFET were compared. The result shows that the substrate current increases drastically after *c*-SBD, but has little change after *e*-SBD. The substrate current at a positive gate bias is attributed to valence electron tunneling from the channel to the gate. The generated holes left behind in the channel then flow to the substrate. This tunneling process is unlikely to occur in the n^+ drain region since the valence-band edge of the n^+ drain is aligned with the band gap of the n^+ poly-gate.

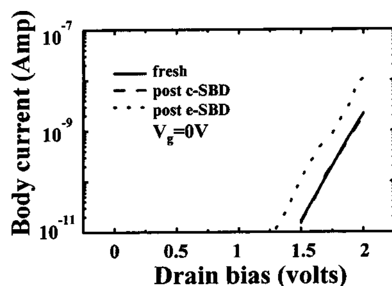

FIG. 2. Body current versus drain bias in *n*MOSFETs. Solid line refers to an unstressed device and dashed line (dotted line) refers to a device after channel SBD (drain edge SBD).

Thus, I_b is enhanced significantly at a positive gate bias in a *c*-SBD device due to localized effective oxide thinning[14,17,18] while I_b in an *e*-SBD device is nearly unchanged. Figure 2 shows the drain bias dependence of the GIDL current before and after SBD. The substrate current has an apparent increase after edge SBD. This is because at a high drain bias the I_b comes from electron band-to-band tunneling in the drain depletion region and the generated holes flow to the substrate. Since the electrical field in the drain region becomes stronger after *e*-SBD due to effectively oxide thinning, the GIDL (I_b) in an *e*-SBD device is enhanced. The same phenomena in *p*-MOSFETs are also observed and the result is shown in Fig. 3.

III. MODES OF SBD ENHANCED HYSTERESIS

Two modes of SBD enhanced body potential alteration are proposed. Figure 4 illustrates two floating-body charging processes in *c*-SBD and in *e*-SBD SOI *n*MOSFETs.[19,20] In a *c*-SBD device with a positive gate bias [Fig. 4(a)], valence band electron tunneling from the channel to the gate is increased after SBD. The generated holes flow to the body and raise the body potential. Figure 4(b) shows the drain-induced floating-body charging in an *e*-SBD *n*MOSFET. Since the

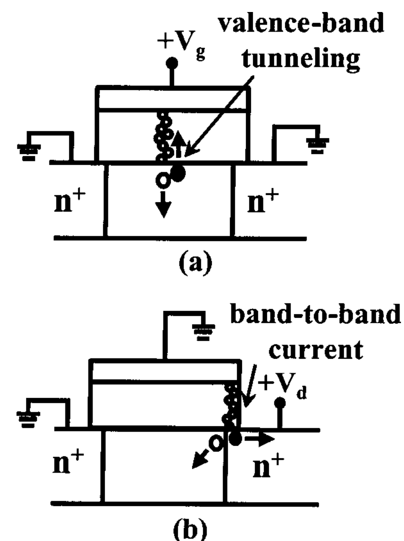

FIG. 4. Illustration of two soft-breakdown enhanced floating-body charging processes in SOI *n*MOSFETs. (a) Soft breakdown in the channel region and hole creation due to valence band electron tunneling; (b) soft breakdown in the drain region and enhanced GIDL current.

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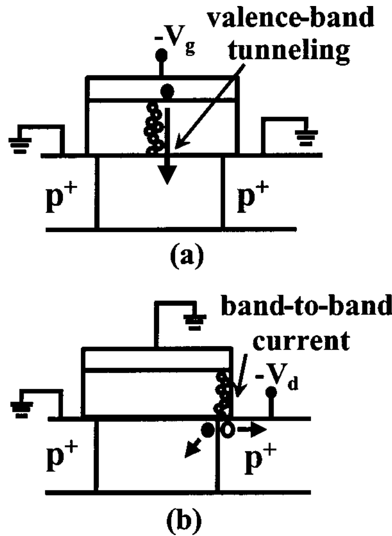

FIG. 5. Illustration of two soft-breakdown enhanced floating-body charging processes in SOI *p*MOSFETs. (a) Soft breakdown in the channel region and valence band electron tunneling from poly-gate to the floating body; (b) soft breakdown in the drain region and enhanced GIDL current.

breakdown path is in the drain edge, the GIDL current increases due to a stronger band bending in the n^+ drain region, thus raising the body potential at a high drain bias. On the contrary, the GIDL current does not change in a *c*-SBD device. Likewise, Fig. 5 shows two possible floating-body charging processes in *p*MOSFETs. Due to the above two charging processes, we conclude that the body potential of both *n*MOSFET and *p*MOSFET can be modified either during gate switching or during drain switching depending on the location of a SBD spot.

IV. RESULTS AND DISCUSSION

Figure 6 shows the $I_{\mathrm{ds}}-V_{\mathrm{gs}}$ hysteresis in a PD SOI *n*MOSFET before and after *c*-SBD. The measurement drain bias is 0.1 V. The gate bias is swept from 0 V to 1.3 V and then is reversely swept from 1.3 to 0 V. Note that (i) the subthreshold hysteresis before SBD is insignificant and (ii) the post-SBD hysteresis is induced by gate bias sweep in this device. The corresponding body potential fluctuation in gate bias sweep is shown in Fig. 6. The arrow in the figure indicates the direction of bias sweep. After *c*-SBD, the body potential begins to rise when the V_g amplitude is above 0.8 V. The gate switching induced body potential variation

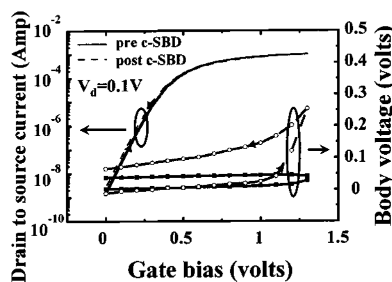

FIG. 6. Hysteresis in I_{ds} and corresponding floating-body potential versus V_g in a *c*-SBD SOI *n*MOSFETs. Measurement is performed with forward and then reverse drain sweeps from 0 V to 1.3 V.

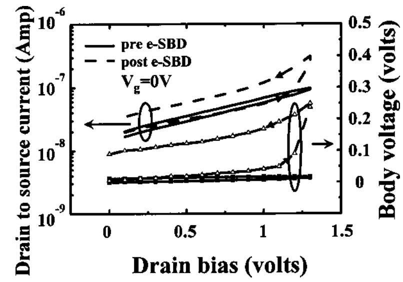

FIG. 7. Hysteresis in subthreshold current and corresponding floating-body potential in an *e*-SBD SOI *n*MOSFETs. Measurement is performed with forward and then reverse drain sweeps from 0 V to 1.3 V.

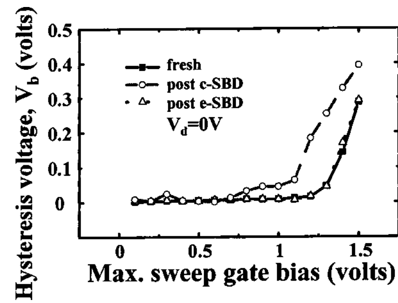

FIG. 8. The variation of body voltage V_b as a function of the amplitude of gate bias sweep in SOI *n*MOSFETs. $V_d=0$ V.

can be as large as 0.3 V in this case. The pre-SBD body potential hysteresis at the same switching amplitude is less than a few tens of millivolts. The *c*-SBD induced V_t hysteresis is also observed in a *p*MOSFET. The measurement data are not shown here.

In an *e*-SBD device, although gate enhanced hysteresis is not observed, drain sweep induced hysteresis in subthreshold leakage current is remarkable (Fig. 7). In this figure, the measurement V_{gs} is 0 V and the drain bias is swept from 0 V to 1.3 V and then reversely swept back. The body potential variation is shown in Fig. 7, too. The *e*-SBD enhanced hysteresis effect is clearly shown in this figure. It should be noted these breakdown-induced hysteresis effects occurs in off-state rather than in on-state where hot carrier impact ionization has been reported as a responsible charging mechanism.[5]

The relationship between the magnitude of sweep voltage and the body potential hysteresis in the two SBD modes is investigated. In *n*MOSFETS, the degree of hysteresis in terms of the body potential variation versus the amplitude of the sweep voltage is shown in Fig. 8 for gate bias sweep and

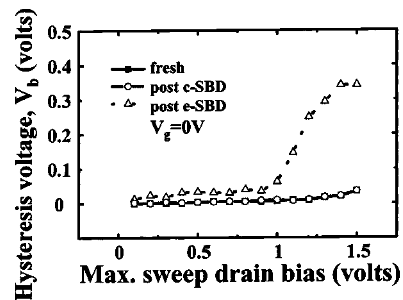

FIG. 9. The variation of body voltage V_b as a function of the amplitude of drain bias sweep in SOI *n*MOSFETs. $V_g=0$ V.

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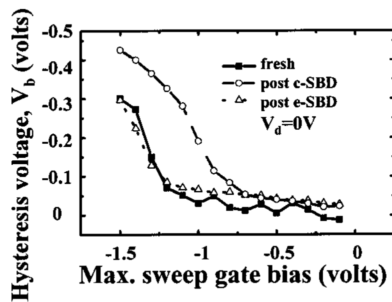

FIG. 10. The variation of body voltage V_b as a function of the amplitude of gate bias sweep in SOI *p*MOSFETs. $V_d=0$ V.

in Fig. 9 for drain bias sweep. The hysteresis voltage is defined as the maximum substrate charging voltage during the sweep. In gate bias sweep (Fig. 8), the *c*-SBD device shows an increased hysteresis voltage while the hysteresis voltage of the *e*-SBD device is almost unchanged. In contrast, the *e*-SBD device shows a larger hysteresis voltage in drain bias sweep (Fig. 9). Similar results in *p*MOSFETs are presented in Fig. 10 for gate bias sweep and in Fig. 11 for drain bias sweep. From our characterization, we found SBD induced hysteresis effect may become appreciable even when the supply voltage is below 0.8 V.

The impact of SBD enhanced body charging effect in CMOS operation is described as follows. Figure 12 illustrates the dominant V_t hysteresis modes in a SOI CMOS inverter. Hot carrier (HC) induced floating body charging occurs in on-state[1,5] and it is dominant only when the inverter is during switching. On the other hand, floating body charging takes place in *c*-SBD (*e*-SBD) *n*MOSFETs and *e*-SBD (*c*-SBD) *p*MOSFETs when the input signal is at high (low) state. Since the soft breakdown induced body charging is in the off-state, the time for charging can be much longer than the on-state HC caused body charging. Our study reveals that SBD in PD SOI MOSFETs not only increases leakage current but also affects circuit stability.

V. CONCLUSIONS

The significance of soft breakdown position to V_t hysteresis in PD SOI CMOS devices has been evaluated. Two SBD enhanced hysteresis modes in off-state CMOS are identified. The dominant floating body charging mechanism is valence band tunneling in *c*-SBD devices and band-to-band tunneling

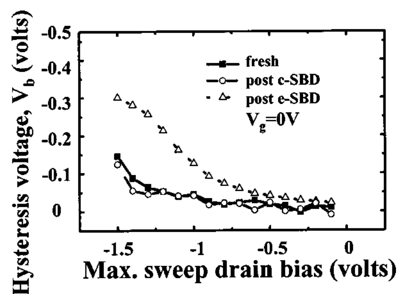

FIG. 11. The variation of body voltage V_b as a function of the amplitude of drain bias sweep in SOI *p*MOSFETs. $V_g=0$ V.

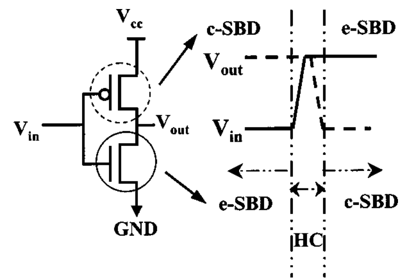

FIG. 12. Illustration of dominant V_t hysteresis modes in the switching of an SOI CMOS inverter.

in *e*-SBD devices. The SBD enhanced hysteresis effect may occur even with supply voltage less than 1.0 V and would be a serious reliability concern in ultrathin oxide PD SOI circuits.

ACKNOWLEDGMENTS

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