Edge quantum yield in n-channel metal-oxide-semiconductor field-effect transistor

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Edge quantum yield in *n*-channel metal-oxide-semiconductor field-effect transistor

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The quantum yield of impact ionization is performed on an *n*-channel metal-oxide-semiconductor field-effect transistor (*n*-MOSFET) by a carrier separation measurement. When the *n*-MOSFET is biased in accumulation, the carrier separation measurement demonstrates that the gate current mainly originates from the electrons injected into the underlying drain/source overlap regions. The measured substrate current is due to excess holes originating from the impact ionization of the injected electrons in the overlap regions. Therefore, the quantum yield in the overlap regions can be determined by the ratio of the substrate current to the gate current. It is well matched with the theoretical calculation of quantum yield. © *2004 American Institute of Physics.*
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p-channel metal-oxide-semiconductor field-effect transistors (*p*-MOSFETs) are generally used in the study of quantum yield of impact ionization for electrons in silicon. The quantum yield experiment by a carrier separation configuration can essentially assess the energy of electrons injected into the gate oxide.[1] Such an experiment on n^+-poly gate *p*-MOSFETs in the stress-induced leakage current mode has evidenced the inelastic trap-assisted tunneling mechanism of injected electrons.[2] For p^+-poly gate *p*-MOSFETs the inelastic trap-assisted tunneling mechanism in the stress-induced leakage current mode has also been proposed.[3] Recently, it has been reported that quantum yield experiments can be performed directly on a triple well structure of *n*-channel metal-oxide-semiconductor field-effect transistors (*n*-MOSFETs).[4] Therefore, this work focuses on the gate-to-drain/source overlap regions of an *n*-MOSFET.

The *n*-MOSFET with n^+-poly gate was fabricated in a state-of-the-art 0.15 μm process. The gate width/length aspect ratio is 100 μm/0.13 μm. In this process, the gate oxide was thermally grown in dilute oxygen ambient. The physical gate oxide thickness was determined to be 2.6 nm by using an $I-V$ fitting method.[5] A schematic illustration of the experimental set-up of the carrier separation measurement is shown in Fig. 1.

Figure 2 depicts the dependence of the measured gate current I_G, drain current I_D, source current I_S, and substrate current I_B on the gate voltage V_G in accumulation. This figure concludes three points. First, $I_D \approx I_S$ indicates the symmetry of experimental set-up. Second, $I_G \approx I_D + I_S$ satisfies in the direct tunneling regime ($-4\ \mathrm{V} < V_G < 0$). It effectively points out that the electron current paths are mainly from the gate terminal to the drain and source terminals, as plotted in Fig. 1. Third, since the substrate current has a negative sign, this indicates that the impact ionization induced holes flow down into the substrate. However, these holes could be either generated in the overlap regions or in the substrate region.

The quantum yield experiment gives strong evidence to the validity of the impact ionization in the overlap regions. The quantum yield γ, which is determined by the ratio of the substrate current I_B to the gate current I_G, is described as a function of the electron energy E_e. Assuming the electron energy E_e is equal to the potential drop across the oxide ($E_e = qV_{ox}$), featuring quasiballistic transport. In the gate-to-overlap regions, the oxide voltage V_{ox} is expressed as

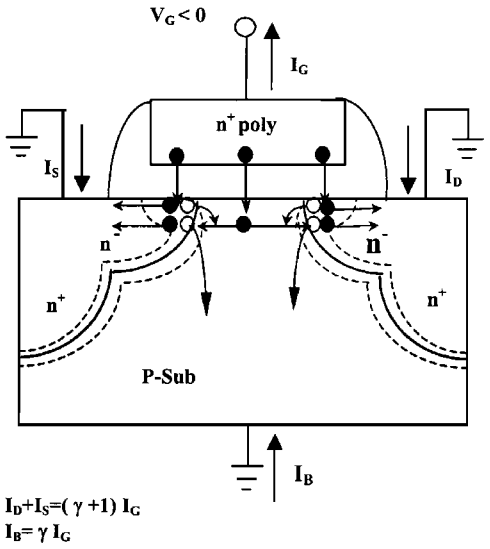

FIG. 1. A schematic illustration of the quantum yield experiment in the *n*-MOSFET. The closed and open circles represent electrons and holes, respectively. The dotted lines represent the depletion region edges.

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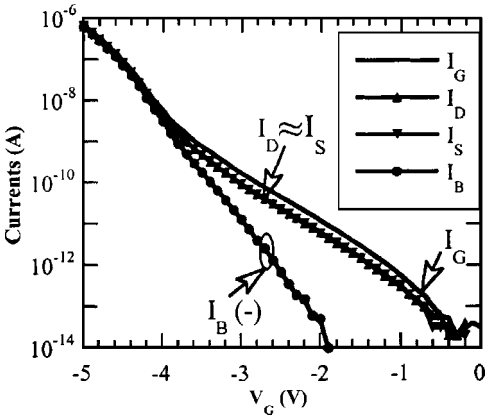

FIG. 2. Four terminal currents of the *n*-MOSFET are measured in accumulation. The polarity of the substrate current I_B is especially pointed out.

$V_G - V_d$, where V_d is the overlap band bending. V_d can be obtained by using a depletion approximation. Due to the coincidence between the resulting ratio γ in the overlap regions and the quantum yield theory,[6] as shown in Fig. 3, it is named as ''edge quantum yield'' in this work. On the other hand, the possibility of impact ionization in the substrate region is also considered. Similarly, the V_{ox} in the gate-to-substrate region is expressed as V_G-E_g/q, where E_g/q is the silicon band gap in volts. The discrepancy between the resulting ratio γ in the substrate region and the quantum yield theory,[6] especially at $-3\ \mathrm{V} < V_G < 0$, is shown in Fig. 3. It is

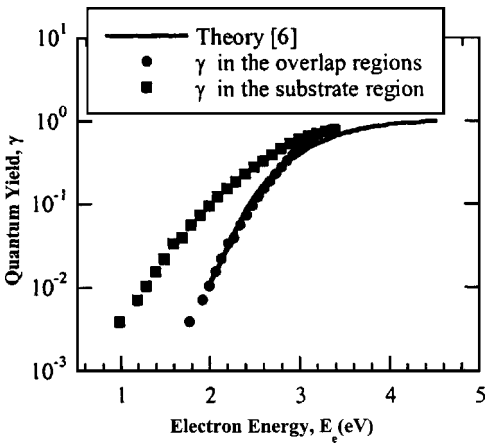

FIG. 3. Quantum yield, $\gamma(=I_B/I_G)$, is described as a function of the electron energy E_e. The closed circles and squares represent the quantum yield in the overlap regions and the substrate region, respectively.

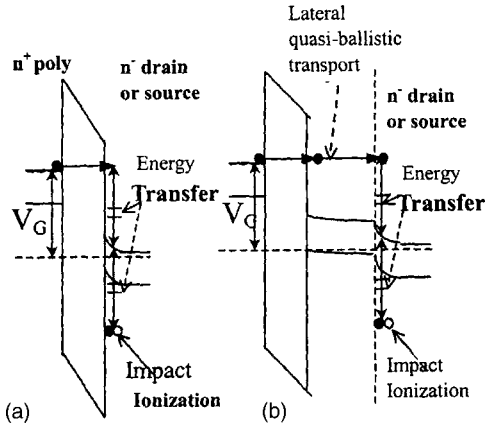

FIG. 4. Energy-band diagram in the overlap regions is given for (a) n^+-poly gate/n^--drain or source (b) n^+-poly gate/*p*-substrate/n^--drain or source.

reasonable to infer that the impact ionization in the substrate region is negligible due to a small channel length.

To further interpret the edge quantum yield, the energy-band diagram in the overlap regions is depicted as follows. Figure 4(a) shows how the injected electrons from the gate to drain/source overlap regions transfer energy via impact ionization. A more interesting phenomenon is highlighted in Fig. 4(b) for the electrons injected into the substrate. We assume that since a small channel length allows lateral quasiballistic behavior, the energetic electrons will traverse to the drain/source collectors without energy loss. When these ''hot'' electrons enter the overlap depletion regions, they would transfer the energy via impact ionization to become ''cold'' electrons eventually.

In conclusion, the edge quantum yield experiment has been successfully performed on an *n*-MOSFET and its physical basis has been clarified. The experimental data are in excellent agreement with theoretical calculation.

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