Pocket Implantation Effect on Drain Current Flicker Noise in Analog nMOSFET Devices

Jun-Wei Wu, *Student Member, IEEE*, Chih-Chang Cheng, Kai-Lin Chiu, Jyh-Chyurn Guo, Wai-Yi Lien, Chih-Sheng Chang, Gou-Wei Huang, and Tahui Wang, *Senior Member, IEEE*

***Abstract*—The pocket implantation effect on drain current flicker noise in 0.13 μm CMOS process based high performance analog nMOSFETs is investigated. Our result shows that pocket implantation will significantly degrade device low-frequency noise primarily because of nonuniform threshold voltage distribution along the channel. An analytical flicker noise model to account for a pocket doping effect is proposed. In our model, the local threshold voltage and the width of the pocket implant region are extracted from the measured reverse short-channel effect, and the oxide trap density is extracted from a long-channel device. Good agreement between our model and the measurement result is obtained without other fitting parameters.**

***Index Terms*—Flicker noise, modeling, nonuniform threshold voltage, pocket implant.**

I. Introduction

THE CMOS technology, which possesses the advantage of low cost, high integration, and low power, is finding more and more important applications in the area of mixed mode and RF ICs. As compared with bipolar transistors, CMOS devices exhibit large noise, especially in the low-frequency region where flicker noise is dominant [1]. Flicker noise will affect the signal-to-noise ratio in operational amplifiers and in analog/digital and digital/analog converters. Phase noise of voltage-controlled oscillators originating from flicker noise is another concern for RF applications [2]. In order to reduce low-frequency noise in analog devices, the physical origin of flicker noise in today's CMOS devices should be further explored.

Pocket implantation is necessary in CMOS process to reduce the subthreshold leakage in logic devices. However, it has some drawbacks in analog circuits, such as the increase of drain-substrate coupling, poor Early voltage, lower high-frequency output resistance [3] and increased nonlinearity [4]. Recent study has shown that pocket implantation will also degrade drain current flicker noise [3]–[7]. New MOSFET structures, such as single pocket, asymmetric channel structure, [3], [5] and epitaxial channel MOSFETs [6], [7], were proposed to reduce flicker noise by elimination of pocket implantation. Although some researchers suspected that the increase of low-frequency noise in pocket-implanted devices results from additional oxide trap creation by pocket implantation [7], the real cause of pocket implantation induced noise degradation is still not clear. The purpose of this paper is to investigate pocket implantation effect on flicker noise in nMOSFETs with various pocket doses and device dimensions. An analytical flicker noise model taking into account a pocket doping effect will be proposed.

The input/output nMOSFETs of a 0.13-μm CMOS technology is used in this work. The I/O devices have a 5.8-nm gate oxide, a gate length from 0.22 to 10 μm, and a gate width of 10 μm. Two pocket implant doses were used. Due to the statistical nature of the flicker noise, devices with too small an area may exhibit a large fluctuation range in noise [8]. In this paper, each noise measurement data point represents an average of three to ten devices. The normalized noise power spectrum density $(S_{\rm id}/I_d^2)$ is chosen as a monitor of drain current noise, which is considered to be a fair index because of the normalization to the drain current. In addition, charge pumping measurement is performed to characterize oxide (interface) trap density for different pocket implant splits.

According to the unified flicker noise model [9], the normalized noise power spectrum density $(S_{\rm id}/I_d^2)$ has the following simple analytic form at very low drain voltages:

$$\frac{S_{\rm id}}{I_d^2} = \frac{kT}{\gamma f W L_{\rm eff}^2} \int_0^{L_{\rm eff}} N_t(E_{\rm fn}, x) \left[\frac{1}{N(x)} + \alpha\mu\right]^2 dx \qquad (1)$$

where $\gamma \approx 10^8$ cm^{-1} is the attenuation coefficient of the electron wave function in the oxide [10], α is the scattering coefficient [11], $N(x)$ is the number of channel carriers per unit area, and $N_t(E_{\rm fn}, x)$ is the oxide trap density at the Fermi level $E_{\rm fn}$. The $1/N(x)$ term in the bracket represents charge number fluctuation and the $\alpha\mu$ term is from mobility fluctuation. For nMOSFETs at a low gate overdrive bias, $\alpha\mu$ is smaller than $1/N(x)$, which means that the number fluctuation mechanism dominates noise behavior.

II. Measurement Result and Discussion

Fig. 1 shows the diagram of an nMOSFET with pocket implantation. Pocket implantation will cause nonuniform threshold voltage distribution along the channel and may create additional oxide traps N_t near the source/drain edge. According

Manuscript received October 15, 2003; revised March 2, 2004. This work was supported in part by the National Science Council of Taiwan, R.O.C., under Contract NSC92-2215-E009-024 and in part by Taiwan Semiconductor Manufacturing Company. The review of this paper was arranged by Editor M. J. Deen.

J.-W. Wu, C.-C. Cheng, J.-C. Guo, and T. Wang are with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300, Taiwan, R.O.C.

K.-L. Chiu is with United Microelectronics Corporation, Hsinchu 300, Taiwan, R.O.C.

W.-Y. Lien and C.-S. Chang are with the Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan, R.O.C.

G.-W. Huang is with the National Nano Device Laboratories, Hsinchu 300, Taiwan, R.O.C.

Digital Object Identifier 10.1109/TED.2004.831369

0018-9383/04$20.00 © 2004 IEEE

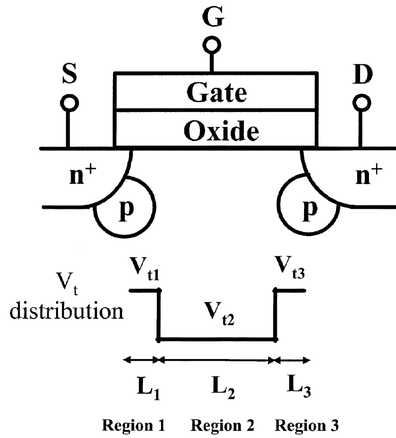


Fig. 1. Diagram of pocket implant-induced nonuniform threshold voltage distribution along the channel. Regions 1 and 3 are the pocket implant-affected region and possess a higher threshold voltage. Region 2 represents the rest of the channel.

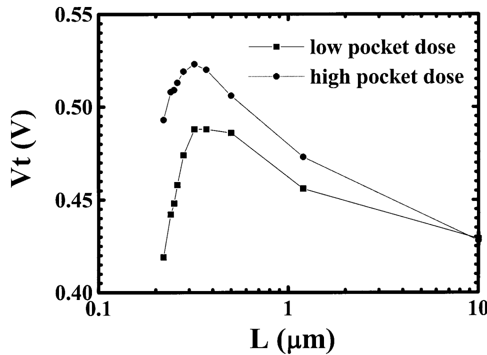
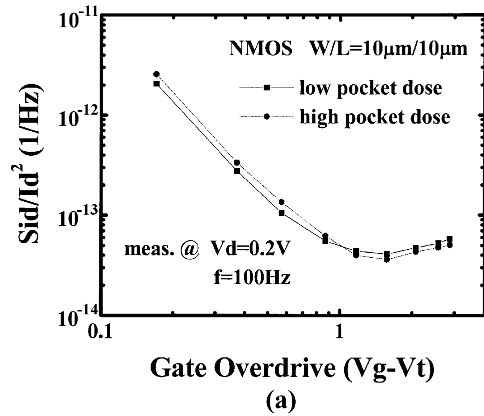


Fig. 2. Reverse SCE for low/high pocket doses.



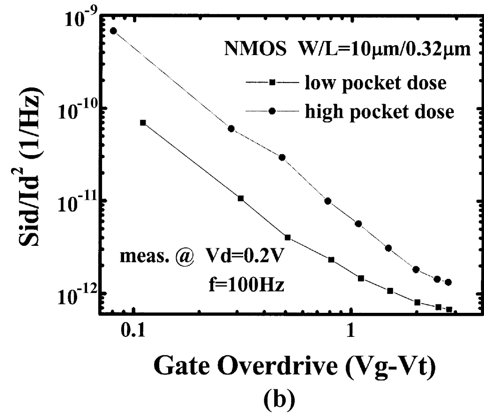


Fig. 3. Normalized noise power spectrum density versus gate overdrive voltage $(V_g–V_t)$ for low/high pocket doses. The noise is measured in the linear regime. (a) nMOS $(W/L = 10/10\ \mu\text{m})$, and all data points are averaged from three devices. (b) nMOS $(W/L = 10/0.32\ \mu\text{m})$, and all data points are averaged from ten devices.

to (1), both nonuniform V_t distribution and oxide trap creation affect drain current flicker noise. Two pocket implant doses are compared in this study. The higher pocket dose is about 2.2 times larger than the lower one. Fig. 2 shows the reverse short-channel effect (RSCE) of nMOSFETs of the two doses. As expected, the higher pocket implant dose shows a larger RSCE. The short-channel effect (SCE) becomes dominant for a gate length below 0.3 μm. The measured noise behavior of these two pocket implant splits is shown in Fig. 3. The comparison is made at the same gate overdrive voltage $(V_g–V_t)$. To avoid the complication resulting from the SCE in the analysis of noise, two gate lengths $L_g = 0.32$ and 10 μm) in the RSCE regime are used for study. The noise is measured in linear operation regime $(V_d = 0.2$ V) that the inversion charge is not affected by the drain bias. The noise data point shown in Fig. 3 is obtained at $f = 100$ Hz. For a long-channel device [$L_g = 10\ \mu$m, Fig. 3(a)], the noise of the two different pocket split devices is almost the same without regard to a considerably different pocket dosage. Fig. 3(b) shows the noise in two shorter gate length $(L_g = 0.32\ \mu\text{m})$ devices with the same pocket split. The higher pocket dose device apparently exhibits much worse noise behavior in the entire range of gate bias. Fig. 4 shows the measured flicker noise versus gate length for the two pocket dosages. The pocket implant-induced noise degradation is more significant in a shorter gate length device because the pocket implant region occupies a larger portion of the channel.

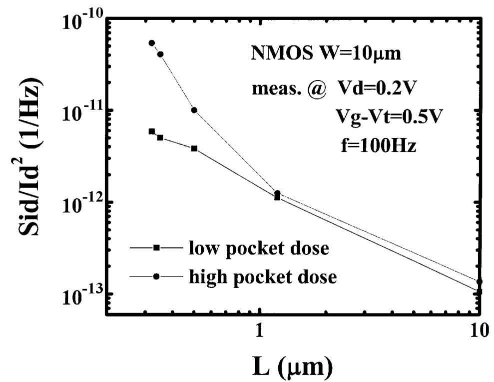


Fig. 4. Normalized noise power spectrum density versus gate length for low/high pocket doses. The noise is measured at the same gate overdrive voltage.

Previous work attributed the severe noise degradation in a pocket-implanted device to more oxide trap creation due to pocket implant [12]. In order to clarify this point, we measured the charge pumping current for the two pocket splits. Nearly the same result is obtained in Fig. 5 with extracted interface trap density about $1.6 \times 10^{10} 1/\text{cm}^2$. This implies that the two implant splits yield almost the same trap density in gate oxide. Thus, the more severe noise degradation in the higher pocket dose device in Fig. 3(b) cannot be explained simply by implant caused oxide trap creation. Rather, a nonuniform

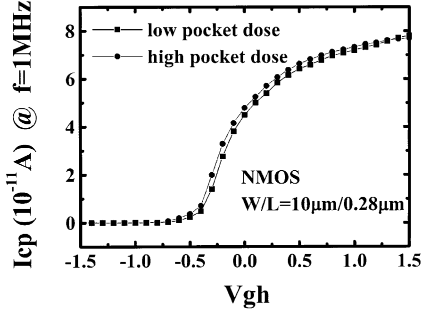


Fig. 5. Charge pumping current versus the high level of gate pulse ($V_{\rm gh}$) in charge pumping measurement for low/high pocket doses.

threshold voltage distribution along the channel resulting from pocket implant should be responsible for the observed noise degradation. A simple analytic model is proposed to explain a nonuniform threshold voltage effect on noise degradation.

III. Noise Modeling Including Pocket Implant

In our model, the channel of an nMOSFET is divided into three regions, as suggested in [13], [14]. Regions 1 and 3 in Fig. 1 represent a pocket region, where the local threshold voltage (V_t) is increased due to pocket implantation. Region 2 represents the rest of the channel and possesses a lower V_t. In our model, the $S_{\rm id}$ is divided into three terms by introducing the nonuniform V_t distribution into the $N_(x)$ term. At a relatively low gate overdrive bias, the mobility fluctuation term in (1) can be neglected. In addition, since the oxide (interface) trap density is not affected by pocket implantation process, a uniform distribution of oxide trap density along the channel is assumed. Based on these assumptions, (1) can be reduced to

$$\begin{aligned}\frac{S_{\rm id}}{I_d^2} &= \frac{kT}{\gamma f W L_{\rm eff}^2} N_t(E_{\rm fn}) \\ &\quad \times \left[\int_{L_1} \frac{1}{N_1^2(x)}dx + \int_{L_2} \frac{1}{N_2^2(x)}dx + \int_{L_3} \frac{1}{N_3^2(x)}dx\right] \\ &\approx \frac{kTq^2}{\gamma f W L_{\rm eff}^2 C_{\rm ox}^2} N_t(E_{\rm fn}) \\ &\quad \times \left[\frac{L_1}{(V_g - V_{t1})^2} + \frac{L_2}{(V_g - V_{t2})^2} + \frac{L_3}{(V_g - V_{t3})^2}\right] \quad (2)\end{aligned}$$

where N_1 and N_3 represent conducting charge density in region 1 and region 3, which are modulated by pocket implant dosage. In the long-channel devices ($L_g = 10\ \mu$m), the noise component arising from the pocket implantation regions is relatively small. This argument is evident from Fig. 3(a) that the noise is nearly the same for different pocket splits in long-channel devices. In other words, the second term in (2), i.e., L_2 region, is dominant in a long-channel device. From the measured noise and threshold voltage in a long-channel device, the oxide trap density $N_t(E_{\rm fn})$ can be extracted. The result is shown in Table I. The measured and calculated results of noise level in a long-channel device are shown in Fig. 6. Good agreement between our model and measurement result is achieved in a low gate overdrive voltage regime where the number fluctuation is dominant.

TABLE I
Values of Pocket Region Length, Threshold Voltage and Oxide Trap Density for Low/High Pocket Doses

	Low Pocket Dose	High Pocket Dose
$N_t(E_{fn})$	1.7x10^{11} cm^{-2}	1.8x10^{11} cm^{-2}
L_1=L_3	62nm	71nm
V_{t2}	0.43 V	0.43 V
V_{t1}=V_{t3}	0.50 V	0.61 V

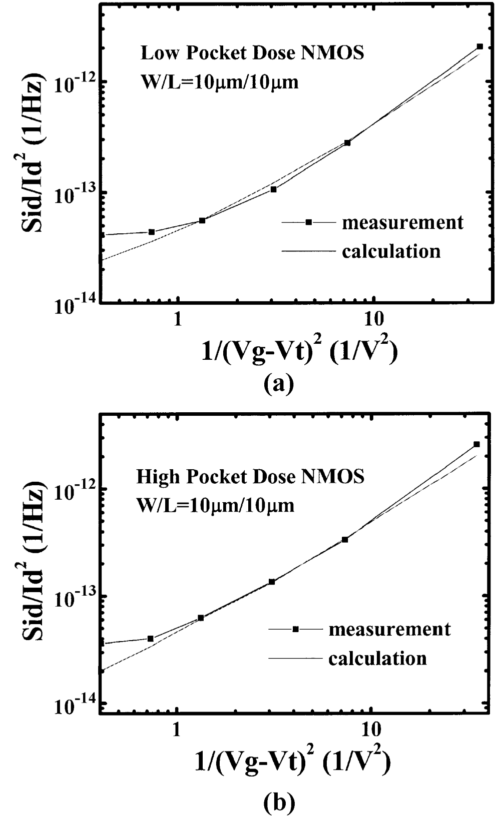


Fig. 6. Comparison of calculated and measured noise results for nMOS with $W/L = 10/10\ \mu$m. (a) Low pocket dose. (b) High pocket dose.

For noise calculation in short-channel devices, the respective parameters in the pocket region must be extracted first. The effective channel length is about $L_{\rm eff} = L_{\rm mask} - 0.06\ \mu$m, which is evaluated from the shift and ratio method [15]. The width and the local V_t of the pocket regions can be extracted from the measured RSCE by using the method in [16] and [17]. The extracted parameters used in our model are given in Table I. The measured and calculated results in 0.32 μm devices are shown in Fig. 7. No other fitting parameters are used.

It should be remarked that a small difference between modeled and measured results is noticed in Figs. 6 and 7 at a higher gate overdrive bias. The reason is that the mobility fluctuation mechanism ($\alpha\mu$) plays a part in drain current noise at a high gate overdrive bias.

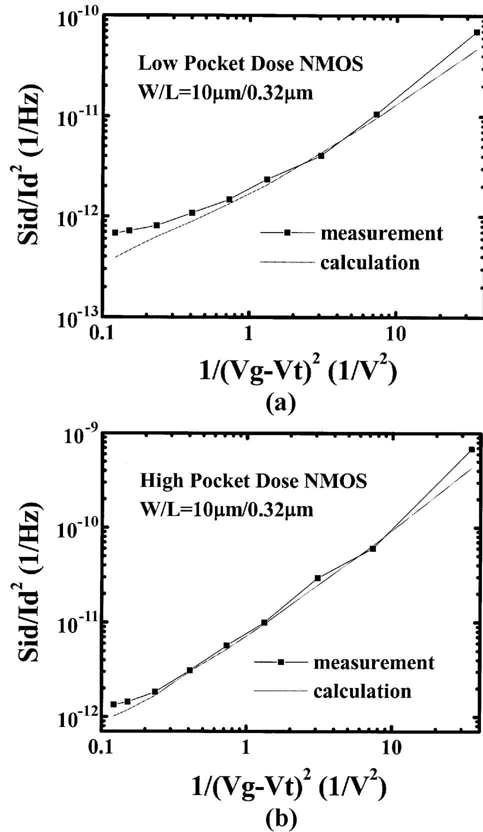


Fig. 7. Comparison of calculated and measured noise results for nMOS with $W/L = 10\ \mu m/0.32\ \mu m$. (a) Low pocket dose. (b) High pocket dose.

IV. Conclusion

Pocket implantation effect on drain current flicker noise in nMOSFETs is investigated. The result shows that nonuniform threshold voltage distribution along the channel caused by pocket implantation is responsible for flicker noise degradation in a short-channel device. This effect will become more significant as channel length is further reduced. A simple analytical noise model including pocket implantation effect for various gate length devices has been developed and can be easily implemented into a circuit simulator.

References

[1] A. van der Ziel, *Noise in Solid State Devices and Circuits*. New York: Wiley, 1986.

[2] A. Hajimiri and T. H. Lee, "A general theory of phase noise in electrical oscillators," *IEEE J. Solid-State Circuits*, vol. 33, pp. 179–194, Jan. 1998.

[3] A. Chatterjee, K. Vasanth, D. T. Crider, M. Nandakumar, G. Pollack, R. Aggarwal, M. Rodder, and H. Shichijo, "Transistor design issues in integrating analog functions with high performance digital CMOS," in *Symp. VLSI Tech. Dig.*, 1999, pp. 147–148.

[4] Q. Li and J. S. Yuan, "Linearity analysis and design optimization for 0.18 μm CMOS RF mixer," in *Proc. Circuits, Devices Systems*, 2002, pp. 112–118.

[5] H. V. Deshpande, B. Cheng, and J. C. S. Woo, "Analog device design for low power mixed mode applications in deep submicrometer CMOS technology," *IEEE Electron Device Lett.*, vol. 22, pp. 588–590, July 2001.

[6] T. Ohguro, H. Naruse, H. Sugaya, H. Kimijima, E. Morifuji, T. Yoshitomi, T. Morimoto, H. S. Momose, Y. Katsumata, and H. Iwai, "0.12 μm raised gate/source/drain epitaxial channel nMOS technology," in *IEDM Tech. Dig.*, 1998, pp. 927–930.

[7] T. Ohguro, R. Hasumi, T. Ishikawa, M. Nishigori, H. Oyamatsu, and F. Matsuoka, "An epitaxial channel MOSFET for improving flicker noise under low supply voltage," in *Symp. VLSI Tech. Dig.*, 2000, pp. 160–161.

[8] R. Brederlow, W. Weber, D. S.-Landsiedel, and R. Thewes, "Fluctuations of the low-frequency noise of MOS transistors and their modeling in analog and RF-circuits," in *IEDM Tech. Dig.*, 1999, pp. 159–162.

[9] K. K. Hung, P. K. Ko, C. Hu, and Y. C. Cheng, "A unified model for the flicker noise in metal–oxide–semiconductor field-effect transistors," *IEEE Trans. Electron Devices*, vol. 37, pp. 654–665, Apr. 1990.

[10] S. Christensson, I. Lundsstrom, and C. Svensson, "Low-frequency noise in MOS transistors—One theory," *Solid State Electron.*, vol. 11, p. 797, 1968.

[11] T. H. Ning and C. T. Sah, "Theory of scattering of electrons in a nondegenerate-semiconductor-surface inversion layer by surface-oxide charges," *Phys. Rev. B, Condens. Matter*, vol. 6, p. 4605, 1972.

[12] J. W. Wu, H. C. Chang, and T. Wang, "Oxide soft breakdown effects on drain current flicker noise in ultra-thin oxide CMOS devices," in *Proc. SSDM*, 2002, pp. 698–699.

[13] M. H. Tsai and T. P. Ma, "The impact of device scaling on the current fluctuations in MOSFETs," *IEEE Trans. Electron Devices*, vol. 41, pp. 2061–2068, Nov. 1994.

[14] Z. Celik-Butler and P. Vasina, "Channel length scaling of 1/f noise in 0.18-μm technology MDD nMOSFETs," *Solid State Electron.*, vol. 43, pp. 1695–1701, 1999.

[15] Y. Taur, "MOSFET channel length: extraction and interpretation," *IEEE Trans. Electron Devices*, vol. 47, p. 160, Jan. 2000.

[16] R. Rios, W.-K. Shih, A. Shah, S. Mudanai, P. Packan, T. Standford, and K. Mistry, "A three-transistor threshold voltage model for halo processes," in *IEDM Tech. Dig.*, 2002, pp. 113–116.

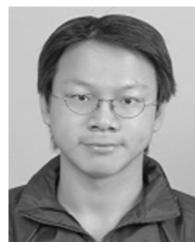
[17] H. van Meer, "Limitation of shift-and ratio based Leff extraction techniques for MOS transistors with halo or pocket implants," *IEEE Electron Device Lett.*, vol. 21, p. 133, Feb. 2000.

Jun-Wei Wu (S'02) was born in Tao-Yuan, Taiwan, R.O.C. He received the B.S. degree in electronics engineering, in 1998, from National Chiao-Tung University, Hsinchu, Taiwan, where he is currently pursuing the Ph.D. degree in electronics engineering.

His research interest includes RF CMOS device modeling, flicker noise characterization and modeling, and LDMOS power device modeling and reliability analysis.

Chih-Chang Cheng received the B.S. degree in physics from National Central University, Taoyuan, Taiwan, R.O.C., in 2002. He is currently pursuing the Ph.D. degree in electronics engineering at the National Chiao-Tung University, Hsinchu, Taiwan.

His research interest includes high-voltage power devices and flicker noise.



Kai-Lin Chiu was born in Kaohsiung, Taiwan, R.O.C. in 1978. He received the B.S. and M.S. degree, in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 2001 and 2003, respectively.

In 2004, he joined United Microelectronics Corporation, Hsinchu, where he was engaged in the development and characterization of mixed-mode technology. His research interests includes the reliability issues and analog performance of CMOS.

Jyh–Chyurn Guo was born in Taiwan, R.O.C., in 1960. She received the B.S.E.E. and M.S.E.E. degrees from the National Tsing-Hua University (NTHU), Hsinchu, Taiwan, in 1982 and 1984, respectively, and the Ph.D. degree in electronics engineering from the National Chiao-Tung University (NCTU), Hsinchu, in 1994. The subject of her Ph.D. dissertation was "A new parameter extraction technique and modeling for miniaturized MOSFETs."

She joined NCTU's electronics engineering faculty in 2003, and before that, she has been working in the semiconductor industry with a focus on device design and VLSI technology development. In 1984, she joined the Electronics Research and Service Organization/Industrial Technology Research Institute (ERSO/ITRI), where she was engaged in diversified semiconductor integrated circuit technologies. From 1984 to 1990, she was with the high-voltage bipolar/CMOS/DMOS integrated circuit project responsible for high-voltage and power device simulation and design. Since 1991, she had been with the submicrometer project in ERSO/ITRI and working on the process simulation and device design for high-speed SRAM technology. From 1994 to 1998, she was with Macronix International Corporation where she was engaged in the high-density and low-power Flash memory technology development and led a team responsible for Flash memory device design and reliability analysis. In 1998, she joined Vanguard International Semiconductor Corporation, where she served as a Department Manager responsible for advanced DRAM device design with a major focus on 0.18–μm 64-M DRAM development. In 2000, she joined Taiwan Semiconductor Manufacturing Company, where she served as a Program Manager in charge of 0.1-μm logic CMOS FEOL technology development. Since 2001, she has been engaged in HPA and RF CMOS technology development, and led a team focusing on 0.13-μm CMOS-based mixed-signal and RF device design. She has authored or coauthored around 30 technical papers and has been granted about ten international patents in her professional field. Her current research interests are RF CMOS and HPA device design and modeling, novel nonvolatile memory technology, and circuit technology for SoC.

Wai–Yi Lien was born in Taiwan, in 1963. He received the Ph.D. degree in power mechanical engineering from National Tsing-Hua University, Hsinchu, Taiwan, R.O.C., in 1995.

He joined the Logic Technology Division, Taiwan Semiconductor Manufacturing Company Ltd., Hsinchu, in 1995. He has done extensive research in DRAM, mixed signal and RF processes of CMOS technology, and 3-D electromagnetic simulation on RF passive components.

Chih-Sheng Chang was born in Hualien, Taiwan, R.O.C., on November 3, 1964. He received the B.S. and M.S. degrees in electrical engineering from National Taiwan University, Taipei, in 1986 and 1990, respectively, and the Ph.D. degree from the Department of Electrical and Computer Engineering, University of Illinois, Urbana-Champaign, in 1996.

Since 1999, he has been with Taiwan Semiconductor Manufacturing Company (TSMC), Ltd., Hsinchu, where he has worked on TCAD, MOS device design, and RF devices optimization and characterization. He has been the main device designer for TSMC's 0.15-μm and 0.13-μm high-speed devices. Currently, he is a Technology Manager in the Communication Technology Department, Logic Technology Division, where he is in charge of the development of RF active and passive devices for 0.18-, 0.13-, and 90-nm technologies.

Gou-Wei Huang was born in Taipei, Taiwan, R.O.C., in 1969. He received the B.S. degree in electronics engineering and the Ph.D. degree from National Chiao-Tung University, Hsinchu, Taiwan, in 1991 and 1997, respectively.

He joined National Nano Device Laboratories, Hsinchu, in 1997 as an Associate Researcher. His current research interests focus on microwave device design, characterization, and modeling.

Tahui Wang (M'86–SM'94) was born in Taoyuan, Taiwan, R.O.C., on May 3, 1958. He received the B.S.E.E. degree from National Taiwan University, Taipei, in 1980 and the Ph.D. degree in electrical engineering from the University of Illinois, Urbana-Champaign, in 1985.

From 1985 to 1987, he was with Hewlett-Packard Laboratories, Palo Alto, CA, where he was engaged in the development of GaAs HEMT devices and circuits. Since 1987, he has been with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, where he is currently a Professor. His research interests include hot-carrier phenomena characterization and reliability physics in VLSI devices, RF CMOS devices and nonvolatile semiconduct or devices.

Dr. Wang was given the Best Teacher Award by Taiwan's Ministry of Education. He has served as technical committee member of many international conferences, among them IEDM, IRPS, and VLSI-TSA.