Design on ESD Protection Scheme for IC With Power-Down-Mode Operation

Ming-Dou Ker, *Senior Member, IEEE,* and Kun-Hsien Lin, *Student Member, IEEE*

***Abstract*—This paper presents a new electrostatic discharge (ESD) protection scheme for IC with power-down-mode operation. Adding a VDD ESD bus line and diodes into the proposed ESD protection scheme can block the leakage current from I/O pin to VDD power line and avoid malfunction during power-down operation. The whole-chip ESD protection design can be achieved by insertion of ESD clamp circuits between VSS power line and both the VDD power line and VDD ESD bus line. Experiment results show that the human-body model (HBM) ESD level of this new scheme can be greater than 7.5 kV in a 0.35-μm silicided CMOS process.**

***Index Terms*—Electrostatic discharge (ESD), ESD bus, ESD protection scheme, leakage current, power-down mode.**

I. Introduction

THE power-down-mode feature currently plays an important role in portable and mobile system-on-a-chip (SOC) products that require effective power saving. In order to achieve IC power-down-mode operation, modification on the design of I/O circuits and electrostatic discharge (ESD) protection circuits has been studied [1], [2]. The traditional ESD protection scheme, as shown in Fig. 1(a), will have leakage issues when power-down-mode operation is applied to the IC. If the VDD power line is grounded and the I/O voltage level is high, a large leakage current will be induced from the input or output pads to the VDD power line through the parasitic diodes of the output pMOS (Mp_out) or the input ESD protection pMOS (Mp_in). On the other hand, if the VDD power line is floating and the I/O voltage level is high, the internal circuits of the IC may be triggered to cause malfunction by charging the VDD power line through the parasitic diodes of output pMOS or input ESD protection pMOS. Therefore, the parasitic diode of pMOS connected between the I/O pad and VDD power line must be removed to avoid leakage current or malfunction when the IC is operating in power-down-mode condition.

ESD stresses on an I/O pad have four pin-combination modes: positive-to-VSS (PS-mode), negative-to-VSS (NS-mode), positive-to-VDD (PD-mode), and negative-to-VDD (ND-mode) [3]. For the purpose of avoiding the unexpected ESD damage in the internal circuits of CMOS ICs [4]–[6], the turn-on-efficient power-rail ESD clamp circuit was often placed between VDD and VSS power lines [7]. ESD current at the I/O pad under the PS-mode ESD stress can be discharged through the parasitic diode of pMOS and the VDD-to-VSS ESD clamp circuit to ground. Consequently, the traditional I/O circuits cooperating with the VDD-to-VSS ESD clamp circuit can achieve a much higher ESD level [7]. However, the absence of the diode between the I/O pad and VDD power line for power-down-mode operation will seriously degrade ESD performance of the I/O pad under the PS-mode and PD-mode ESD stresses.

Owing to the ESD protection and leakage issue when input pad voltage exceeded VDD during normal circuit operation, the ESD protection network utilizing ESD buses was reported [8]. In addition, in order to solve the ESD protection and leakage issue for IC with power-down-mode operation, some modified designs had also been reported [9], [10]. The gate-grounded nMOS has been used to replace the diode between the I/O pad and VDD power line [9]. In [10], the design was focused on improving the ESD robustness of the ESD protection circuit between the I/O pad and VSS power line. However, the turn-on efficiency of the ESD protection device [9] or the complicated ESD protection circuit [10] is the concern to implement the approach.

In this paper, a new ESD protection scheme for IC with power-down-mode operation is proposed. This new scheme can overcome the leakage issue and have a very high ESD level for IC with power-down-mode operation. It has been successfully verified in a 0.35-μm silicided CMOS process.

II. New ESD Protection Scheme for IC With Power-Down-Mode Operation

The proposed ESD protection scheme for the IC with power-down-mode operation is shown in Fig. 1(b) with the additional ESD bus line (VDD_ESD), which is realized by wide metal line in CMOS IC. The VDD_ESD bus line is not directly connected to an external power supply pin. The diode D1 is connected between the VDD power line and VDD_ESD bus line to block the leakage current path from the input pad to VDD when the power of VDD is off. The diode D2 is connected between the VDD power line and the source of output pMOS (Mp_out) to block the leakage current path from the output pad to VDD when the power of VDD is off. The VDD_ESD bus line is not connected to the source of Mp_out in this scheme, because Mp_out may be turned on. The gate voltage of Mp_out will be dropped down and induces leakage current between I/O pads when the power of VDD is off. With the new proposed ESD protection scheme, the leakage current or malfunction issues for the IC with power-down-mode operation can be avoided. The diode D3 is connected between the output pad and VDD_ESD bus line for ESD protection purpose. One power-rail ESD clamp circuit is connected between VDD power line and VSS power line. A second power-rail ESD clamp circuit is connected between VDD_ESD bus line and VSS power line.

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The authors are with the Nanoelectronics and Gigascale Systems Laboratory, Institute of Electronics, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. (e-mail: mdker@ieee.org).

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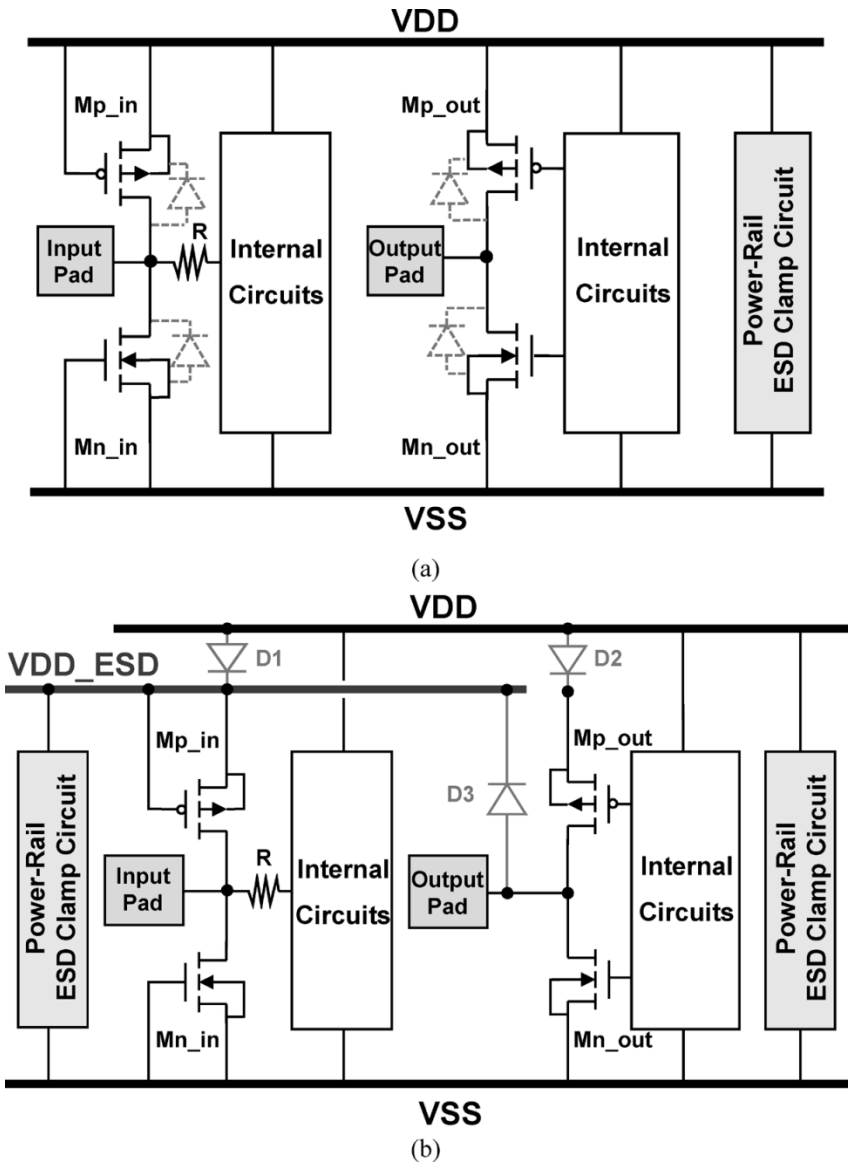

Fig. 1. (a) Traditional ESD protection scheme in a CMOS IC with pMOS and nMOS as ESD protection devices for input and output pads. (b) The new proposed ESD protection scheme for the IC with power-down-mode operation.

In the typical mixed-voltage I/O buffer, the output pMOS, connected from the I/O pad to the VDD power line, has self-biased circuits for tracking its gate and n-well voltages to avoid the leakage current path from the I/O pad to VDD when an over-VDD external signal is applied to the I/O pad [11]. However, during the power-down-mode operation, the tracking circuits will not function because the power of VDD is off. The channel of output pMOS cannot be kept off when the external voltage level on the output pad is high; therefore, the leakage current may be induced from the output pad to VDD when the power of VDD is off. By using the new proposed ESD protection scheme, the leakage current path from the I/O pad to VDD can be completely blocked by the diode D2 during the power-down-mode operation. Although the output signal cannot be pulled up to VDD (kept at VDD-Vd, where Vd is the cut-in voltage of the diode D2) during normal circuit operating condition, it can be further improved with additional output-swing improvement circuit [12]. The output signal can be fully pulled up to VDD by the output-swing improvement circuit without causing any increase of the extra leakage current.

The ESD current at the input (or output) pad under PS-mode ESD stress can be discharged through the parasitic diode of Mp_in (or the diode D3) to the VDD_ESD bus, and then discharged through the ESD clamp circuit from the VDD_ESD bus to the grounded VSS power line. The ESD current at the input (or output) pad under the PD-mode ESD stress can be discharged through the parasitic diode of Mp_in (or the diode D3) to VDD_ESD bus line, the ESD clamp circuit to VSS power line, and then through the parasitic diode of ESD clamp circuit to the grounded VDD power line. The ESD current at the input (or output) pad under the NS-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to ground. The ESD current at the input (or output) pad under the ND-mode ESD stress can be discharged through the parasitic diode of Mn_in (or Mn_out) to VSS power line, and then discharged through the VDD-to-VSS ESD clamp circuit to the

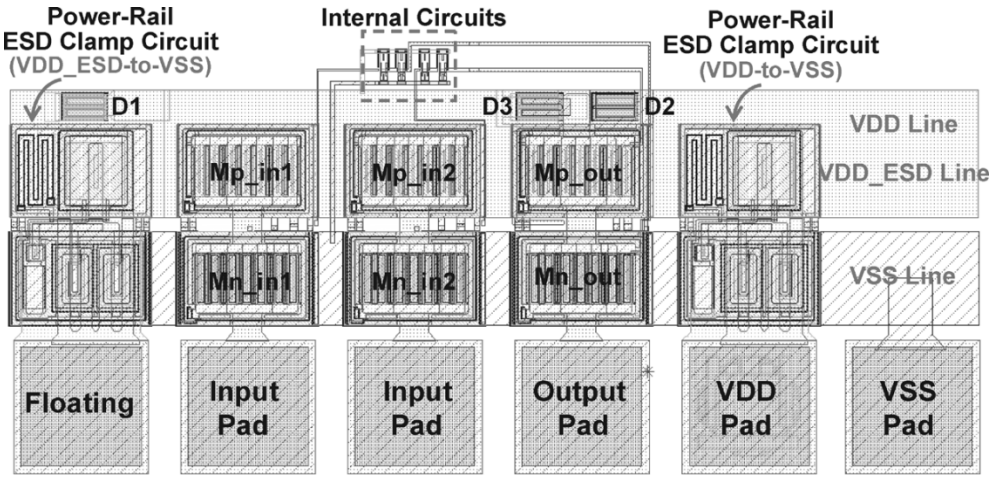

Fig. 2. Layout view of the new proposed ESD protection scheme fabricated in a 0.35-μm silicided CMOS process.

grounded VDD power line. The four modes of ESD stresses on the I/O pads can be safely protected by this new proposed ESD protection scheme.

III. Experimental Results

A. Layout Structure

The test chip with the traditional ESD protection scheme and the new proposed ESD protection scheme have been fabricated in a 0.35-μm silicided CMOS process. Fig. 2 shows the layout view of the new proposed ESD protection circuits. In order to save the layout area, the VDD_ESD bus line is realized by the different parallel metal layers, which overlaps the VDD power line. Some inverters are connected from the input pad to the output pad, being served as the internal circuits for function verification of this testchip. The input ESD protection devices are realized by the gate-connected-to-source pMOS and gate-grounded nMOS with both the device dimensions (W/L) of 490/0.5 (μm/μm). The output ESD protection devices are realized by the output buffer of pMOS and nMOS with the same device dimensions. The layout parameters of ESD protection devices and output buffers are drawn according to the foundry's ESD rules with the silicide-blocking mask. In the proposed ESD protection scheme, the junction perimeter of the diodes (D1, D2, and D3) is drawn as 50 μm. The power-rail ESD clamp circuit is realized by the substrate-triggering field-oxide device (STFOD) [13] to have high enough ESD level in a limited layout area.

B. Leakage Current

The leakage currents at the input pad and output pad of the traditional ESD protection scheme and the new proposed ESD protection scheme under power-down-mode operating condition are measured and compared in Fig. 3. The leakage current is measured by applying a voltage ramp from 0 to 3.3 V to the input or output pads under the bias condition of 0-V VDD and 0-V VSS. In Fig. 2, the leakage current at the input (output) pad of the new proposed ESD protection scheme is only 136 pA (206 pA), when a 3.3-V signal is applied to the input (output) pad. On the contrary, the traditional ESD protection scheme has a very high leakage current of up to several mA when the input

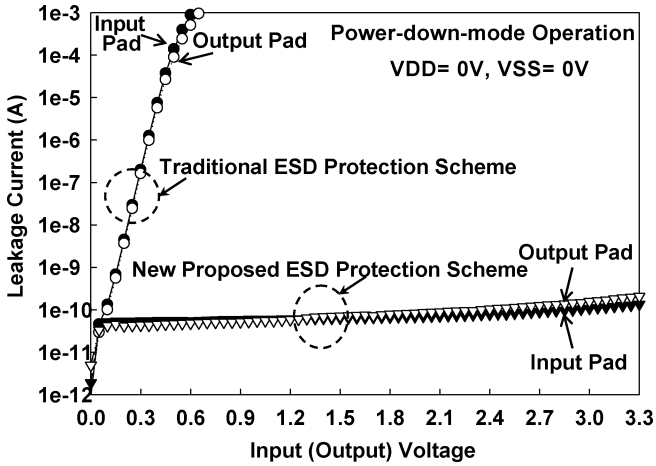

Fig. 3. Comparison of the leakage currents on the input/output pads with the new proposed ESD protection scheme or the traditional ESD protection scheme under power-down-mode operating condition.

or output voltage is only increased to 0.7 V. The leakage current in the new proposed ESD protection scheme has been successfully blocked by the diode of D1 or D2. The experimental results have verified that the new proposed ESD protection scheme can avoid the leakage current from the I/O pin to VDD power line under the power-down-mode operating condition.

C. Function Verification

The measurement setup to verify the function of I/O cells with the new proposed ESD protection scheme, or the traditional ESD protection scheme, under power-down-mode operating condition is shown in Fig. 4(a). A 0-to-3.3-V voltage pulse with a rise time of 20 ns is applied to the input pad under the power-down-mode condition of 0-V VSS but VDD is floating. The voltage waveforms on the input/output pads of the I/O cells with the traditional ESD protection scheme and the new proposed ESD protection scheme under power-down-mode operating condition are shown in Figs. 4(b) and (c), respectively. With the traditional ESD protection scheme, the voltage waveform on the output pad is dropped to a voltage level of $\sim$1.4 V, when the input voltage level is 0 V, as that shown in Fig. 4(b). It implies that the internal circuits are triggered by the input

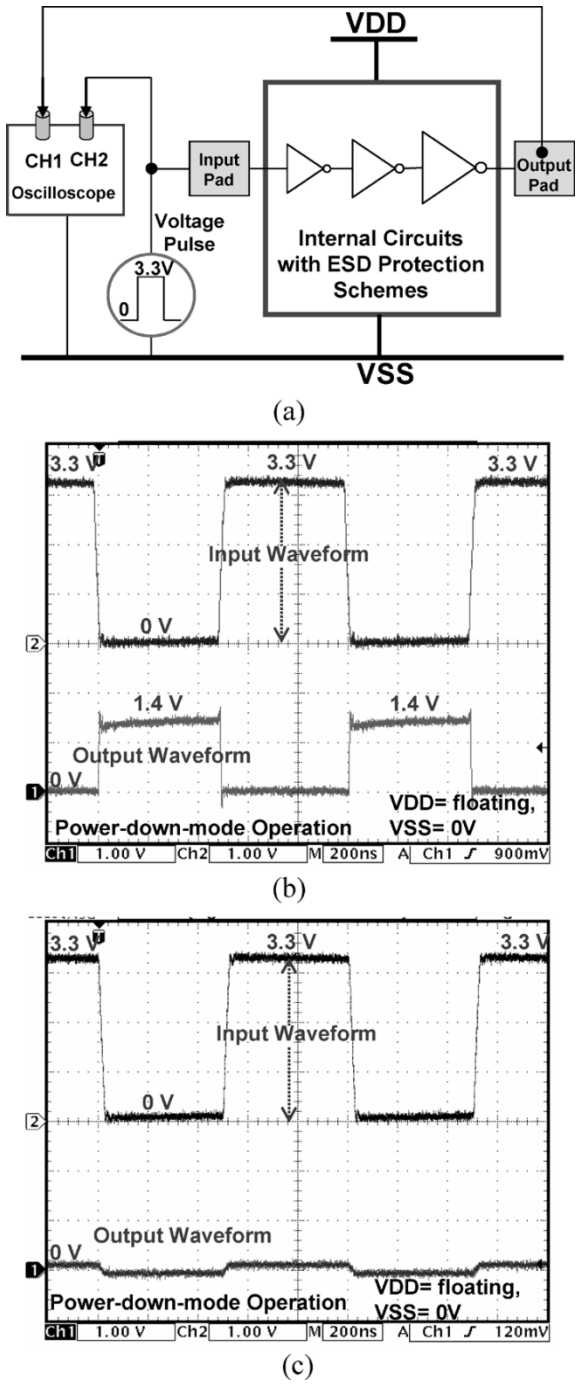

Fig. 4. (a) The measurement setup to verify the ESD protection scheme for IC with power-down-mode operation. The measured voltage waveforms on the input/output pads of IC with (b) the traditional ESD protection scheme, and (c) the new proposed ESD protection scheme, under power-down-mode operating condition with $\mathrm{VDD} = \mathrm{floating}$ and $\mathrm{VSS} = 0\ \mathrm{V}$. ($Y$ axis $= 1\ \mathrm{V/Div.}$, X axis $= 200\ \mathrm{ns/Div.}$).

voltage waveform under power-down-mode operating condition, although the circuits are expected to be off. With the wrong voltage waveform at the I/O pads, the system could be malfunction. However, with the new proposed ESD protection scheme, the voltage level on the output pad is always kept at ~0 V, as that shown in Fig. 4(c). It implies that the internal circuits can be really turned off by the new proposed ESD protection scheme under power-down-mode operating condition.

TABLE I
HBM ESD ROBUSTNESS OF THE TRADITIONAL ESD PROTECTION SCHEME AND THE NEW PROPOSED ESD PROTECTION SCHEME REALIZED IN A 0.35-μm SILICIDED CMOS PROCESS

ESD Protection Scheme \ HBM ESD Stress	PS-Mode VSS(+)	NS-Mode VSS(-)	PD-Mode VDD(+)	ND-Mode VDD(-)	VDD-to-VSS(+)	VDD-to-VSS(-)
Traditional Scheme (Input Pin)	7.5kV	>8kV	>8kV	5kV	5kV	>8kV
Traditional Scheme (Output Pin)	7.5kV	>8kV	>8kV	5kV		
New Proposed Scheme (Input Pin)	7.5kV	>8kV	7.5kV	>8kV	>8kV	>8kV
New Proposed Scheme (Output Pin)	>8kV	>8kV	>8kV	>8kV		

D. ESD Robustness

The human-body-model (HBM) ESD robustness of I/O pads with the traditional or new proposed ESD protection schemes under different pin combinations is listed in Table I. The failure criterion is defined as the leakage current of the circuits after ESD zapping is greater than 1 μA under the normal operating voltage of 3.3 V. With the traditional ESD protection scheme, the ESD level of the I/O pads is 5 kV, which is dominated by the I/O pad under the ND-mode ESD stress or positive VDD-to-VSS ESD stress. However, with the new proposed ESD protection scheme, the ESD levels of the input pad under the PS- and PD-mode ESD stresses are 7.5 kV, whereas the ESD levels of the output pad under all modes of ESD stresses are over 8 kV. The ESD level of I/O pad under the ND-mode ESD stress or VDD-to-VSS ESD stress is improved by the extra ESD current path in the new proposed ESD protection scheme, which is discharged through the diode D1 and ESD clamp circuit between the VDD ESD bus line and VSS power line. As a result, ESD level of the whole chip can be efficiently improved by the new proposed ESD protection scheme for IC with power-down-mode operation.

IV. CONCLUSION

The new ESD protection scheme for IC with power-down-mode operation has been successfully designed and verified in a 0.35-μm silicided CMOS process. Under the power-down-mode operating condition, the new proposed ESD protection scheme can provide the I/O pad without leakage path, and avoid triggering the internal circuits those should be off. High ESD robustness has been practically achieved in the testchip by the new proposed ESD protection scheme to sustain HBM ESD stress of up to 7.5 kV in a 0.35-μm silicided CMOS process.

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