N-Type Schottky Barrier Source/Drain MOSFET Using Ytterbium Silicide

Shiyang Zhu, *Member, IEEE*, Jingde Chen, M.-F. Li, *Senior Member, IEEE*, S. J. Lee, *Member, IEEE*, Jagar Singh, C. X. Zhu, *Member, IEEE*, Anyan Du, C. H. Tung, *Senior Member, IEEE*, Albert Chin, *Senior Member, IEEE*, and D. L. Kwong, *Senior Member, IEEE*

***Abstract*—Ytterbium silicide, for the first time, was used to form the Schottky barrier source/drain (S/D) of N-channel MOSFETs. The device fabrication was performed at low temperature, wich is highly preferred in the establishment of Schottky barrier S/D transistor (SSDT) technology, including the HfO_2 gate dielectric, and HaN/TaN metal gate. The $YbSi_{2-x}$ silicided N-SSDT has demonstrated a very promising characteristic with a recorded high I_{on}/I_{off} ratio of $\sim 10^7$ and a steep subthreshold slope of 75 mV/dec, which is attributed to the lower electron barrier height and better film morphology of the $YbSi_{2-x}$/Si contact compared with other self-aligned rare earth metal-(Erbium, Terbium, Dysprosium) silicided Schottky junctions.**

***Index Terms*—MOSFET, rare earth (RE) metal, Schottky, silicide.**

I. Introduction

THE SCHOTTKY barrier source/drain transistor (SSDT) architecture [1] has been proposed to overcome the series resistance problem of ultrashallow S/D junction of sub50–nm MOSFETs [2]–[4], due to the abrupt silicide/Si interface and low resistance of silicide. The barrier height of the Schottky junction should be low enough to obtain a high-driving current [5] and to prevent two different slopes in the subthreshold region of the MOSFETs [4], [6]. P-channel SSDT (P-SSDT) with PtSi as Schottky S/D (hole barrier $\Phi_p = 0.24$–0.28 eV) has been fabricated with quite acceptable electrical performance with I_{on}/I_{off} ratio of $\sim 10^8$ [6], [7] and one subthreshold slope of 66 mV/dec [6]. However, the electrical performance of N-channel SSDT (N-SSDT) is still inferior mainly due to lack of suitable silicide material [4]–[6]. Erbium silicide has been widely adopted for N-SSDT, but its relatively high electron barrier height and poor film morphology formed by solid-state reaction of deposited Er and substrate Si do not meet the device performance criteria. The I_{on}/I_{off} ratio of the recently reported N-SSDT with $ErSi_{2-x}$ is about 10^5 [8]. On the other hand, the log I_d versus V_g curve shows two slopes at the subthreshold region for long-channel devices [4], [6]. $DySi_{2-x}$ was reported recently [6]. However, it has the similar problems as that of Erbium silicide.

It is well known that the low work function metals usually have low Schottky electron barrier height [9]. Yb has lower photoelectric work function (2.59 eV) than Er (3.12 eV) and Dy (3.09 eV) [1], therefore, Yb silicide is expected to have a lower Schottky electron barrier height. This is the motivation for Yb silicide to be used for N-SSDT and eventually can lead to an excellent electrical device performance.

II. MOS Device Fabrication

A simplified low-temperature process, which has been described in our previous paper [6], [10] was used to fabricate N-SSDT with HfO_2 gate oxide and HfN/TaN metal gate. Starting substrates were p-type Si(100) wafers with resistivity of 4–8 Ω·cm. HfO_2 (4–6 nm) was deposited at 400 °C using $Hf[OC(CH_3)_3]_4$ and O_2 in a metal–organic CVD(MOCVD) system, followed by an *in situ* annealing in N_2 ambient at 700 °C. Then HfN (∼50 nm) and TaN (∼100 nm) were deposited sequentially in a sputtering system with a base pressure of $\sim 1.5 \times 10^{-7}$ torr. Wafers were patterned and subsequently etched using the standard photolithograph and dry etch processes. Immediately after the diluted hydrogen fluoride (DHF) solution dipping, the patterned wafer was loaded into the sputtering system again. Yb (or other RE metal: Er, Dy, Tb) (∼100 nm) and HfN (∼100 nm) were deposited in sequence. HfN was used as a capping layer to prevent RE metal oxidization during *ex situ* annealing. Silicidation was performed by rapid thermal anneal (RTA) at 600 °C for 1 min in N_2 ambient, followed by forming-gas anneal (FGA) at 420 °C for 1 h. The silicidation can be performed by only a FGA step, while the $YbSi_{2-x}$ film morphology is improved by the RTA step. The HfN capping layer and unreacted RE metal were selectively removed by wet etch in DHF (HF: $H_2O = 1 : 100$) and sulphuric-acid hydrogen peroxide mixed (SPM) solution ($H_2SO_4 : H_2O_2 = 3 : 1$ at 120 °C) sequentially. The square sheet resistance of $YbSi_{2-x}$ is ∼3.8 Ω/sq. and the thickness is ∼90 nm [measured by

Manuscript received April 14, 2004; revised May 11, 2004. The review of this letter was arranged by Editor C.-P. Chang.

S. Zhu is with the Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260 (e-mail: elelimf@nus.edu.sg). He is also with the Department of Microelectronics, Fudan University, Shanghai 200433, China.

J. Chen, S. J. Lee, and C. X. Zhu are with the Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260.

M.-F. Li is with the Silicon Nano Device Laboratory, Department of Electrical and Computer Engineering, National University of Singapore, Singapore 119260 and also with the Institute of Microelectronics, Singapore 117685.

J. Singh, A. Du, and C. H. Tung are with the Institute of Microelectronics, Singapore 117685.

A. Chin is with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu 300 Taiwan.

D. L. Kwong is with the Department of Electrical and Computer Engineering, The University of Texas, Austin, TX 78712 USA.

Digital Object Identifier 10.1109/LED.2004.831582

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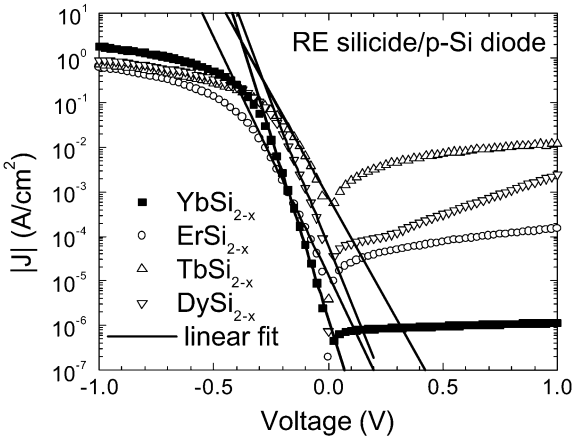

Fig. 1. Room-temperature *I–V* curves of various RE silicide/p-Si(100) diodes and the linear fitting based on the thermal emission model. The deduced barrier heights and ideality factors are summarized in Table I.

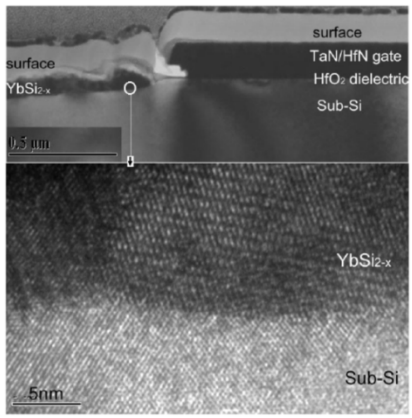

Fig. 2. (Top) XTEM image of the final N-SSDT fabricated by the simplified one-mask process and a "hole" between the S/D and the gate acts as a sidewall spacer [10], and (bottom) a high resolution XTEM image of the polycrystalline $YbSi_{2-x}$/Si(100) contact. Even though the quite rough $YbSi_{2-x}$ surface, which is probably affected by the SPM solution during the selectively etching step, the polycrystalline $YbSi_{2-x}$/Si interface is quite smooth and flat.

cross-sectional transmission electron microscopy (XTEM)], the resistivity of $YbSi_{2-x}$ is calculated to be $\sim 34\ \mu\Omega\cdot$cm.

III. Results and Discussion

Fig. 1 shows current–voltage (*I–V*) curves of various RE silicide/p-Si(100) Schottky diodes. The Schottky hole barrier height (Φ_P^{I-V}) and the ideality factor were deduced by linear fitting based on the thermal emission model [9]. The values are summarized in Table I. The hole barrier heights (Φ_P^{C-V}) deduced from capacitance–voltage (*C–V*) curves are also given. The $YbSi_{2-x}$/p-Si contact has the highest hole barrier height of 0.85 eV, lowest reverse bias leakage current, and the best rectifying property with near unity ideality factor. Other diodes have significantly higher leakage current at reverse bias, larger than unity ideality factors and larger difference between Φ_P^{I-V} and $\Phi_{\rm P}^{C-V}$, implying the unnegligible barrier height inhomogeneity [11]. Observing in the microscope, the surfaces of $ErSi_{2-x}$ and $DySi_{2-x}$ contain many square pits with micrometer size. While there are no such pits on the surface of $YbSi_{2-x}$ and $TbSi_{2-x}$ even though their surface roughness is still quite large as measured by atomic force microscopy. Fig. 2 (top) shows the cross-sectional XTEM image of the final N-SSDT fabricated by our simplified one-mask process.

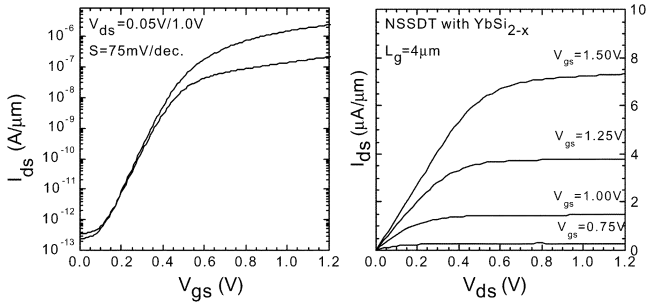

Fig. 3. I_d–V_d and I_d-V_g curves of N-SSDT with $YbSi_{2-x}$ S/D. The channel width and length are 400 and 4 μm respectively. Equivalent oxide thickness of HfO_2 is 2.5 nm as deduced from *C–V* and $V_{\rm th} = 0.40$ V.

TABLE I
Electrical Characteristics of Various RE Silicide/p-Si(100) Contacts Formed by Solid-State Reaction and the Corresponding NSSDT Properties. Barrier Heights Deduced From *C–V* Have Relatively Large Deviation. Data of PtSi/n-Si and P-SSDT [6] Are Also Included for Comparison

Silicide/p-Si (100) diode	$ErSi_{2-x}$	$TbSi_{2-x}$	$DySi_{2-x}$	**$YbSi_{2-x}$**	*PtSi Silicide on n-Si(100)*
Hole barrier obtained by the I-V measurement Φ_p^{I-V} (eV)	0.71	0.60	0.67	**0.82**	*0.84 (electron barrier Φ_n^{I-V})*
Ideality factor in I-V	1.57	1.83	1.33	**1.04**	*1.02*
Hole Barrier obtained by C-V measurement Φ_p^{C-V} (eV)	~ 0.78	~ 0.87	~ 0.83	**~ 0.88**	*~0.86 (electron barrier Φ_n^{C-V})*
Averaged hole barrier $\Phi_p \equiv (\Phi_p^{I-V} + \Phi_p^{I-V})/2$ (eV)	0.75 (1)	0.74	0.75 (2)	**0.85**	*0.85 (electron barrier Φ_n)*
Electron Barrier $\Phi_n \equiv 1.12$ eV - Φ_p (eV) (3)	0.37	0.38	0.37	**0.27**	*0.27 (hole barrier Φ_p)*
$I_{leakage}$ @ 1V (A/cm^2)	1.5×10^{-4}	1.2×10^{-2}	2.3×10^{-3}	**1.1×10^{-6}**	*4.6×10^{-7} @-1V*
SSDT properties: I_{on}/I_{off} ratio	10^3~10^4	10^3~10^4	10^4~10^5	**~10^7**	*~10^9*
I_{ds} @ $\lvert V_{ds}\rvert = V_{gs}-V_{th} = 1$V ($\mu$A/$\mu$m) ($L_g = 4$ μm)	~ 1.4	~ 0.26	~ 2.5	**~ 3.4**	*~3.2*

(1) Compared to the reported value of *0.71 eV* for the $ErSi_{2-x}$ film from I-V [15] and *0.85 eV* from C-V [20]

(2) Compared to the reported value of *0.74 eV* for the $DySi_{2-x}$ film formed by UHV evaporation [18]

(3) Due to the difficulty to measure a low electron Schottky barrier height Φ_n directly, the high hole barrier height Φ_p is measured and the electron barrier height is calculated according to the approximation of $\Phi_n + \Phi_p \cong E_g$ (silicon bandgap).

Fig. 3 shows the I_d–V_d and I_d–V_g curves of N-SSDT with $YbSi_{2-x}$. The $I_{\rm on}/I_{\rm off}$ ratio reaches $\sim 10^7$ with one subthreshold slope of ~ 75 mV/dec, and its drivability is slightly larger than the corresponding P-SSDT with PtSi with the same device structure (Table I). To our knowledge, this is the best electrical performance for N-SSDT reported so far. For comparison, Fig. 4 shows the transfer characteristics of N-SSDT with the same device structure and technology, however using

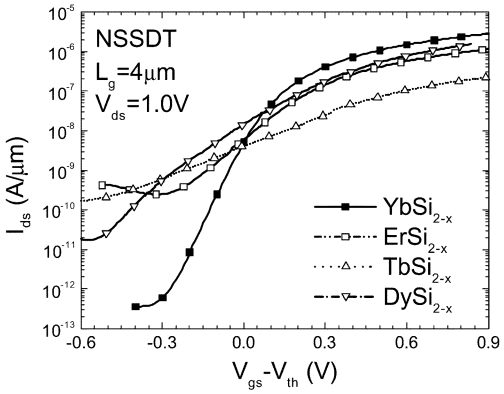

Fig. 4. Transfer characteristics of N-SSDTs with various RE silicides. All devices have the same size of $W/L = 400\ \mu$m/4 μm, and were fabricated by the same process.

$ErSi_{2-x}$, $TbSi_{2-x}$ and $DySi_{2-x}$, respectively. The electrical results of these devices are summarized in Table I.

Besides the low electron barrier height, $YbSi_{2-x}$ has better film quality than other RE silicides. The growth of $ErSi_{2-x}$ or $DySi_{2-x}$ during solid-state reaction of deposited RE metal and substrate Si (100) is strongly nucleation preferred, resulting in a nonuniform, columnar growth of the layer with rough surface and interface [12], [13]. The formed silicide has been reported to be $ErSi_{1.7}$ or $DySi_{1.7}$ due to the Si vacancy in the silicide film [4]. In the case of $YbSi_{2-x}$, the formed silicide has been reported to be $YbSi_{1.8}$ [14]. Our x-ray diffraction and energy dispersive X-ray analysis (not shown here) also confirm that the formed film is $YbSi_{1.8}$. Less Si vacancy may cause the silicide more uniformly. From Fig. 2, the grain size of the polycrystalline $YbSi_{1.8}$ is about 5–10 nm and the grain growths approximately along Si[110] axis. Columnar growth, as in the cases of $ErSi_{2-x}$ and $DySi_{2-x}$, was not found.

The RE silicide property is sensitive to the oxygen contamination. For $ErSi_{2-x}$ silicide, $\Phi_N = 0.28$ eV when grown in ultrahigh-vacuum (UHV) condition [15], however Φ_N becomes higher when grown in normal vacuum level as reported in this work and other paper [16], [17]. Our result shows that $YbSi_{2-x}$ grown in normal vacuum condition has better rectifying characteristics than $ErSi_{2-x}$ grown in UHV condition. It implies that $YbSi_{2-x}$ is not so sensitive to oxygen as $ErSi_{2-x}$, or even better rectifying property of $YbSi_{2-x}$/Si contact may be obtained if it is grown in UHV condition. Very low barrier height (0.08 eV) of metal/n-Si contacts has been reported recently by surface passivation of a thin Se layer [18]. However, such method is infeasible for N-SSDT fabrication due to the requirement of self-aligned S/D formation.

IV. Conclusion

Several rare earth metals are investigated for silicide S/D. The $YbSi_{2-x}$ has been found to be a very promising candidate for N-SSDT as it provides a high drive current with a very low leakage current. It is probably due to the low electron barrier height of the $YbSi_{2-x}$/Si Schottky contact and smooth $YbSi_{2-x}$/Si interface. It can be concluded that $YbSi_{2-x}$ is a much better silicide material than the usually used $ErSi_{2-x}$ for N-SSDT.

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