IOPscience iopscience.iop.org

Home Search Collections Journals About Contact us My IOPscience

A unified quantum correction model for nanoscale single- and double-gate MOSFETs under inversion conditions

This content has been downloaded from IOPscience. Please scroll down to see the full text.

2004 Nanotechnology 15 1009

(http://iopscience.iop.org/0957-4484/15/8/026)

View the table of contents for this issue, or go to the journal homepage for more

Download details:

IP Address: 140.113.38.11
This content was downloaded on 27/04/2014 at 23:56

Please note that terms and conditions apply.

Nanotechnology **15** (2004) 1009–1016 PII: S0957-4484(04)75302-7

A unified quantum correction model for nanoscale single- and double-gate MOSFETs under inversion conditions

Yiming Li[1,2,4] **and Shao-Ming Yu**[3]

[1] Department of Computational Nanoelectronics, National Nano Device Laboratories, Hsinchu 300, Taiwan

[2] Microelectronics and Information Systems Research Center, National Chiao Tung University, Hsinchu 300, Taiwan

[3] Department of Computer and Information Science, National Chiao Tung University, Hsinchu 300, Taiwan

E-mail: ymli@mail.nctu.edu.tw

Received 16 January 2004
Published 18 June 2004
Online at stacks.iop.org/Nano/15/1009
doi:10.1088/0957-4484/15/8/026

Abstract

In this paper a unified quantum correction charge model for nanoscale single- and double-gate MOS structures is presented. Based on the numerical solution of Schrödinger–Poisson equations, the developed quantum correction charge model is mainly optimized with respect to (i) the left and right positions of the charge concentration peak, (ii) the maximum of the charge concentration, (iii) the total inversion charge sheet density, and (iv) the average inversion charge depth, respectively. For nanoscale single- and double-gate MOS structures, this model predicts inversion layer electron density for various oxide thicknesses, silicon film thicknesses, and applied voltages. Compared to the Schrödinger–Poisson results, our model prediction is within 2.5% of accuracy for both the single- and double gate MOS structures on average. This quantum correction model has continuous derivatives and is therefore amenable to a device simulator.

1. Introduction

The study of nanoscale single- and double-gate (SG and DG) MOSFETs has been of great interest in recent years [1–11]. As the dimensions of MOSFETs are aggressively scaled into the nanoscale regime, it is quite necessary to take the quantum mechanical effects into consideration in device modelling and simulation. Various approaches have been proposed to investigate the device's quantization effects in the inversion conditions [1, 4, 12–22]. For an oxide thickness (T_{ox}) of 1–3 nm, a silicon film thickness (T_{si}) of 5–100 nm, and an applied gate voltage (V_G) of 0.5–1.5 V, the inversion carrier density shifts away from the interfaces of SiO_2/Si due to the quantization effect [12]. The Schrödinger–Poisson (SP) equations subject to an appropriate boundary condition at the Si/SiO_2 interfaces have been applied to study such a quantum effect [13–15], but it is a time-consuming task in realistic device simulation and characterization.

In this paper, we have successfully developed a unified quantum correction model feasible for nanoscale SG and symmetric and asymmetric DG (SDG and ADG) MOSFETs simulation simultaneously. This unified model for both the SG and DG MOS structures is a generalization of the analytical model proposed by us [16] recently. The numerical solution of SP equations is utilized to construct the model, where there are four physically based optimization constraints: (i) the left and right positions of the charge concentration peak, (ii) the maximum of the charge concentration, (iii) the total inversion charge sheet density, and (iv) the average inversion charge depth; these are considered as criteria for the parameter formulation. All parameters of the unified model are expressed as a function of T_{ox}, T_{si}, and V_G. For a 2D nanodevice simulation, they can also be in terms of T_{ox}, T_{si}, and surface electric field E_s. The developed model is

[4] Author to whom any correspondence should be addressed.

© 2004 IOP Publishing Ltd Printed in the UK

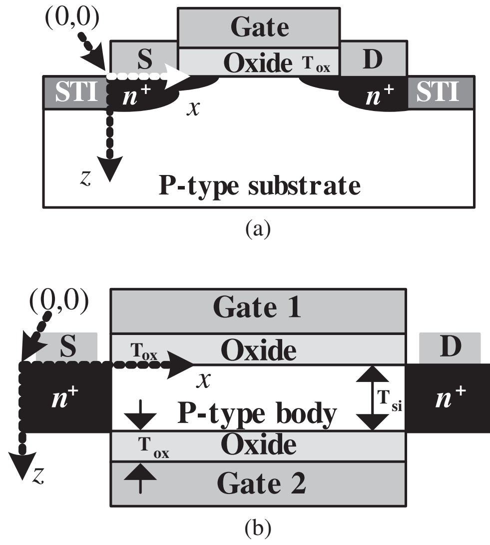

Figure 1. Cross-section views of the nanoscale (a) single-gate MOSFET and (b) double-gate MOSFETs.

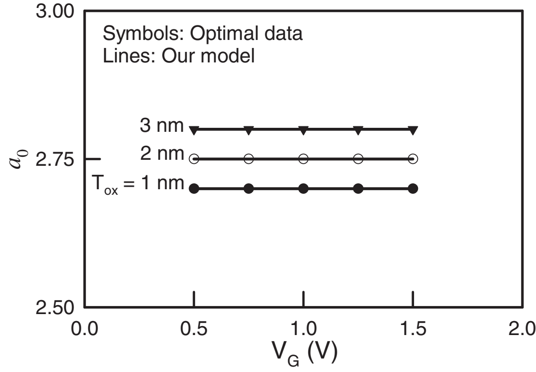

Figure 2. Plot of the optimal value for the parameter a_0 and its formula for the SG MOS structure with different T_{ox} and V_G.

firstly compared with four well established quantum correction models, i.e., the Hänsch model [17], the modified local density approximation (MLDA) model [18], the density gradient (DG) model [14, 19, 20], and the effective potential (EP) model [21], in terms of accuracy for predicting the inversion layer charge distribution of the SG and DG MOS structures. Application of this charge quantization model to the C–V measurement of an ultra-thin oxide MOSFET produces an excellent agreement. We have also applied it to the simulation of a 20 nm SDG MOSFET's I–V curves with a hydrodynamic (HD) device simulator.

This paper is organized as follows. Section 2 introduces the model formulation. Section 3 describes the calculated results illustrating the preliminary model accuracy and different simulation cases. Section 4 draws the conclusions.

2. A unified quantum correction model

As shown in figure 1, poly–oxide–silicon (figure 1(a)) and poly–oxide–silicon–oxide–poly (figure 1(b)) are simulated [15, 16, 22]. The coupled Schrödinger and Poisson equations are solved self-consistently along the longitudinal z-direction under the gate. First of all the Poisson equation

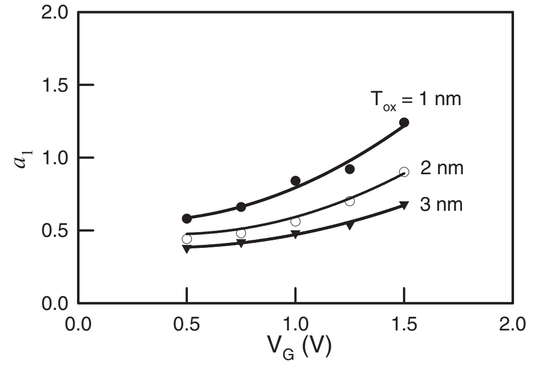

Figure 3. Plot of the optimal value for the parameter a_1 and its formula for the SG MOS structure with different T_{ox} and V_G.

is solved to obtain the potential distribution. It is then used in the solution of the Schrödinger equation. With the two-dimensional electron gas formula [23, 24], the charge density can be calculated with the solved wavefunctions and energy levels from the Schrödinger equation. Once the new charge density is obtained, it is plugged into the Poisson equation to solve the new potential. The potential is then updated and the Schrödinger equation is solved again. These steps are repeated iteratively until the convergence criterion is reached [13–15]. For simplicity in the model construction, the SP equations considered here are only assumed to have no wave penetration at the Si/SiO_2 interface [13–15]. The SP equations are discretized by the finite difference method (the so-called box method). After the discretization, the corresponding matrix eigenvalue problem and the system of nonlinear algebraic equations are solved iteratively to obtain a self-consistent solution [13–15]. More than 32 sub-bands are calculated in the Schrödinger equation solver. For the DG MOS structures, the chosen T_{ox} varies from 1 to 3 nm, T_{si} varies from 5 to 100 nm, and the applied V_G ranges from 0.5 to 1.5 V [1–11]. For the SG MOS structures under inversion we consider the electron density from the interface of SiO_2/Si to silicon bulk completely. For both the SDG and ADG MOS structures, it is sufficient to consider the modelling from the left (or right) interface of SiO_2/Si to $T_{si}/2$. The proposed explicit formula of the calculated inversion-layer charge densities for both the SG and DG MOS structures are

$$n_{QM} = a_0 n_{\mathrm{CL}}\left(1 - \exp\left(-a_1\xi^2\left(1 - \frac{1}{2}\left(\frac{\xi}{\xi_0}\right)^2\right) - a_2\xi^3\right)\right), \tag{1}$$

where n_{CL} is the classical electron density solved from the Poisson equation. $\xi = z/\lambda_{\mathrm{th}}$ and $\lambda_{\mathrm{th}} = \left(\frac{\hbar^2}{2m_0 k_{\mathrm{B}} T}\right)^{1/2}$ is the thermal wavelength, $\hbar$ is the reduced Planck constant, m_0 is the electron rest mass, k_{B} is the Boltzmann constant, and T is the absolute temperature. For the SG MOS structure, ξ_0 is chosen to be the bulk thickness. Physically, the bulk thickness is at infinity where the gradient of potential vanishes. The potential is calculated with the classical Poisson equation. Numerically, it is effectively taken far enough so that it does not significantly affect the results. For example, the bulk thickness used in our modelling and simulation is taken as 100 nm. $\xi_0 = T_{si}/2\lambda_{\mathrm{th}}$ is for both the SDG and ADG MOS structures. The mathematical derivation of (1) is based on an approximate solution of the Schrödinger equation as well as the two-dimensional electron

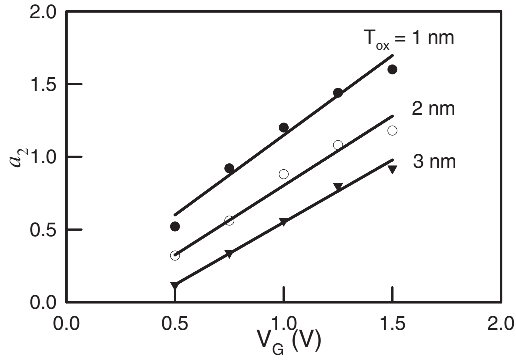

Figure 4. Plot of the optimal value for the parameter a_2 and its formula for the SG MOS structure with different T_{ox} and V_G.

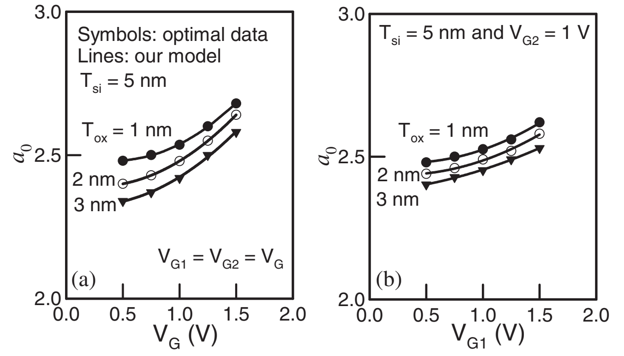

Figure 5. Plot of the optimal value for the parameter a_0 and its formula for the (a) SDG and (b) ADG MOS structures with different T_{ox} and V_G, where V_{G2} is fixed at 1 V for the case of ADG.

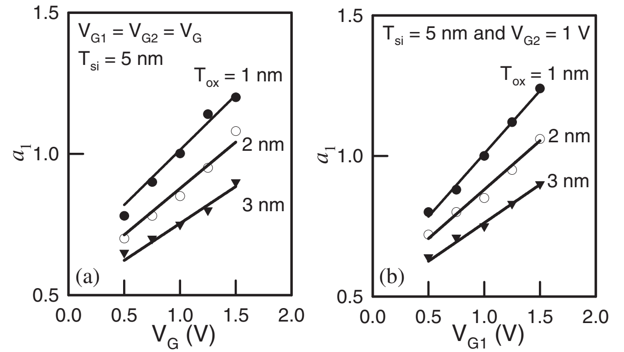

Figure 6. Plot of the optimal value for the parameter a_1 and its formula for the (a) SDG and (b) ADG MOS structures with different T_{ox} and V_G, where V_{G2} is fixed at 1 V for the case of ADG.

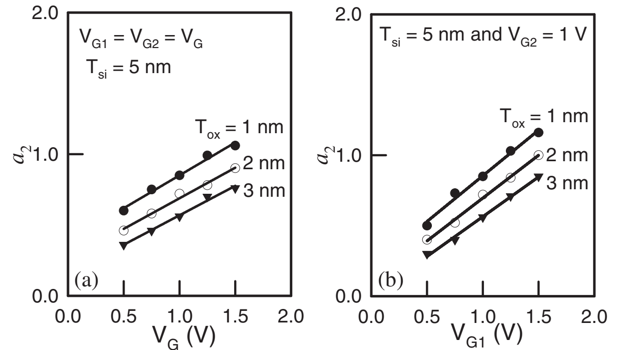

Figure 7. Plot of the optimal value for the parameter a_2 and its formula for the (a) SDG and (b) ADG MOS structures with different T_{ox} and V_G, where V_{G2} is fixed at 1 V for the case of ADG.

gas formulation for the electron density near the interfaces of SiO_2/Si [17, 23, 24]. Using a generic algorithm [25], the three model parameters a_0, a_1, and a_2 are systematically optimized to best fit the self-consistent SP solution with respect to the values of T_{ox}, T_{si}, and V_G for both the SG and DG MOS structures. The model accuracy of these parameters is based on the optimization with respect to the aforementioned four constraints. The average inversion charge depth is defined as $\langle z\rangle = \int_0^{T_{si}} zn(z)\,dz / \int_0^{T_{si}} n(z)\,dz$.

The results of these parameters for the SG MOS structures are shown in figures 2–4. As seen in figure 2, the plots of a_0 versus V_G are horizontal lines and are independent of V_G. Figure 3 shows that the dependence of the a_1 on V_G for different T_{ox} is similar; all have a positive slope when $V_G \geqslant 0.2T_{ox}$. Shown in figure 4 are plots of a_2 versus V_G, all having a positive slope when $T_{ox} \leqslant 10$ nm. For a fixed V_G, we note that a_1 and a_2 decrease as T_{ox} increases. Similarly, figures 5–7 show the results of these parameters for the SDG and ADG MOS structures with $T_{si} = 5$ nm for example. As seen in figure 5, the plots of a_0 versus V_G are quadric functions of V_{G1} and V_{G2}. It is found that a_0 is independent of T_{si} when T_{si} approaches infinity. Figure 6 shows that the dependence of the a_1 on V_G for fixed T_{si} and different T_{ox} is similar; all almost have a positive slope. Shown in figure 7 are plots of a_2 versus V_G, all having a positive slope similar to the cases of SG MOS structure shown in figure 4. It is found that a_1 and a_2 depend only on T_{si} and T_{ox} at a very low V_{G1}. Both a_1 and a_2 are independent of T_{si} exponentially when T_{si} approaches infinity. For a fixed V_G, we note that a_0, a_1, and a_2 decrease as T_{ox} is increased.

After optimization, a set of these parameters for the SG MOS structure is expressed as a function of V_G and T_{ox}:

$$a_0 = 2.65 + 0.05T_{ox}, \tag{2}$$

$$a_1 = 0.549 - 0.0152T_{ox} - 0.159T_{ox}V_G + 0.398V_G^2, \tag{3}$$

$$a_2 = 0.252 - 0.172T_{ox} + 1.104V_G - 0.1T_{ox}V_G, \tag{4}$$

where V_G is in volts and T_{ox} is in nanometres. With variables of V_{G1}, V_{G2}, T_{si}, and T_{ox}, the parameters for both the SDG and ADG MOS structures are

$$a_0 = 1.456 + \frac{0.314}{T_{ox}} + \frac{3.980}{T_{si}} - \frac{0.502(V_{G1}+V_{G2})}{T_{ox}T_{si}} + 0.0427(V_{G1}+V_{G2})^2, \tag{5}$$

$$a_1 = 0.087 - 60.881\exp(-T_{si}) + \frac{0.916}{T_{ox}} + 0.909V_{G1} - \frac{102.121\exp(-T_{si})V_{G1}}{T_{ox}} + \frac{0.341V_{G1}^2}{(V_{G1}+V_{G2})}, \tag{6}$$

$$a_2 = 0.011 + 52.041\exp(-T_{si}) - \frac{0.0421}{T_{ox}} - 0.115V_{G1} + \frac{86.036\exp(-T_{si})V_{G1}}{T_{ox}} + \frac{0.244V_{G1}^2}{(V_{G1}+V_{G2})}, \tag{7}$$

where V_{G1} and V_{G2} are in volts, and T_{si} and T_{ox} are in nanometres. The two sets of the model parameters given

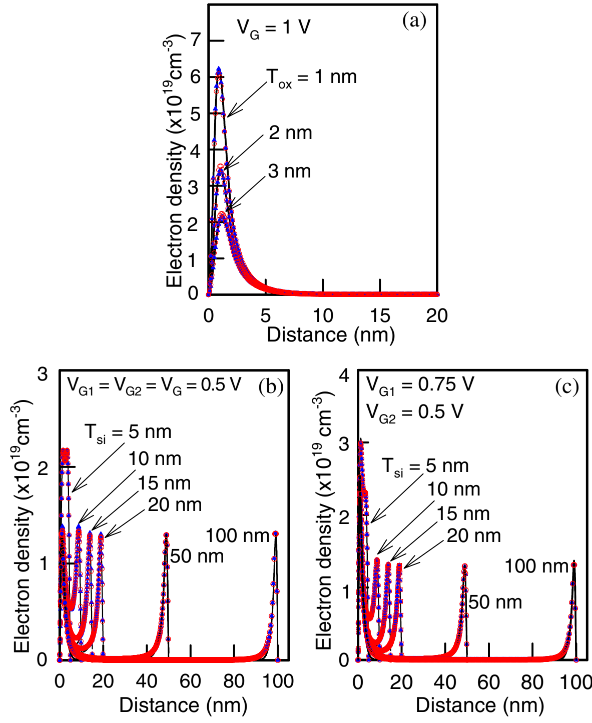

Figure 8. Electron density with the SP (curves) model, the optimal value (triangles), and our model (circles) for the (a) SG, (b) SDG, and (c) ADG MOS structures.

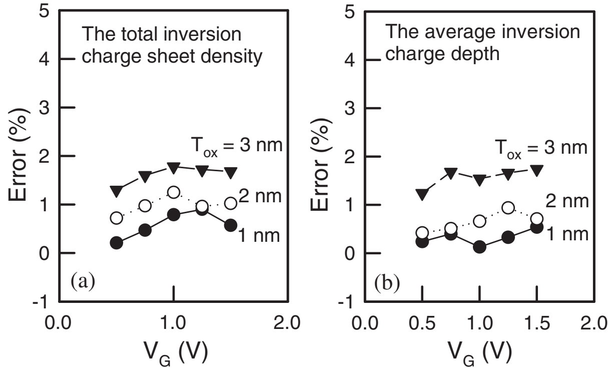

Figure 9. Errors of (a) the total inversion charge sheet density and (b) the average inversion charge depth versus V_G for the case of an SG with different T_{ox}.

in (2)–(4) and (5)–(7) are based on a p-type silicon body with $N_A = 10^{17}$ cm^{-3}. For other doping concentrations, V_G should be adjusted by an amount equal to a shift in the threshold voltage due to the change in N_A. However, this adjustment is usually very small (∼0.1 V). The accuracy of the model inversion-layer charge density given by (1), (2)–(4), and (5)–(7) compared to the SP solution is very good. In terms of the four criteria mentioned above, the accuracy is within 2.5%.

Shown in figures 8(a)–(c) are the electron densities between our results (symbols) and the SP solutions (lines) against distance for the SG, SDG, and ADG MOS structures, respectively. A uniform doping profile with $N_A = 10^{17}$ cm^{-3} is used for the simulations. Shown in figures 9, 10 respectively are the errors between the established a formula and the SP solution against V_G for each optimization criterion in the SG and DG MOS structures. For the SG MOS structure, as shown

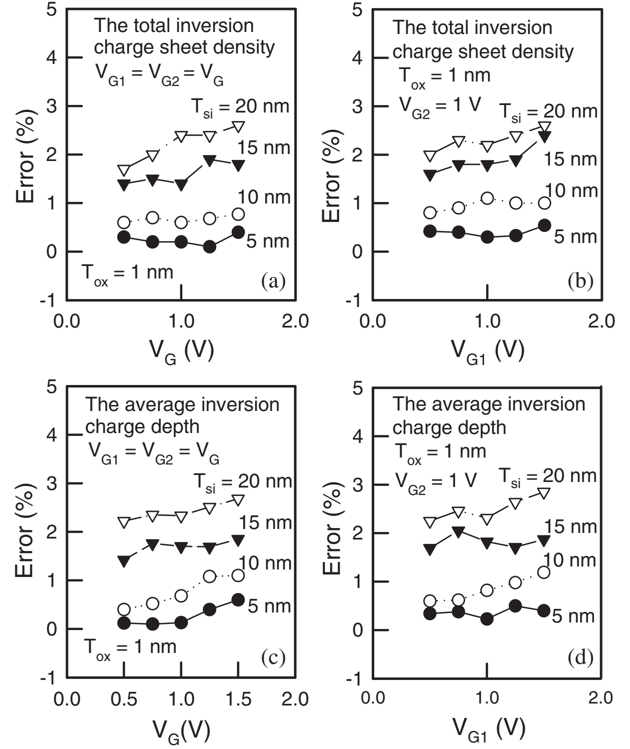

Figure 10. Errors of the total inversion charge sheet density versus V_G for both the (a) SDG and (b) ADG. Errors of the average inversion charge depth versus V_G for both the (c) SDG and (d) ADG with different T_{si}.

in figures 9(a) and (b), the errors of the total inversion charge sheet density and the average inversion charge depth between our model and the SP equation are all less than 1.8%. The error of the position of the charge concentration peak and the error of the maximum of the charge concentration are both less than 1%. For both the SDG and ADG MOS structures, figures 10(a) and (b) show that the error of the total inversion charge sheet density between our model and the SP equation is less than 2.6%. Figures 10(c) and (d) show that the error of the average inversion charge depth is within 2.7%. The error of the left and right positions of the charge concentration peak is less than 2.1%, and the error of the maximum of the charge concentration is less than 1.8%, respectively. For the SG and DG MOS structures with different doping profiles, i.e., Gaussian doping profiles and low-high doping profiles, and concentration N_A varying from 10^{16} to 10^{18} cm^{-3}, the four errors versus V_G are also theoretically estimated with the same a formula. We have found that the error fluctuations are all less than 4.8%, and this maximum error occurred at the SDG MOS structure with the Gaussian doping profiles with $N_A = 10^{16}$ cm^{-3}, $T_{ox} = 3.0$ nm, $T_{si} = 100$ nm and $V_G = 0.5$ V. We have expressed the coefficients a_0, a_1, and a_2 in terms of the surface electric field E_s and the oxide thickness T_{ox} for applications to a two-dimensional (2D) simulation. For the SG MOS structure, the formulae are

$$a_0 = 2.65 + 0.05T_{ox}, \tag{8}$$

$$a_1 = 0.222 + 0.220E_s + 0.0652E_s^2, \tag{9}$$

$$a_2 = -0.5137 + 1.329E_s - 0.212E_s^2, \tag{10}$$

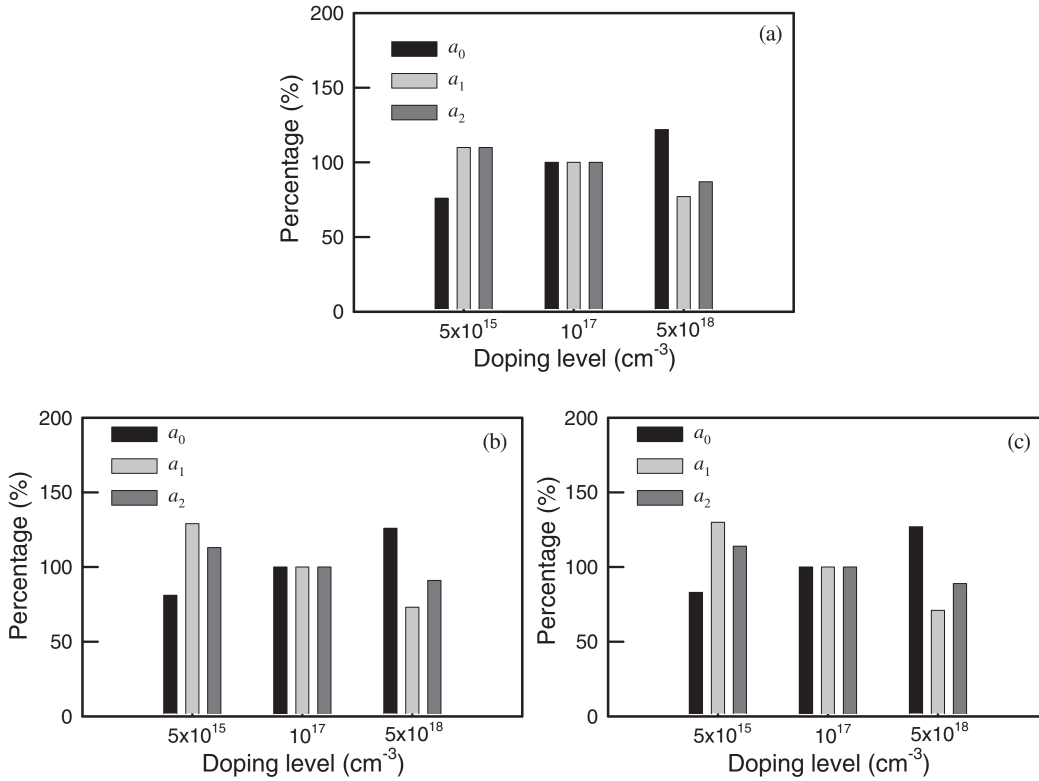

Figure 11. The variation percentage of the modelled parameters a_0, a_1, and a_2 versus the uniform doping level. (a) The result of the SG MOS structure with $V_G = 1.5$ V, $T_{ox} = 1$ nm, (b) the plot of the SDG MOS structure with $V_{G1} = V_{G2} = 1.5$ V, $T_{ox} = 1$ nm, and $T_{si} = 5$ nm, and (c) the plot of the ADG MOS structure with $V_{G1} = 1.5$ V, $V_{G2} = 1.0$ V, and $T_{ox} = 1$ nm.

and for the DG MOS structures the formulae are

$$a_0 = 1.639 + \frac{0.0598}{T_{ox}} + \frac{3.905}{T_{si}} - \frac{0.333(E_{S1} + E_{S2})}{T_{ox}T_{si}} + 0.0202(E_{S1} + E_{S2})^2, \qquad (11)$$

$$a_1 = 0.694 - 81.93\exp(-T_{si}) - \frac{0.256}{T_{ox}} + 0.773E_{S1} - \frac{50.99\exp(-T_{si})E_{S1}}{T_{ox}} + \frac{0.259E_{S1}^2}{E_{S1} + E_{S2}}, \qquad (12)$$

$$a_2 = 0.0247 + 96.02\exp(-T_{si})E_{S1} + \frac{0.0628}{T_{ox}} - 0.148E_{S1} - \frac{28.6\exp(-T_{si})E_{S1}}{T_{ox}} + \frac{0.189E_{S1}^2}{E_{S1} + E_{S2}}, \qquad (13)$$

where T_{ox} is in nm and the E_s in MV cm^{-1} is self-consistently computed with the DD model. If the silicon film thickness of the DG MOS structure becomes very thick, i.e., T_{si} approaches infinity in (5)–(7) and (11)–(13), the models of a are independent of T_{si}.

The model parameters a_0, a_1, and a_2 discussed above are mainly based on the doping level $N_A = 10^{17}$ cm^{-3}. To assess the validity of the proposed model, the variation of the modelled parameters a_0, a_1, and a_2 with respect to the doping level is further examined. For the aforementioned four constraints under the same error criteria above, the variation is calculated for all V_G, T_{ox}, and T_{si}. For both the SG and DG MOS structures with uniform doping profile, the modelled parameter a_0 increases when the doping level varies from 5×10^{15} to 5×10^{18} cm^{-3}. Both the modelled parameters a_1 and a_2 decrease when the doping level changes from 5×10^{15} to 5×10^{18} cm^{-3}. For example, under a set of fixed V_G, T_{ox}, and T_{si}, figures 11(a)–(c) show the variation of the modelled parameters a_0, a_1, and a_2 versus the doping level, respectively. Based on our numerical calculations, it is found that the variation of the three modelled parameters a_0, a_1, and a_2 is within 25% for all V_G, T_{ox}, and T_{si}.

3. Results and discussion

Figures 12(a)–(c) are comparisons of the inversion layer charge distribution for the SG, SDG, and ADG MOS structures among the Hänsch model [17], the MLDA model [18], the EP model [21], the DG model [14, 19, 20], and our model. A uniform doping profile with $N_A = 10^{17}$ cm^{-3} and $T_{ox} = 1$ nm are assumed for the SG and DG MOS structures. $T_{si} =$ 5 nm is for the cases of SDG and ADG. The parameter m_k appearing in the first four well known quantum correction models are optimally determined by calibrating with the SP solutions [22, 26]. More than 32 subbands are calculated in the Schrödinger equation solver. For the SG MOS structure, the optimized m_k is 0.36 m_0 ($m_0 = 9.11 \times 10^{-31}$ kg), 0.41, 0.283, and 1.22 m_0 corresponding to the Hänsch, the MLDA, the EP, and the DG models, respectively. The optimized m_k in the SDG MOS structure is 0.32, 0.45, 0.315, and 1.41 m_0 (similarly, the optimized m_k in the ADG MOS structure is 0.27, 0.41, 0.291, and 1.34 m_0) for the Hänsch, the MLDA, the EP, and the DG models, respectively. Among these simulations we find that the agreement of our result with the SP data is excellent in the prediction of the inversion layer charge distributions. The

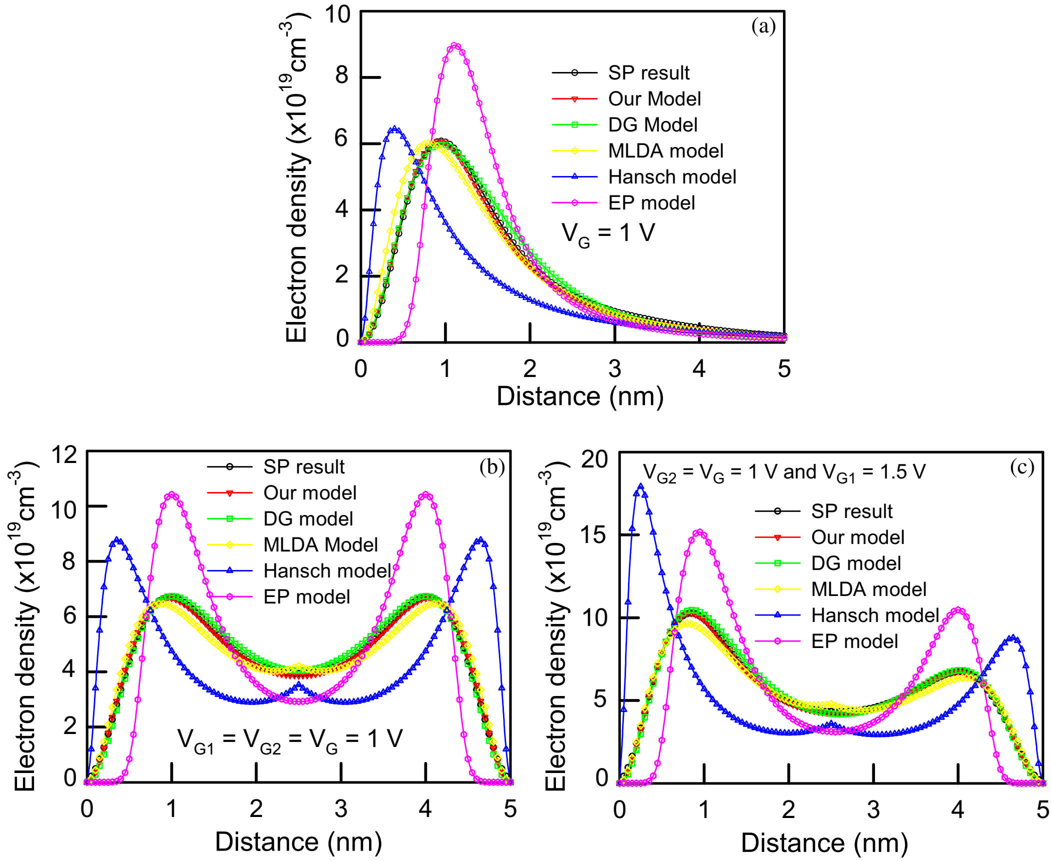

Figure 12. Electron density with different models for the (a) SG, (b) SDG, and (c) ADG MOS structures.

Hänsch and MLDA models are found to have non-physical kinks in the DG MOS simulation which are sensitive to the selection of parameter m_k and depend on T_{si} and V_{G1} and V_{G2}, as seen in figures 12(b) and (c).

As applications, we apply our quantum correction model, equations (1) and (2)–(4), for the inversion charge to the calculation of C–V curves. A 20×20 μm^2 N-MOSFET with $T_{ox} = 1.6$ nm is considered for investigating the C–V curves. The details of the calculation of C–V curves as well as the experimental measurement setting were discussed in [16]. As shown in figure 13, the agreement of our result with the measurement is acceptable except for $V_G \geqslant 1.0$ V. The difference between simulated and measured C–V curves is due to the assumption of zero wavefunction penetration in the SP equations.

Application to a 2D DG MOSFET simulation is performed with the quantum correction model in terms of E_s, T_{ox}, and T_{si}. The drain current (I_{DS}) of the 20 nm SDG N-MOSFET is computed using the conventional HD model together with equations (1) and (11)–(13). The device in our simulation is with $T_{si} = 10$ nm and $T_{ox} = 2$ nm. We assume the source and drain doping concentration $N_D = 10^{20}$ cm^{-3}. The device has a uniform channel doping profile $N_A = 10^{17}$ cm^{-3}. The mobility model is crucial to nanoscale device simulation. In this simulation a field dependent mobility is adopted [11, 27]. However, different surface mobility models lead to different drain current also in the linear region. Therefore, advanced studies and experimental calibration are necessary to enable a sound model for practical nanoscale

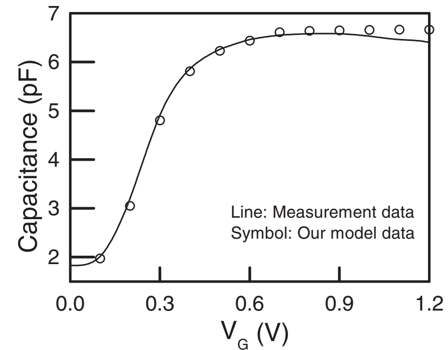

Figure 13. Comparison of C–V curves between our model and the SP model for a 20×20 μm^2 N-MOSFET with $T_{ox} = 1.6$ nm.

MOSFETs simulation. Numerical solution of the 2D classical HD with and without a quantum correction model is achieved by using an adaptive mesh refinement technique [28, 29]. Error estimation is performed on the computed results, and therefore the simulation mesh is refined to locate the sharp variations of electrostatic potential and electron density near the channel surfaces and drain side. Figure 14 shows the computed I_{DS} versus drain voltage (V_{DS}) for the 20 nm SDG MOSFETs at gate voltage $V_{G1} = V_{G2} = 0.7$ V. Due to the overestimation of the current density at both surfaces of the device channel, the classical HD simulation yields higher drain current levels (>40% at $V_{DS} = 1$ V) than the quantum mechanical simulation [30–32]. To verify the validity of our

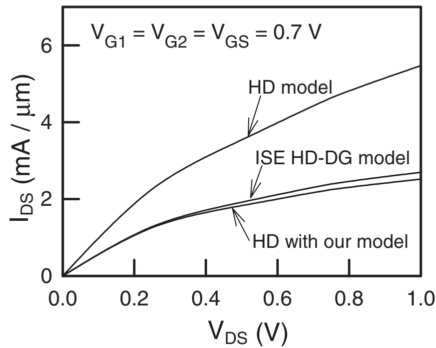

Figure 14. The simulated drain current of the 20 nm SDG N-MOSFET using the classical HD with and without the quantum correction model.

simulation, we have performed the same simulation by using an ISE DESSIS device simulator (version 8.5), where the 2D HD together with the density-gradient (DG) model is simulated. As shown in figure 14, it is found that the result obtained with our proposed model has demonstrated its accuracy in comparison to the results calculated with the HD-DG model. However, for including complete transport phenomena, such as the short channel effect for multi-dimensional application, a set of 2D SP equations should be further considered in the model formulation.

4. Conclusions

We have successfully developed a unified quantum correction model for correcting the classical inversion-layer charge distribution which agrees with the SP solution within 2.5%. By using the classical charge density from the solution of the DD/HD based device simulator, together with the device oxide thickness, silicon film thickness, and gate voltage (or surface electric field), the proposed inversion-layer charge correction model calculates nanoscale single- and double-gate MOSFET inversion charge explicitly, taking into consideration the quantum effect. Comparisons among the four well known quantum correction models suggest that the proposed model is attractive to the modelling of nanoscale MOSFETs. The application of this model to the *C–V* measurement has produced an excellent agreement. Our preliminary 2D HD simulation shows that this inversion-layer charge correction model is computationally cost-effective and amenable to a device simulator for industrial application.

Acknowledgments

This work is supported in part by the National Science Council of TAIWAN under contract No. NSC-92-2112-M-429-001 and by the grant of the Ministry of Economic Affairs, Taiwan under contract No. PSOC 92-EC-17-A-07-S1-0011.

References

[1] Sano N, Hiroki A and Matsuzawa K 2002 Device modeling and simulations toward sub-10 nm semiconductor devices *IEEE Trans. Nanotechnol.* **1** 63–71

[2] Masahara M, Matsukawa T, Ishii K, Liu Y, Tanoue H, Sakamoto K, Sekigawa T, Yamauchi H, Kanemaru S and Suzuki E 2002 15-nm-thick Si channel wall vertical double-gate MOSFET *Tech. Dig. of Int. Electron Devices Mtg. (IEDM'02)* pp 949–51

[3] Yu B *et al* 2002 FinFET scaling to 10 nm gate length *Tech. Dig. of Int. Electron Devices Mtg. (IEDM'02)* pp 251–4

[4] Laux S E, Kumar A and Fischetti M V 2002 QDAME simulation of 7.5 nm double-gate Si nFETs with differing access geometries *Tech. Dig. of Int. Electron Devices Mtg. (IEDM'02)* pp 715–8

[5] Pei G, Kedzierski J, Oldiges P, Ieong M and Kan E C-C 2002 FinFET design considerations based on 3-D simulation and analytical modeling *IEEE Trans. Electron Devices* **49** 1411–9

[6] Schulz T, Rosner W, Landgraf E, Risch L and Langmann U 2002 Planar and vertical double gate concepts *Solid-State Electron.* **46** 985–9

[7] Tang S H, Xuan P, Bokor J and Hu C 2002 Comparison of short-channel effect and offstate leakage in symmetric vs. asymmetric double gate MOSFETs *Proc. IEEE Int. SOI Conf.* pp 120–1

[8] Fossum J G, Ge L and Chiang M H 2002 Speed superiority of scaled double-gate CMOS *IEEE Trans. Electron Devices* **49** 808–11

[9] Song S, Kim H, Yoo J Y, Yi J H, Kim W S, Lee N I, Fujihara K, Kang H-K and Moon J T 2001 On the gate oxide scaling of high performance CMOS transistors *Tech. Dig. of Int. Electron Devices Mtg. (IEDM'01)* pp 3.2.1–4

[10] Mouis M, Genin F-N and Poncet A 2001 Gate control in ultra-short channel double-gate MOSFETs accounting for 2D and quantum confinement effects *Proc. Device Res. Conf.* pp 195–6

[11] Walczak J and Majkusiak B 2001 The remote roughness mobility resulting from the ultrathin SiO_2 thickness nonuniformity in the DG SOI and bulk MOS transistors *Microelectron. Eng.* **59** 417–21

[12] Stern F and Howard W E 1967 Properties of semiconductor surface inversion layers in the electric quantum limit *Phys. Rev.* **163** 816–35

[13] Fiegna C and Abramo A 1997 Solution of 1-D Schrödinger and Poisson equations in single and double gate SOI MOS *Proc. Tech. Dig. of Int. Conf. on Simul. of Semicond. Proc. and Devices SISPAD* pp 93–6

[14] Li Y, Lee J-W, Tang T-W, Chao T-S, Lei T-F and Sze S M 2002 Numerical simulation of quantum effects in high-*k* gate dielectrics MOS structures using quantum mechanical models *Comput. Phys. Commun.* **147** 214–7

[15] Li Y, Chao T-S and Sze S M 2003 A novel parallel approach for quantum effect simulation in semiconductor devices *Int. J. Modelling Simul.* **23** 94–102

[16] Tang T-W and Li Y 2002 A SPICE-compatible model for nanoscale MOSFET capacitor simulation under the inversion condition *IEEE Trans. Nanotechnol.* **1** 243–6

[17] Hänsch W, Vogelsang T, Kircher R and Orlowski M 1989 Carrier transport near the Si/SiO interface of a MOSFET *Solid-State Electron.* **32** 839–49

[18] Paasch G and Ubensee H 1982 A modified local density approximation *Phys. Status Solidi* b **113** 165–78

[19] Ancona M G and Tiersten H F 1987 Macroscopic physics of the silicon inversion layer *Phys. Rev.* B **35** 7959–65

[20] Ancona M G, Yu Z, Dutton R W, Vande Voorde P J, Cao M and Vook D 2000 Density-gradient analysis of MOS tunneling *IEEE Trans. Electron Dev.* **47** 2310–9

[21] Ferry D K, Ramey S, Shifren L and Akis R 2002 The effective potential in device modeling: the good, the bad and the ugly *J. Comput. Electron.* **1** 59–65

[22] Li Y, Tang T-W and Wang X 2002 Modeling of quantum effects for ultrathin oxide MOS structures with an effective potential *IEEE Trans. Nanotechnol.* **1** 238–42

[23] Taur Y and Ning T H 1998 *Fundamentals of Modern VLSI Devices* (New York: Cambridge University Press)

[24] Ando T, Fowler A B and Stern F 1982 Electronics properties of two-dimensional systems *Rev. Mod. Phys.* **54** 437–672

[25] Li Y, Cho Y-Y, Wang C-S and Huang K-Y 2003 A genetic algorithm approach to InGaP/GaAs HBT parameters extraction and RF characterization *Japan. J. Appl. Phys.* 1 **42** 2371–4
[26] Wang X and Tang T-W 2002 Comparison of three quantum correction models for the charge density in MOS inversion layers *J. Comput. Electron.* **1** 283–7
[27] Darwish M N, Lentz J L, Pinto M R, Zeitzoff P M, Krutsick T J and Vuong H H 1997 An improved electron and hole mobility model for general purpose device simulation *IEEE Trans. Electron Devices* **44** 1529–38
[28] Li Y, Sze S M and Chao T-S 2002 A practical implementation of parallel dynamic load balancing for adaptive computing in VLSI device simulation *Eng. Comput.* **18** 124–37
[29] Li Y, Chao T-S and Sze S M 2002 A domain partition approach to parallel adaptive simulation of dynamic threshold voltage MOSFET *Comput. Phys. Commun.* **147** 697–701
[30] Ogawa M, Tsuchiya H and Miyoshi T 2003 Quantum electron transport modeling in nano-scale devices *IEICE Trans. Electron.* **86-C** 363–71
[31] Asenov A, Watling J R, Brown A R and Ferry D K 2002 The use of quantum potentials for confinement and tunnelling in semiconductor devices *J. Comput. Electron.* **1** 503–13
[32] Choi Y-K, Ha D, King T-J and Bokor J 2003 Investigation of gate-induced drain leakage (GIDL) current in thin body devices: single-gate ultra-thin body, symmetrical double-gate, and asymmetrical double-gate MOSFETs *Japan. J. Appl. Phys.* 1 **42** 2073–6