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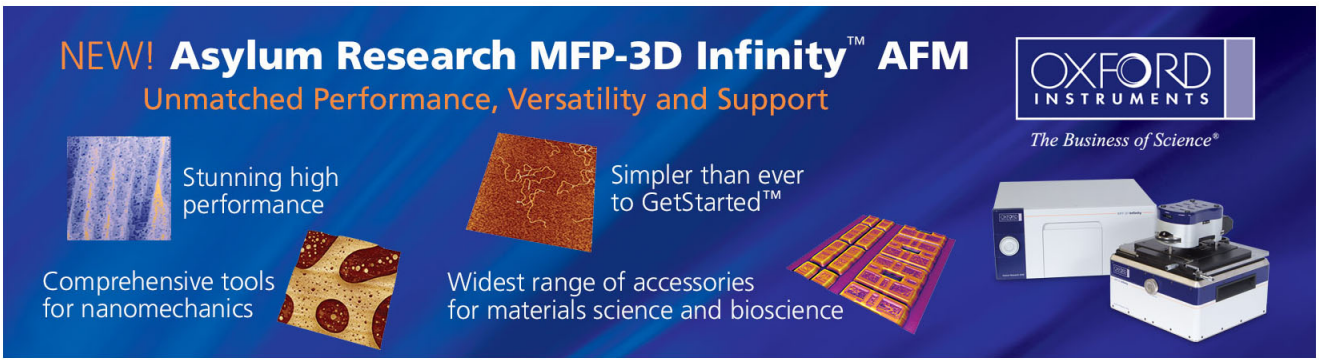

Quasisuperlattice storage: A concept of multilevel charge storage

T. C. Chang[a)]
Department of Physics and Institute of Electro-Optical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan, Republic of China and Center for Nanoscience & Nanotechnology, National Sun Yat-sen University, 70 Lien-hai Road, Kaohsiung 804, Taiwan, Republic of China

S. T. Yan
Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan, Republic of China

P. T. Liu
Department of Photonics and Display Institute, National Chiao Tung University, Hsin-Chu, Taiwan, Republic of China and National Nano Device Laboratory, 1001-1 Ta-Hsueh Road, Hsin-Chu, Taiwan, Republic of China

C. W. Chen
Institute of Electronics, National Chiao Tung University, Hsin-Chu, Taiwan, Republic of China

H. H. Wu
Department of Physics and Institute of Electro-Optical Engineering, National Sun Yat-Sen University, Kaohsiung, Taiwan, Republic of China

S. M. Sze
National Nano Device Laboratory, 1001-1 Ta-Hsueh Road, Hsin-Chu, Taiwan, Republic of China

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A concept of the quasisuperlattice storage has been demonstrated in this study. Under suitably operated voltage, two apparent states of charge storage can be distinguished. The memory effects are due to the multilevel storage in the quasisuperlattice. Also, the *a*-Si quantum wells provide a feasible design for the 2 bit per cell nonvolatile memory devices. The operation of the 2 bit per cell needs to be performed by Fowler–Nordheim tunneling instead of conventional channel hot electron injection. Additionally, the dual read operation of the source and drain sides for conventional SONOS 2 bit/cell device is not necessary, which simplifies the circuit design engineering. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1772873]

Recently, portable electronic devices such as digital cameras, laptops, smart cards, mp3 players, USB Flash, have caught much attention in the market and significantly impacted the semiconductor industries. All of the above-mentioned products are based on the device of Flash nonvolatile memory. The commercially available Flash memory contains the structure of a poly-Si floating gate (FG), which is served as a charge-trapping layer.[1] Since the difficulties of consecutive scaling have been faced, a candidate, SONOS nonvolatile memory device, arose and positioned an important part of the industry.[2–5] SONOS possesses a structure similar to FG memory device but silicon nitride is adopted as the charge-trapping layer rather than poly-Si layer.[6,7] The SONOS structure has a great potential of scaling the thickness of the tunnel oxide down to 1.6 nm and reducing the programming voltage below 5 V.[6,8] That, hence, improves the performance of speed of the memory device. However, the SONOS memories hardly reach a data retention for 10 years. This is why the actual use of SONOS memories is limited to military applications needing high radiation hardness.[9] In this study, both Si and silicon nitride are utilized as the charge-trapping layers and a Si/silicon nitride quasisuperlattice structure is proposed as the multilevel charge storage. Through the electrical measurements, 2 bit per cell Fowler–Nordheim (FN) tunneling operation has been proposed.

Single-crystal, 6 in. in diameter, (100) oriented *p*-type silicon wafers were used in the present study. The wafers were chemically cleaned by a standard RCA cleaning, followed by a dry oxidation in an atmospheric pressure chemical vapor deposition furnace at 925 °C to form a 3 nm tunnel oxide. Subsequently, silicon nitride (Si_3N_4) and amorphous Si (*a*-Si) quasisuperlattice of two periods were deposited by low pressure chemical vapor deposition (LPCVD) at 780 and 550 °C, respectively. Each of the four LPCVD layers was controlled to be about 2 nm. A 10-nm-thick tetraethyl orthosilicate (TEOS) oxide was deposited on the quasisuperlattice as the control oxide layer. To densify the control oxide layer, a steam densification was performed at 982 °C.[10] Via the TEOS oxide deposition and steam densification, the two *a*-Si layers will be crystallized into micro-crystal or poly-crystal, which depends on the grain size of the Si layers. After the Al electrodes were patterned and sintered, capacitance–voltage measurements were performed to investigate the memory effects of the quasisuperlattice storage (QS^2) memory device.

Figure 1 shows the ideal energy band diagram of the QS^2 memory device at $V=0$. The quasisuperlattice of Si_3N_4 and *a*-Si clearly shows the band offsets that can easily trap electrons as the memory elements. The undoped *a*-Si layers are with a wider band gap than that of the Si substrate. To write the memory device, a positive gate voltage has to be applied to make electrons directly tunnel through the tunnel oxide by FN tunneling. The tunneling electrons may be trapped in the

[a)]Electronic mail: tcchang@mail.phys.nsysu.edu.tw

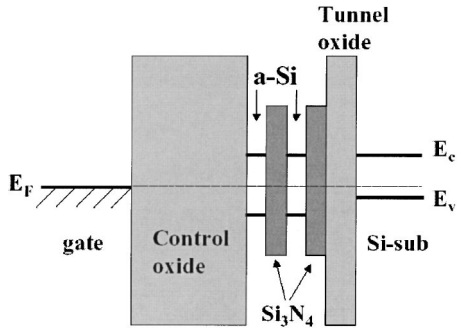

FIG. 1. The ideal energy band diagram of the QS^2 memory device at $V=0$.

trap states of the nitride layers, the interface states between Si_3N_4 and *a*-Si layers, or the quantum wells of the *a*-Si layers. The trapped electrons cause a threshold voltage shift (ΔV_t), memory window, of the memory device, which can be defined as "1" or "0" according to the different threshold voltages. To erase the memory device, negative gate polarity is applied to make the trapped electrons tunnel back to the channel. The control oxide is utilized to prevent the carriers of gate electrode from injecting into the charge trapping sites by FN tunneling.

Figure 2 exhibits $C-V$ hysteresis after the bi-directional voltage sweeping. The voltage is swept between 4 and (−7) V or 7 and (−7) V. The erasing voltage is fixed at (−7) V. Under the programming voltage of 4 and 7 V, the memory window is 0.1 and 0.93 V, respectively, and increasing with the programming voltage. It is worth noting that the hysteresis is counterclockwise, which is due to substrate injection from the electrons of the deep inversion layer and holes of the deep accumulation layer of Si substrate.[11]

Under varied programming voltages and fixed erasing voltage, the relationship between threshold voltage shift and programming voltage is of special interest. Figure 3 exhibits the gate voltage dependence of the memory window. The threshold voltage shift is increased with the gate voltage. However, there are two sudden rises of the threshold voltage

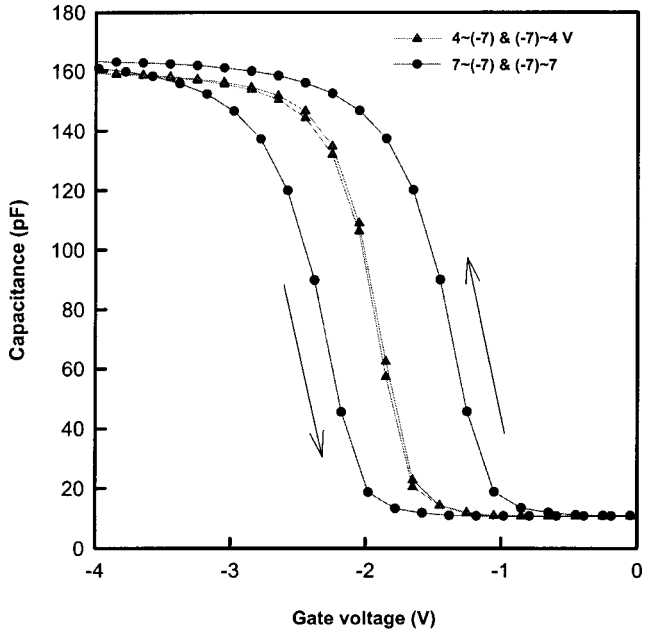

FIG. 2. $C-V$ hysteresis after the bi-directional voltage sweeping. The erasing voltage is fixed at (−7) V.

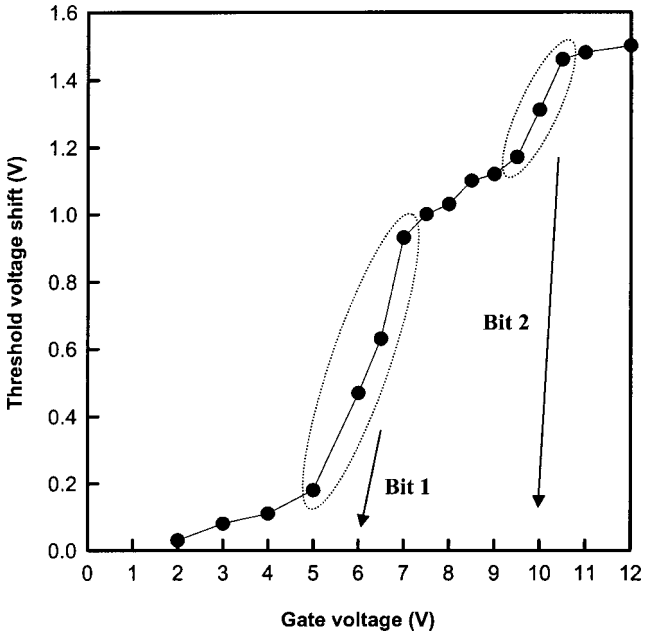

FIG. 3. Gate voltage dependence of the memory window. There are two sudden rises of the threshold voltage shift observed, which take place at around 5 and 9.5 V.

shift observed, which take place at around 5 and 9.5 V. As the memory device is written with different programming voltages, the tunneling electrons will be captured at the trap states of the Si_3N_4 layer, the interface states between Si_3N_4 and *a*-Si layers, and/or the quantum well of *a*-Si. During low-voltage programming, the electrons are captured at the charge-trapping sites of trap states of the Si_3N_4 layer and the interface states between Si_3N_4 and *a*-Si layers. The sudden rise implies the charge storage of the *a*-Si quantum well. Figure 4 shows the band diagram of the memory device under programming. The first sudden rise in Fig. 3 is attributed to the charge storage in the *a*-Si quantum well between two nitride layers. The second sudden rise is deduced that under high-voltage programming the electrons may be written into the *a*-Si quantum well between nitride and control oxide layers. It is also observed that in Fig. 3 the increments of the two sudden rises are obviously different from each other. The

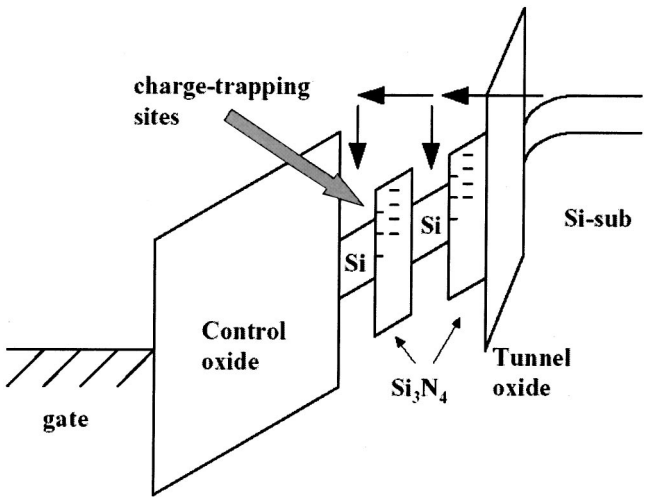

FIG. 4. The band diagram of the memory device under programming. Under suitably operated voltage, two apparent states of charge storage can be distinguishable.

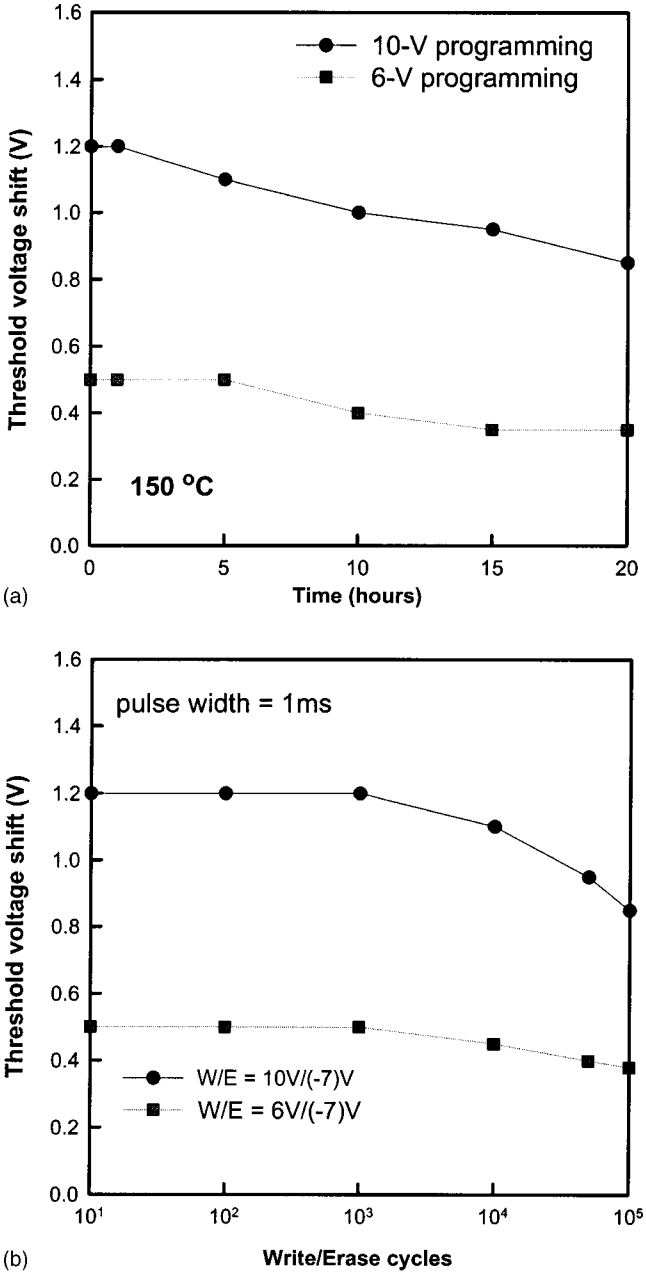

FIG. 5. (a) The retention and (b) endurance of the quasisuperlattice memory device. Two different programming states were performed and the erasing voltage was fixed at (−7) V.

increment of the second sudden rise is smaller than that of the first one. The threshold voltage shift is due to the electrons trapped in the gate dielectrics and the trapped electrons away from the channel influence the threshold voltage less. Therefore, more considerable threshold voltage shift is observed among the first low-voltage charge storage in the *a*-Si quantum well. In this work the quasisuperlattice storage implies a 2 bit per cell operation by FN tunneling.[12] In the design of the multilevel storage, bit-1 can be operated in the *a*-Si quantum well between the nitride layers at low voltage about 5–7 V, e.g., 6 V. Bit-2 can be operated in the *a*-Si quantum well between nitride and control oxide layers at around 10 V. The 2 bit per cell operation is performed by FN tunneling instead of the conventional channel hot electron injection. Also, the dual read operation of source side and drain side for conventional SONOS 2-bit/cell device is not necessary, which simplifies the circuit design engineering. To examine the reliability issues of the quasisuperlattice structure, the retention and endurance characteristics have been investigated. As shown in Fig. 5(a), the retention characteristics of the two programming states were strictly performed at the environment of 150 °C. For each programming state, the memory window remains distinguishable up to 20 h at 150 °C. Also, the low-voltage programming exhibits a more stubborn retention performance than that of the high-voltage programming. Figure 5(b) shows the endurance characteristics of the memory device for low- and high-voltage programming states. Even 10^5 write/erase cycles are conducted, both programming states possess sufficient memory window for a typical sense amplifier to detect and define "1" and "0," which implies the feasibility of the 2 bit per cell quasisuperlattice nonvolatile memory devices.

In summary, quasisuperlattice storage has been demonstrated for the concept of multilevel charge storage. In the relationship between threshold voltage shift and gate programming voltage, two sudden rises were observed. The obvious memory effects from the measurements of $C-V$ hysteresis exhibited two distinguishable charge storages, which can be utilized as a memory device of 2 bit-per cell.

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