Electromigration and Integration Aspects for the Copper-SiLK System

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In this study, the thermal characteristics and electromigration (EM) resistance of two dielectrics, SiLK™ and SiO_2, are investigated to evaluate the feasibility of low dielectric-constant SiLK for intermetal dielectric applications. Liftoff patterning was employed to fabricate the Cu interconnect for the EM test, and the Taguchi method was used in the experimental design to identify the key parameters for a successful liftoff. It was shown that the thermal impedance of the metal lines passivated with SiLK is 14% higher than that of metal lines passivated with SiO_2. On the basis of the thermal impedance and temperature rise of the interconnect, it was concluded that the major heat transfer path is via the underlayer dielectric to the Si substrate. The activation energy of EM for Cu passivated with SiLK is smaller, and the EM lifetime is shorter than that of Cu passivated with SiO_2. Possible mechanisms are discussed.

Key words: Si, SiO_2, Cu, electromigration, SiLK

INTRODUCTION

As interconnect feature size decreases and clock frequencies increase, interconnect resistance × capacitance (RC) time delay and current density increment become the major limitation to achieving high circuit speeds and reliability. Copper, with its high electrical conductivity and melting temperature, provides smaller RC time delay and electromigration (EM) resistance than Al-based metallization does.[1–4] However, the usage of a copper interconnect poses many challenges, such as lack of a stable self-passivating oxide,[5] poor adhesion of copper to the dielectric,[6] difficulty in dry etching,[7] high diffusivity in silicon and SiO_2,[8,9] and deep levels in silicon.[10]

One of the primary problems with integrating Cu with a low-k dielectric into a multilevel metallization system is the difficulty in patterning the metal. There are several methods for patterned Cu interconnects, such as selective electroless plating, selective chemical-vapor deposition, high-temperature reactive-ion etching, and the liftoff technique.[11,12] Liftoff patterning has been used here to study the integration issues of Cu and the SiLK™ system (Dow Chemical Company, Midland, MI). SiLK is a low molecular-weight aromatic thermosetting polymer. The low molecular-weight polymer will flow to fill small gaps and planarize underlying topology. SiLK films are one of the most attractive interlayer dielectrics because of their good surface planarization characteristics, low dielectric constant, and high toughness.[13,14]

In this study, direct current sputtering was employed to deposit Cu films onto SiO_2/Si substrates. The Taguchi method[15] was applied in the experimental design to identify the key processing parameters for the liftoff process of Cu metallization. Both SiLK and SiO_2 were used as the passivation layer of Cu, and the effects of the overlayer dielectric on the thermal characteristics and EM of copper were explored. The major focus of this work was to investigate the integration aspects of the Cu-SiLK system, including the liftoff process conditions of the Cu interconnect and reliability issues (such as heat dissipation and EM resistance) of the system.

EXPERIMENTAL PROCEDURE

Four-inch-diameter p-type (100) Si wafers with nominal resistivity of 1–10 Ω-cm were used as substrates. An interdigitated comb and serpentine test

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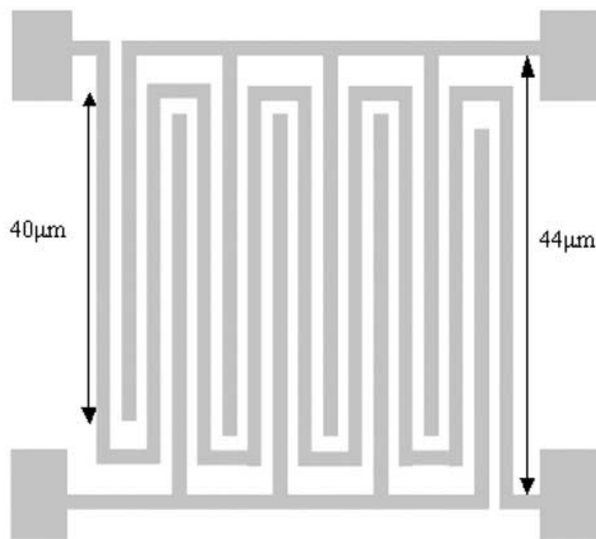

Fig. 1. Test structure for liftoff and EM study.

structure, as shown in Fig. 1, was employed for liftoff and EM study. After standard RCA cleaning and spin drying, 500-nm thermal oxide was grown at 950°C in a steam atmosphere. Then, plasma-enhanced chemical vapor deposition (PECVD) was employed to grow 50 nm of Si_3N_4 on top of the thermal oxide. The parameters studied for the liftoff process include baking of photoresist, thickness of metal, type of barrier, room-temperature storage, oscillation intensity, and oscillation time. The Taguchi method was employed to design the liftoff experiments. Sixty-five samples are studied for each condition, and an optical microscope was used to examine whether the process was successful, i.e., whether an integral test structure was obtained. The optimum process parameters were employed in the liftoff for preparing specimens for the EM test.

The adhesion strength of Cu to the underlayer dielectric was evaluated with a direct pull tester (Sebastian Five, QUAD Group, Spokane, WA). A stud was bonded perpendicularly to the coating surface with epoxy by holding it in contact through a spring mounting chip designed especially for the stud. The assembly was cured at 150°C for 1 h. The stud was then put into the platen and gripped. The tester pulled the stud and samples down against the platen support ridge until the coating failed. The stress of adhesion, σ_a, is defined as $\sigma_a = F/A$. The area of A is the circular section of the stud.

Specimens for EM tests were 250-nm Cu with a 30-nm TaN barrier. The metal film was obtained with the optimized liftoff process. After pattern delineation, wafers were passivated with 650-nm SiLK or 500-nm SiO_2. The SiO_2 films were deposited by the decomposition of tetraethyl orthosilicate with PECVD (Multichamber PECVD, STS-Multiplex Cluster System, England) at 250°C and 100 mtorr. After contact hole opening, 1-μm-thick Al was deposited and patterned to form the contact pads. Finally, samples were annealed at 450°C for 1 h in a 100-torr N_2 purge furnace.

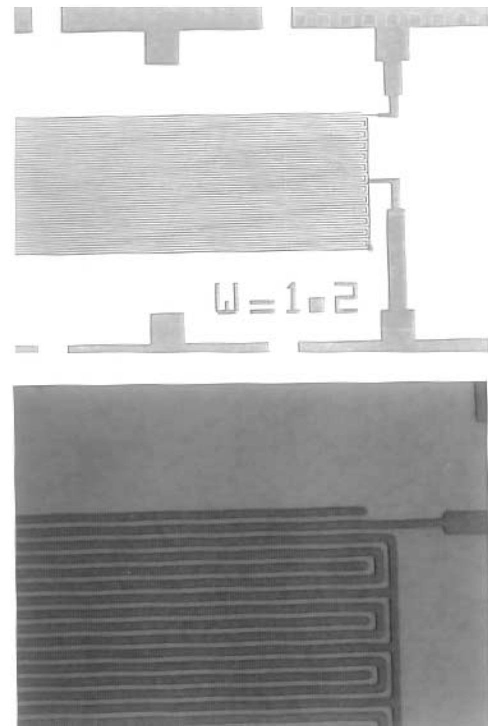

Fig. 2. Photograph of the patterned interdigitated structure.

Accelerated EM tests were carried out on a hot chuck of a probe station. The stressing current density was 2.8×10^6 A/cm^2, and the ambient temperature ranged from 225°C to 300°C in air for the EM test.

RESULTS AND DISCUSSION

Figure 2 shows the photograph of the patterned interdigitated structure. A summary of the liftoff test designed with the Taguchi method is given in Table I. Among the parameters studied, employment of a barrier layer appears to be a key factor to ensure successful liftoff. The barrier layer enhances the adhesion strength of the metal to the dielectric and helps in maintaining the pattern integrity during liftoff. The adhesion strength of Cu to SiO_2 increases from 9.8 MPa to 37.5 MPa when a barrier layer is inserted. On the basis of the yield data shown in Table I, the optimum Cu liftoff conditions are curing the photoresist at 120°C for 3 min, using a metal thickness of 200 nm with a 30-nm TaN barrier layer, and using medium ultrasonic oscillation for an appropriate period of time (4 h in this study) to strip resist and liftoff the metal.

The joule heating induced by power consumption will raise the temperature of the interconnect and integrated circuit chips. The average temperature increase, ΔT, in the Cu interconnect caused by joule heating is shown in Fig. 3. The ΔT of Cu passivated

Table I. Summary of the Liftoff Test

Test Conditions Test Run	Baking of Photoresist*	Metal Thickness (nm)	Barrier Layer	25°C Storage (Days)	Oscillation Intensity**	Oscillation Time (Hour)	Yield*** (%)
1	Y†	200	N‡	0	S	2	0
2	Y	250	Ta	2	M	4	9
3	Y	300	TaN	7	W	8	25
4	N‡	200	N	2	M	8	0
5	N	250	Ta	7	W	2	6
6	N	300	TaN	0	S	4	28
7	Y	200	Ta	0	W	4	9
8	Y	250	TaN	2	S	8	51
9	Y	300	N	7	M	2	0
10	Y	200	TaN	7	M	4	66
11	Y	250	N	0	W	8	0
12	Y	300	Ta	2	S	2	3
13	N	200	Ta	7	S	8	3
14	N	250	TaN	0	M	2	38
15	N	300	N	2	W	4	0
16	N	200	TaN	2	W	2	51
17	N	250	N	7	S	4	0
18	N	300	Ta	0	M	8	0

*The photoresist used is TMHR iP-3650 from TOK Co., Japan; the baking is at 120°C for 3 min.
**The ultrasonic oscillation to lift the photoresist off. S: strong (~200 Watt), M: medium (~170 Watt), W: weak (~140 Watt).
***The sample size is 65.
†y is with baking.
‡N is without baking or barrier layer.

with SiLK (Cu-SiLK) is larger than that of Cu passivated with SiO_2 (Cu-SiO_2) especially at higher current density. The temperature rise caused by joule heating is determined by measuring the temperature coefficient of resistance (TCR):[16]

$$\mathrm{TCR(T)} = \frac{R_1 - R_2}{R_T \times (T_1 - T_2)} \quad (1)$$

where R_1, R_2, and R_T are the resistance at temperatures T_1, T_2, and T (T is normally taken as 20°C), respectively. Therefore, the average temperature rise in the interconnect is

$$\Delta T = T_1 - T_2 = \frac{R_1 - R_2}{\mathrm{TCR(T)} \times R_T} \quad (2)$$

The TCRs of Cu-SiO_2 and Cu-SiLK are 3.22×10^{-3} C^{-1} and 3.21×10^{-3} C^{-1}, respectively. The thermal conductivity of SiLK (1.9×10^{-3} W/cm-°C) is one eleventh of that of silicon dioxide (2.09×10^{-2} W/cm-°C).[13] The temperature rise induced by joule heating is dissipated both through the underlayer insulator dielectric to the Si substrate, which acts as a heat sink, and through the overlayer passivation dielectric, as shown schematically in Fig. 4.

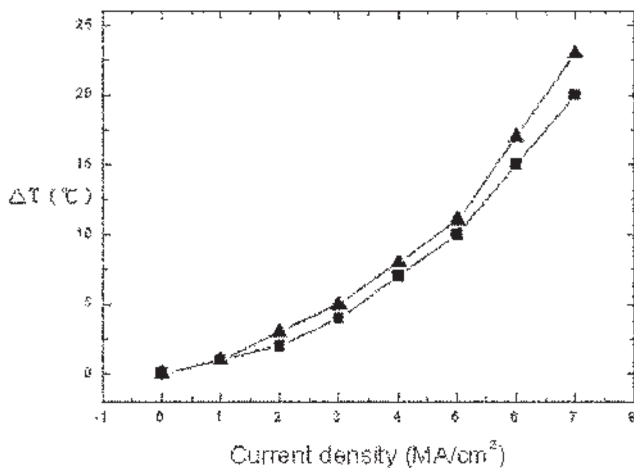

Fig. 3. The average temperature increments of the Cu interconnect as a function of current density. Ambient temperature: 30°C; ■: Cu passivated with SiO_2; and ▲: Cu passivated with SiLK.

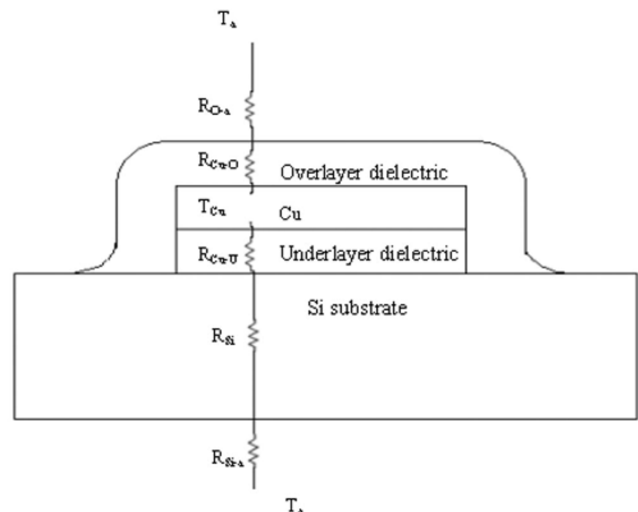

Fig. 4. Schematic diagram for interconnect heat dissipation.

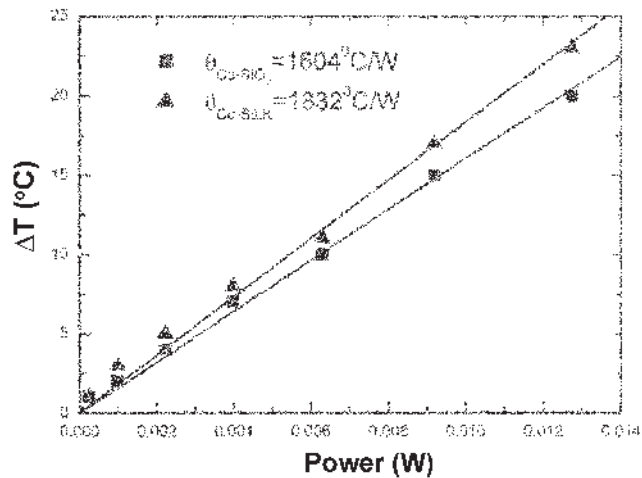

Fig. 5. Temperature increment versus input power of Cu interconnects with SiO_2 or SiLK passivation.

The difference in ΔT between Cu-SiLK and Cu-SiO_2 is not very significant. At a current density of 3×10^6 A/cm^2, ΔT for Cu-SiLK and Cu-SiO_2 are 3°C and 2°C, respectively, as shown in Fig. 3. This suggests that most heat dissipated through the underlayer dielectric to the Si heat sink (substrate); hence, although thermal conductivity of SiLK and SiO_2 differs by an order of magnitude, not much difference is observed between the temperature rise of ΔT of Cu passivated with SiLK and that of Cu passivated with SiO_2. Previous work indicates that when using an underlayer dielectric with poor thermal conductivity, the joule heating could cause a huge temperature rise at the interconnects and, hence, accelerate the EM damage and, finally, lead to catastrophic interconnect failure as well as thermal decomposition of the underlayer dielectric.[1] The thermal impedance, θ_j, is defined by the expression:[17]

$$\Delta T = P \times \theta_j \tag{3}$$

where P is the power input of the interconnect. The θ_j of the Cu-SiLK specimen is 1,832°C/W, which is 14% higher than that of Cu-SiO_2 (1,604°C/W), as shown in Fig. 5. As one compares the thermal impedances obtained in this study to those of a previous work that studied the effect of the underlayer dielectric on the thermal characteristics of the interconnect,[1] it is concluded that the thermal conductivity of the underlayer dielectric plays a crucial role in heat dissipation because most heat dissipated through the underlayer dielectric to the Si substrate, which has a larger thermal conductivity (6.28×10^{-1} W/cm-°C) as compared to the dielectric. In the previous work, polyimide and SiO_2 were used as the underlayer dielectric. The thermal conductivity of SiO_2 is about 20 times that of polyimide (1.05×10^{-3} W/cm-°C). The thermal impedance of Cu on SiO_2 and Cu on polyimide are 234°C/W and 736°C/W, respectively, as compared to 1,604°C/W (Cu-SiO_2) and 1,832°C/W (Cu-SiLK) in this study. Besides, a temperature rise (ΔT) of over 600°C was observed in the Cu on the polyimide system and caused the decomposition of the polyimide underlayer. In this study, the difference in ΔT between Cu with different passivation layers is not as significant as that with different underlayers, and the magnitude of ΔT (i.e., 3°C (Cu-SiLK) and 2°C (Cu-SiO_2)) is small. Hence, the thermal conductivity of the passivation dielectric is not as crucial as that of the underlayer dielectric in respect to degradation induced by thermal stress.

The relative resistance, R/R_0, as a function of time at various temperatures is exhibited in Fig. 6. The

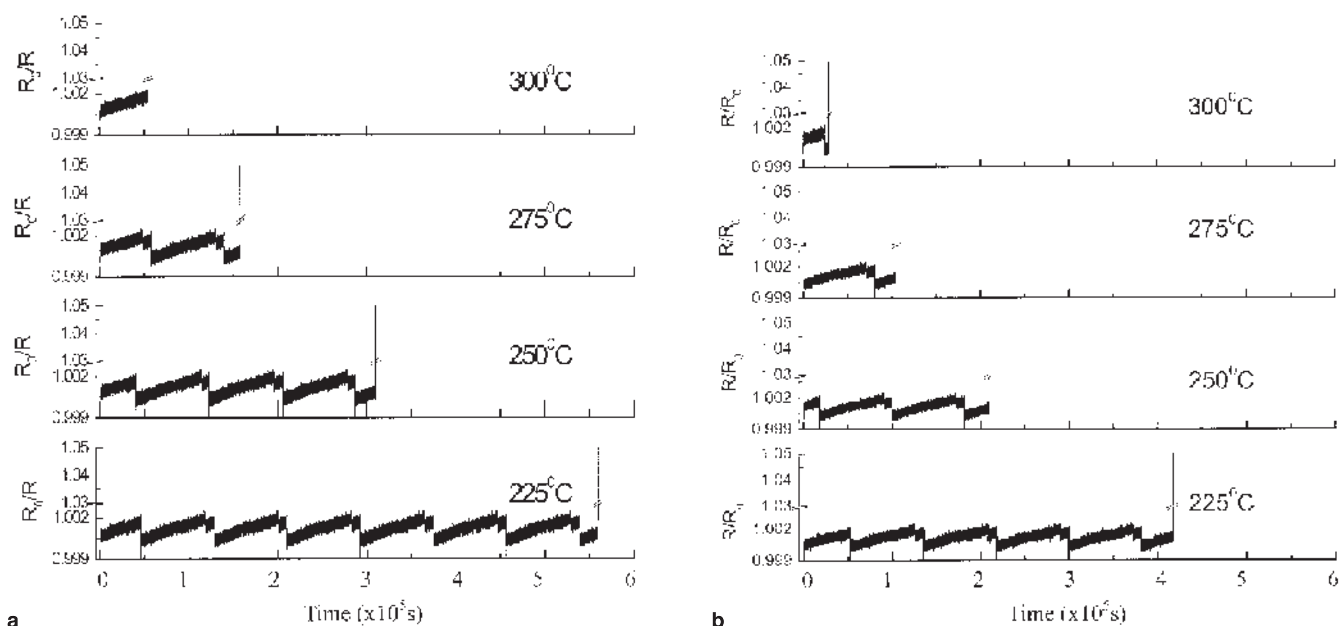

Fig. 6. Relative resistance as a function of current stressing time at various temperatures of Cu passivated with (a) SiO_2 and (b) SiLK. Current density: 2.8×10^6 A/cm^2.

resistance increases more rapidly at higher soaking temperature. By defining a resistance change of 4.5% as the criterion of early stage failure, i.e., assuming the dimensions of the maximum voids are much less than the line width, the time rate change of electrical resistance, dR/dt, caused by EM damage is thermally activated and can be expressed by the following empirical equation:[18]

$$\frac{dR}{dt} \times \frac{1}{R_0} = AJ^n \exp[-\frac{Q}{kT}] \qquad (4)$$

where R_0 is the initial resistance at a given temperature, A is a pre-exponential factor, J^n is the electron current density raised to the nth power, T is temperature, and Q is the activation energy for EM. The activation energy can be obtained from the ln[(dR/dt)$(1/R_0)$] versus 1/T plot shown in Fig. 7. As can be seen from Figs. 6 and 7, both the time to failure and activation energy for EM of Cu-SiLK are smaller than those of Cu-SiO_2. There are several possible causes that could result in shorter EM lifetime and smaller activation for EM of Cu-SiLK as compared to Cu-SiO_2. One is the smaller thermal conductivity of SiLK, which causes a larger temperature gradient and accelerates the EM process.

The residual stress of the Cu film, resulting from the thermal expansion mismatch between the copper and the passivation layer, could also affect the EM process, the residual stress can be estimated as follows:

$$\sigma = E(\alpha_p - \alpha_{Cu})(T - T_0) \qquad (5)$$

where E is the Young's modulus of the Cu film (11,252 kg/mm^2), and α_p and α_{Cu} are the coefficients of thermal expansion (CTE) of the passivation layer and Cu, respectively. The term T_o is the annealing temperature (450°C), and T is testing temperature (225–300°C). The CTE of Cu, SiLK, and SiO_2 are 16.5 ppm/°C, 66 ppm/°C, and 0.5 ppm/°C, respectively.[13,19] Hence, SiLK exerts a compressive stress of 83.54–125.32 kg/mm^2 (300–225°C), while SiO_2 has a tensile stress of 27.01–40.51 kg/mm^2 (300–225°C). Previous works suggest that the presence of high compressive stress would enhance EM resistance.[20,21] However, in this study, samples passivated with SiLK (presumably under compression) have shorter lifetimes than those passivated with SiO_2 (presumably under tension). A similar phenomenon was observed on Cu passivated with various polyimide films.[22] It is probably due to the viscoelastic behavior of the polyimide and/or that at the testing temperature; the polymer flexes and relieves some of the stress present in a test line. Hence, the effect of the compressive stress on the EM resistance is not appreciable.

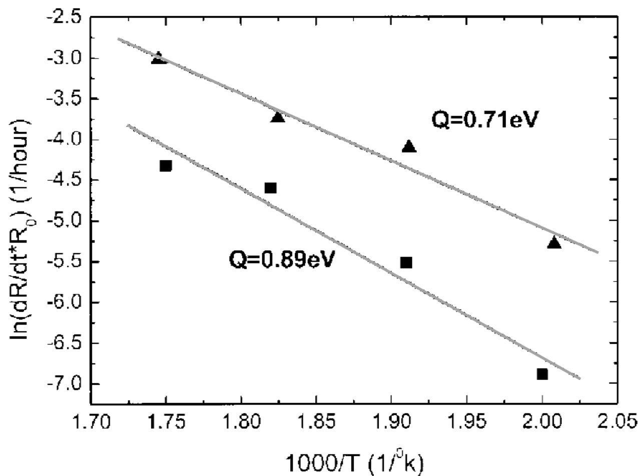

Fig. 7. The ln[(dR/dt)$(1/R_0)$] versus 1/T and activation energy, Q, for Cu films passivated with SiO_2 (■) or SiLK (▲) during EM test. Current density: 2.8 × 10^6 A/cm^2.

Table II. Failure Time and Failure Time Ratio of Cu Films Stressed at 2.8 × 10^6 A/cm^2 and Various Temperatures

Temperature (°C)	$t^*_{SiO_2}$ (×10^5 s)	t^*_{SiLK} (×10^5 s)	t_{SiLK}/t_{SiO_2}
225	5.59	4.18	0.75
250	3.10	2.09	0.67
275	1.58	1.05	0.66
300	0.54	0.29	0.54

*The terms t_{SiO_2} and t_{SiLK} are time to failure for Cu films passivated with SiO_2 and SiLK, respectively.

Table II summarizes the failure time and failure time ratio of Cu films stressed at 2.8 × 10^6 A/cm^2 and various temperatures. The ratio of the failure time (t_{SiLK}/t_{SiO_2}) between Cu passivated with SiLK (t_{SiLK}) and Cu passivated with SiO_2 (t_{SiO_2}) decreases as temperature increases. The atomic diffusivity, D, of copper for passivated samples can be expressed as follows:[23,24]

$$D = D_0 \exp(-Q/kt) = D_0 \exp[-(E_m + f\Omega)/kT] \qquad (6)$$

where f is the constrain force provided by passivation, Ω is the atomic volume, and E_m is the activation energy for diffusion. The Young's modulus of SiO_2 and SiLK are 72 GPa and 2.45 GPa, respectively.[13] The more rigid SiO_2 exerts a larger constrain force on the metallization and retards the diffusion of the metal atoms. Hence, the lifetime for SiO_2-passivated samples is longer than that of SiLK-passivated ones. Besides, it is argued that at higher temperatures the polymer relaxes more, the constrain force decreases diffusion of Cu faster, and consequently, the t_{SiLK}/t_{SiO_2} ratio decreases with the increase of temperature.

CONCLUSIONS

The employment of a barrier layer appears to be a key factor to ensure a successful liftoff for Cu interconnects because the barrier enhances the adhesion strength of metal to the dielectric and helps in maintaining the pattern integrity during liftoff. The thermal impedance of Cu interconnects passivated with SiLK (Cu-SiLK) is about 14% higher than that of Cu passivated with SiO_2 (Cu-SiO_2). Besides, the

difference in joule-heating-induced temperature increase, ΔT, between Cu-SiLK and Cu-SiO_2 is not significant. This suggests that most heat dissipated through the underlayer dielectric to the Si substrate, which acts as a heat sink. Hence, the thermal conductivity of the passivation dielectric is not as critical as that of the underlayer dielectric in respect to thermal-stress-induced degradation. The EM resistance and lifetime of SiLK-passivated Cu is poorer than those of the SiO_2-passivated one. This is attributed to the small thermal conductivity and low rigidity of the SiLK dielectric.

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