Temperature Effect on Read Current in a Two-Bit Nitride-Based Trapping Storage Flash EEPROM Cell

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***Abstract*—The temperature effect on the read current of a two-bit nitride-storage Flash memory cell is investigated. In contrast to a conventional silicon–oxide–nitride–oxide (SONOS) cell with uniform Fowler–Nordheim (FN) programming, a significant high-V_T state read current increase, which results in the read window narrowing at high temperature, is observed in a channel hot electron (CHE) programmed cell. The increment of high-V_T state leakage current shows a positive correlation with program/erase threshold voltage window. Since the temperature effect is very sensitive to a locally trapped charge profile, a two-dimensional simulation with a step charge profile is employed to characterize the relationship between current increment and both charge width and charge density.**

***Index Terms*—EEPROM, Flash memory, nitride-based trapping storage, temperature effect, trapped charge profile, window narrowing.**

I. Introduction

FLASH memory devices based on the storage of charges in localized trap states in silicon nitride were proposed. By taking the advantages of localized charge trapping in the nitride above source and drain junctions, two-bit storage of a single cell can be achieved by utilizing channel hot electron (CHE) program and band-to-band hot hole erase with a reverse read scheme [1]. Some reliability issues such as cycling endurance and retention have been discussed [2]–[4]. For commercial applications, cell operation at temperature up to 85 °C is required. The maintenance of sufficient read current window is necessary in a wide range of temperature. In this letter, we will report for the first time on the temperature effect on read current in a trapping storage device. The impact of a trapped charge profile in high-temperature operation will be studied.

Read window narrowing at high temperature is observed and the relationship between high-V_T state read current increment at high temperature and the trapped charge profile is discussed. A MXVAND cell [3], [4] with a gate length of 0.36 μm and a gate width of 0.2 μm is used. The thicknesses of top and bottom oxides are 9 and 5 nm, whereas the interleaving nitride layer is 5.5 nm thick. Devices are programmed by channel hot electron (CHE) injection at $V_{\rm GS} = 11$ V. To emulate product operation, the drain bias steps from 3.0 to 4.4 V with $\Delta V_D = 0.2$ V.

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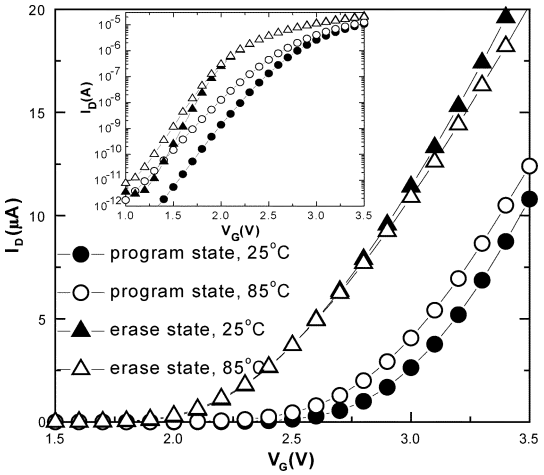

Fig. 1. Measured I_D–V_G curves for both linear and logarithmic scale, biased at $V_D = 1.6$ V, of two MXVAND cells in erase state and program state at room temperature and high temperature, respectively.

II. Read Current Window Narrowing

Fig. 1 shows the I_D–V_G curves, biased at $V_D = 1.6$ V, of MXVAND cells in erase state and program state at room temperature, and high temperature respectively. Here, the erase state and the program state represent the high bound of low-V_t cells and the low bound of high-V_T cells in 2-bits per cell product operation. If we read the data of cells at $V_G = 3$ V, the read current window is about 8.77 μA at room temperature. But the read current window reduces to 7 μA when the cell operates at 85 °C. The degraded read current window may cause an error during data sensing at high temperature especially when the other reliability issues [3], [4] are also taken into account. From the figure, it is found that the window narrowing mainly comes from the read current increment in program state.

When a MOSFET is operated at high temperature, two mechanisms will affect the read current of device. One is the threshold voltage lowering, and the other is the mobility degradation [5], [6]. The former may increase the currents in subthreshold and weakly on regions. The later may degrade the currents in fully on region. As a result, there is usually a crossover between the current–voltage (*I–V*) curves of device measured at room temperature and high temperature. In Fig. 1, the crossover behavior

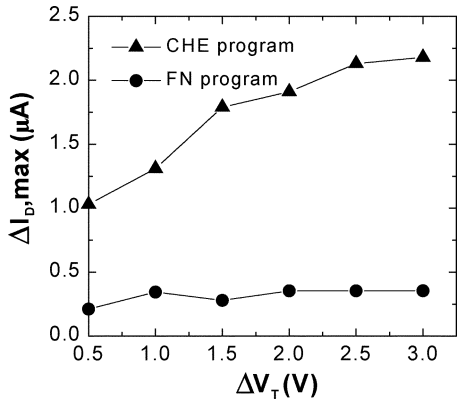

Fig. 2. Temperature effect (ΔI_D) comparison between CHE programming and FN programming. The CHE programming is at $V_{\rm GS} = 11$ V, V_D steps from 3.0 to 4.4 with $\Delta V_D = 0.2$ V, and the V_G steps from 17 to 19 V with $\Delta V_G = 0.5$ V for FN programming.

of the erase state cell happens at about $V_G = 2.6$ V, and the current increment is insignificant in the weakly on region. But for the cell at program state, which has locally programmed charges at source side, the crossover behavior does not appear even when the applied V_G is as high as 3.5 V. Because the impact of our 85 °C measurement on trapped charge profile is confirmed insignificant (not shown), it is inferred that the localized distribution of programmed charges enhance the subthreshold leakage current and results in a larger shift of I_D–V_G curve at high temperature. Thus, a delayed crossover point and a larger drain current increment are observed at the program state.

III. Influence of Trapped-Charge Profile

In Fig. 2, the current increments by using CHE and FN programming are compared. ΔI_D is defined as the maximum read current difference between room temperature and 85 °C, and ΔV_T in Fig. 2 is the V_T window. As programmed V_T is increased, the read V_G for ΔI_D extraction should also increase to keep the constant gate overdrive. The ΔI_D increases with increasing CHE programmed V_T but it keeps almost the same for the cells by FN programming. This result suggests that the temperature effect on read current is enhanced by a localized charge profile and is worsened when the program/erase V_T window is increased.

In the subthreshold region, the drain current is dominated by diffusion current [7] and can be expressed as

$$I_D = I_0 \cdot \exp\left(\frac{q\Psi_{S,\max}}{kT}\right)$$

where $\Psi s, \max$ is the maximum surface potential. Although the first term (I_0) is a function of temperature, the current increment at high temperature is dominated by the second term due to the exponential dependence. Therefore, the entirely different ΔI_D behavior between FN programming and CHE programming originates from the $\Psi s, \max$ difference. The characterization of $\Psi s, \max$ in FN and CHE programmed cells will be discussed in the following.

IV. Relationship Between Trapped Charge Profile and Current Increment

To characterize the observation of Fig. 2, a 2-D simulation [8], [9] is utilized to compare the surface potential of cells by

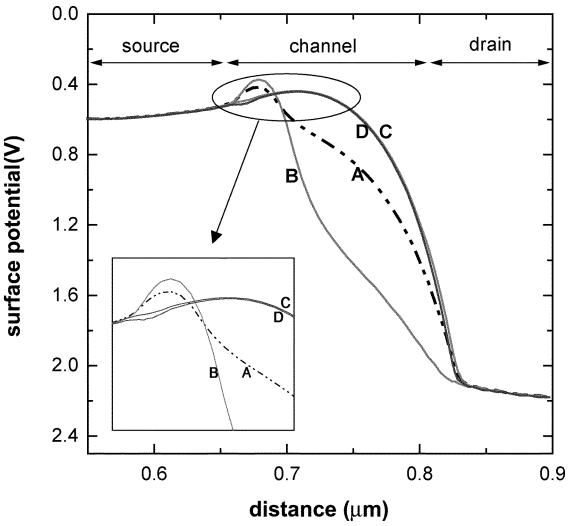

Fig. 3. Simulated surface potential distribution in cells with different V_T by FN and CHE programming. (a) CHE, $\Delta V_T = 0.5$ V at $V_G = 1.5$ V. (b) CHE, $\Delta V_T = 2.0$ V at $V_G = 3.0$ V. (c) FN, $\Delta V_T = 0.5$ V at $V_G = 1.5$ V. (d) FN, $\Delta V_T = 2.0$ V at $V_G = 3.0$ V. The applied bias is $V_D = 1.6$ V with a constant gate overdrive.

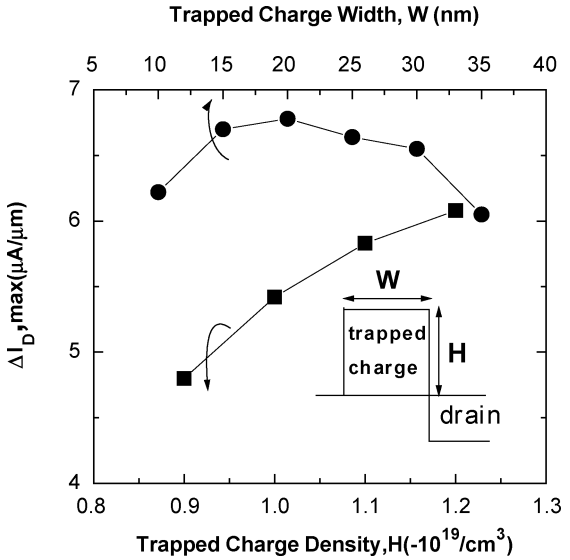

Fig. 4. Relationship between temperature effect (ΔI_D) and both charge density (*H*) and charge width (*W*). The charge density is modified with a fixed width 30 nm over channel, and the charge width is modified with a fixed density $-2 * 10^{19}(1/\mathrm{cm}^3)$ over channel.

CHE programming and FN programming. Fig. 3 shows the simulated surface potential distribution of cells with different V_T by FN and CHE programming. One can see that the cells by FN programming have a constant $\Psi s, \max$ due to the constant gate overdrive. As a result, similar ΔI_D is obtained in the FN programmed cells. As to the CHE programmed cells, the $\Psi s, \max$ are dominated by the local potential barrier, which is pulled high by the local trapped charge. Consequently, if the same ΔV_T are programmed by FN injection and CHE injection, the CHE programmed cell would have a larger $\Psi s, \max$ and much more serious temperature effect. In addition, $\Psi s, \max$ is increased with increasing CHE programmed V_T even the constant gate overdrive is adopted, as shown in Fig. 3. Thus, ΔI_D is increased with increasing CHE programmed V_T.

To further clarify how the temperature effect is influenced by a localized charge profile, the relationship between ΔI_D and both the charge density and the charge width are characterized by simulation. As illustrated in Fig. 4, when the charge density is increased with a fixed width, the ΔI_D is increased due to the increased $\Psi s, \max$. In addition, when the charge distribution is narrowed with a fixed density, the programmed V_T becomes smaller and only a smaller V_G should be applied to extract ΔI_D. It leads to a larger $\Psi s, \max$ and the increased ΔI_D. As the charge width is narrower than a certain value, $\Psi s, \max$ would reduce substantially due to drain-induced barrier lowering. Thus, the ΔI_D turns to decrease when the charge distribution is narrower than a certain width.

V. Conclusion

In this work, the temperature effect of a two-bit nitride-storage Flash memory cell is investigated. A significant program-state read current increment in a CHE programmed cell is observed at high temperature. It degrades the read current window and impacts on data sensing. A localized charge profile that enhances the subthreshold leakage at high temperature may be the root cause of this current increment. From two-dimensional simulation results, the current increment becomes larger as the charge density is higher or the charge distribution is narrower in a certain range.

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