Use of WN_X as the Diffusion Barrier for Interconnect Copper Metallization of InGaP–GaAs HBTs

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***Abstract*—Use of WN_X as the diffusion barrier for interconnect copper metallization of InGaP–GaAs heterojunction bipolar transistors (HBTs) was studied. The WN_X (40 nm) and Cu (400 nm) films were deposited sequentially on the InGaP–GaAs HBT wafers as the diffusion barrier and interconnect metallization layer, respectively, using the sputtering method. As judged from the data of scanning electron microscopy, X-ray diffraction, Auger electron spectroscopy, and sheet resistance, the Cu–WN_X–SiN and Cu–WN_X–Au structures were very stable up to 550 °C and 400 °C annealing, respectively. Current accelerated stress test was conducted on the Cu–WN_X metallized HBTs with $V_{CE} = 2$ V, $J_C = 140$ kA/cm² and stressed for 55 h, the current gain (β) of these HBTs showed no degradation and was still higher than 100 after the stress test. The Cu–WN_X metallized HBTs were also thermally annealed at 250 °C for 25 h and showed no degradation in the device characteristics after the annealing. For comparison, HBTs with Au interconnect metallization were also processed, and these two kinds of devices showed similar characteristics after the stress tests. From these results, it is demonstrated that WN_X is a good diffusion barrier for the interconnection copper metallization of GaAs HBTs.**

***Index Terms*—Copper, GaAs, heterojunction bipolar transistors (HBTs), metallization, tungsten nitride.**

I. Introduction

COPPER METALLIZATION has become an important topic in the silicon integrated circuit technology ever since IBM announced its success in silicon very-large scale integration (VLSI) process [1]–[3]. The advantages of copper metallization for Si VLSI include lower resistivity and higher electromigration resistance. However, copper diffuses very fast into Si when it is in contact with Si substrate without any diffusion barrier [4]–[6]. As in the silicon case, copper also diffuses very fast into GaAs when copper is in direct contact with the GaAs substrate without any diffusion barrier [7]. Even though the use of copper as metallization metal has become very popular in Si devices, there were very few reports of copper metallization of GaAs devices published in the literature and Ta and TaN were used as the diffusion barriers for copper metallization in these reports [8]–[10]. Traditionally, GaAs devices such as metal semiconductor field-effect transistors (MESFETs), high electron mobility transistors (HEMTs), and heterojunction bipolar transistors (HBTs) use Ti as an adhesion layer, and Au as the metallization metal for interconnect metal and transmission lines. The use of copper as the metallization metal has several advantages over gold, such as lower resistivity, higher thermal conductivity, and lower cost. If Cu replaces Au as the interconnect metal for the HBTs, then the improvement in the electrical conductivity can increase the transmission speed of the circuits, and the manufacturing cost will be substantially reduced. However, the use of copper interconnect for HBTs requires suitable diffusion barrier which is compatible with the HBT processes to prevent copper interdiffusion into the GaAs substrate.

Generally, the n-type AuGe–Ni–Au and p-type Ti–Pt–Au or Pt–Ti–Pt–Au ohmic contacts are the most widely used structures for the fabrication of the GaAs-based HBTs. The top layers of the ohmic structures are Au. From the phase diagrams of these materials systems, there are many possible intermetallic compounds in the Cu–Au binary system. Interdiffusion of Cu and Au in the Cu–Au structure was observed at a temperature as low as 150 °C, and a very rapid increase in the resistivity was observed at 250 °C [11]. Meanwhile, HBT is usually passivated with plasma-enhanced chemical vapor deposited silicon nitride (PECVD-SiN) film; if Cu is in direct contact with the silicon nitride film of poor quality, a large amount of copper may diffuse through the microdefects of the PECVD-SiN films during the heat treatment of the metallization process, and the leakage current will increase as a result of the copper diffusion [12]. Diffusion of copper through the ohmic contacts and silicon nitride film into the HBTs will cause the degradation of the electrical properties of the HBT devices. Therefore, a diffusion barrier between ohmic metal and copper and between silicon nitride and copper are mandatory for the use of copper as the interconnect metal for the GaAs HBTs. Tungsten nitride has high melting point, good thermal and chemical stability, and is a good diffusion barrier between Si and Cu. In addition, tungsten does not form intermetallic compound with Cu and Au, as judged from the phase diagram. In this paper, the thermal stabilities of Cu–WN_X–Au and Cu–WN_X–SiN film structures were investigated, and these materials systems were used to fabricate the InGaP–GaAs HBTs with copper interconnects. We are reporting for the first time the fabrication and electrical performance of the Cu-metallized InGaP–GaAs HBTs with WN_X as the diffusion barrier.

II. Experimental

The experiments in this paper include two parts. The first part is the thermal stability study of the diffusion barrier. The stabil-

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ities of WN_X between Cu and Au and between Cu and silicon nitride were investigated. A WN_X film of 40-nm thickness was sputtered onto the Au–GaAs and SiN–GaAs samples, respectively, and then, 200-nm Cu film was subsequently sputtered on top of the WN_X films without breaking vacuum in a multitarget magnetron sputtering system to form Cu–WN_X–Au and Cu–WN_X–SiN multilayer structures. The WN_X films were deposited by dc-magnetron reactive sputtering system using a *W* (99.99%) target reactively sputtered in the N_2–Ar mixture with 20% N_2 and 80% Ar. Prior to the sputtering, the chamber was pumped down to 1.6×10^{-6} torr, and the target was presputtered for 10 min in Ar gas. The flow rate of Ar gas was 24 sccm, and that of the N_2 gas was 4.8 sccm; the deposition rate of the WN_X films was 2.4 nm/min. The sputtering was performed at 200 W dc power with a total pressure of 7.6×10^{-3} torr. The thickness of the WN_X film deposited was 40 nm. After sputtering deposition, the Cu–WN_X–Au and Cu–WN_X–SiN multilayer structures were annealed for 30 min at different temperatures in nitrogen ambient for material analysis. Scanning electron microscopy (SEM), X-ray diffraction (XRD), Auger electron spectroscopy (AES), and sheet resistance were used for phase identification and the study of the interfacial reactions.

The second part is the copper metallized HBT device fabrication using WN_X as the diffusion barrier and the electrical performance evaluation of these devices. The InGaP–GaAs HBTs used in this work were grown by metal–organic chemical vapor deposition (MOCVD) on semi-insulating (100) GaAs substrates. The layer structure consists of (from bottom to top) a n^+-GaAs subcollector (500 nm, 4×10^{18} cm^{-3}), an n^--GaAs collector (700 nm, 2×10^{16} cm^{-3}), a p^+-GaAs base (83 nm, 3×10^{19} cm^{-3}), an n-InGaP emitter (50 nm, 3×10^{17} cm^{-3}), and an n^+-GaAs cap (200 nm, 3×10^{18} cm^{-3}). The HBT devices were fabricated using a standard triple mesa process. The InGaP and GaAs layers were etched by HCl–H_3PO_4 and H_3PO_4–H_2O_2–H_2O solutions, respectively. Alloyed AuGe–Ni–Au, nonalloyed Pt–Ti–Pt–Au, and alloyed AuGe–Ni–Au ohmic metal systems were used for the emitter, base, and collector contacts, respectively. Device passivation was realized with PECVD silicon nitride. After opening the connect via on the nitride film, the diffusion barrier WN_X (40 nm), interconnect Cu (400 nm) metal, and WN_X (10 nm) were sequentially deposited by dc-magnetron reactive sputtering through the collimator over patterned resist. The bulk of the resist and metal were then removed by a wet solvent lift-off process, followed by a high-pressure deionized (DI) water rinse to remove the residues. The top layer WN_X served as a protective layer to prevent Cu film oxidation. The dimension of the emitter area of the HBT was 3×20 μm. The HBTs with conventional Ti (50 nm)/Au (400 nm) interconnect metal were also prepared for comparison. The structure of the InGaP–GaAs HBTs in this study is shown in Fig. 1. The dc current–voltage (*I–V*) characteristics of the HBT devices were measured by HP4142B. Both the 3×20 μm emitter area HBT devices with gold interconnects and the devices with copper interconnects were stressed using current accelerated test and high temperature thermal annealing test for reliability evaluation and comparison. The high current test was performed at high current density of 140 kA/cm^2 for 55 h. The thermal test were carried out by annealing at 250 °C for 25 h in nitrogen ambient.

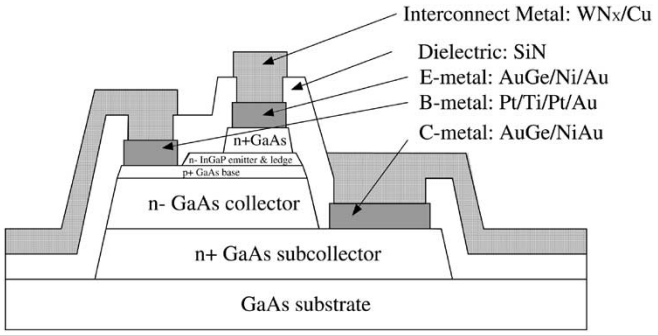

Fig. 1. Cross section of the InGaP–GaAs HBT with interconnect Cu metallization.

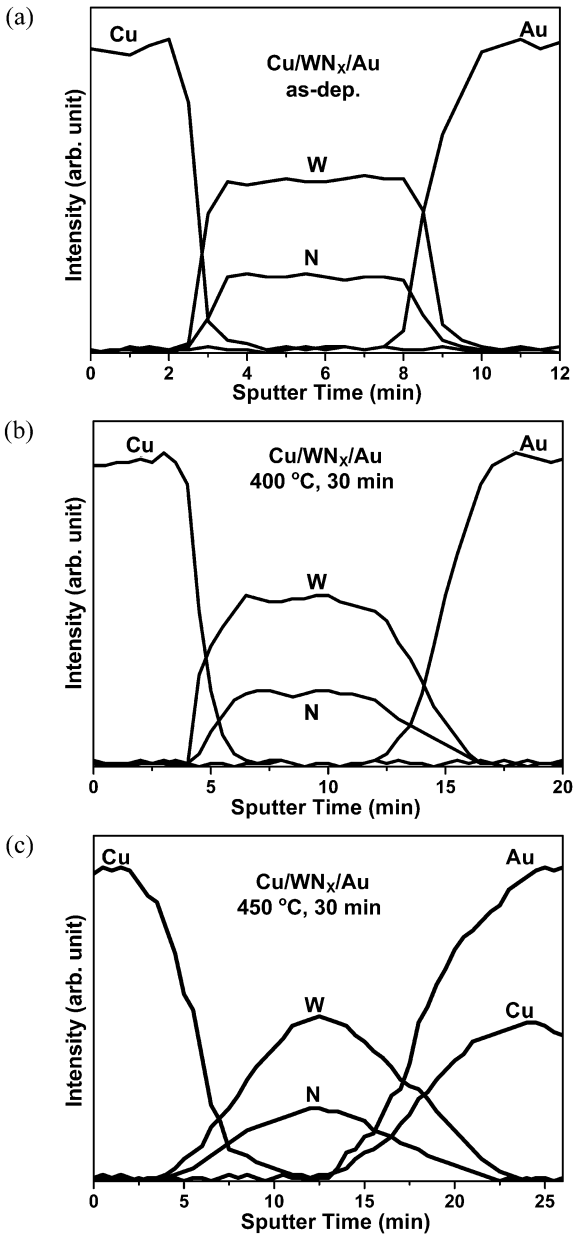

Fig. 2. AES depth profiles of the Cu–WN_X–Au samples (a) as deposited, (b) after 400 °C annealing, and (c) after 450 °C annealing.

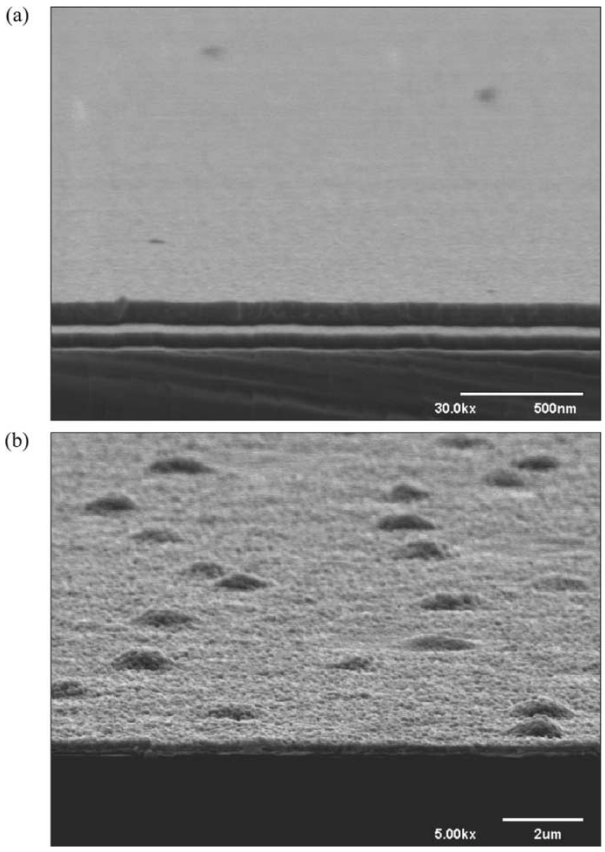

Fig. 3. SEM images of the Cu–WN_X–Au samples (a) as deposited and (b) after 450 °C annealing.

III. Material Stability of the Diffusion Barrier

There are two WN_X-based multilayer structures (Cu–WN_X–Au and Cu–WN_X–SiN–GaAs) in the copper metallized HBTs, as shown in Fig. 1 The stability of these material systems have to be studied before applying them to the device fabrication. The stabilities of these material systems were studied using SEM, AES, XRD and sheet resistances analyzes. The first multilayer structure studied was Cu–WN_X–Au. Fig. 2 shows the AES depth profiles of the Cu–WN_X–Au samples as-deposited and after 400 °C and 450 °C annealing for 30 min. As can be seen from Fig. 2(b), there is no atomic inter-diffusion between Cu and Au after 400 °C annealing. However, after 450 °C annealing for 30 min, the results in Fig. 2(c) show that copper started to diffuse into the gold layer. The SEM micrographs of the surface morphologies of the Cu–WN_X–Au samples as-deposited and after 450 °C annealing are shown in Fig. 3. As can be seen in Fig. 3(a), the surface morphology for the as-deposited sample is very smooth; however, after 450 °C 30 min annealing, the surface morphology started to change and became very rough due to material inter-diffusion and new phase formation as shown in Fig. 3(b). Additional evidence was obtained from the XRD analysis. Fig. 4 shows the XRD results of the Cu–WN_X–Au samples as-deposited and after annealing from 350 °C to 450 °C for 30 min. From the XRD data, it is clear that the diffraction peaks of Au, Cu, and W_2N remained unchanged after 400 °C annealing, suggesting that the Cu–WN_X–Au structure was still quite stable after 400 °C

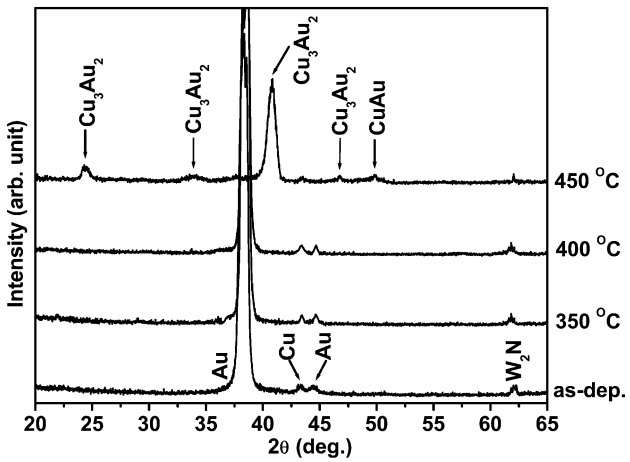

Fig. 4. XRD patterns of the Cu–WN_X–Au samples as deposited and after annealing at various temperatures.

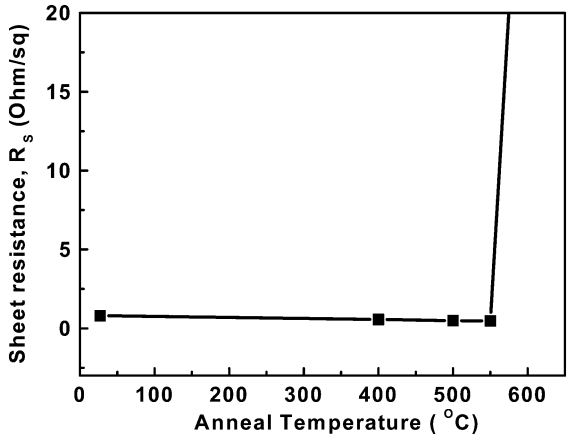

Fig. 5. Sheet resistance of the Cu–WN_X–SiN–GaAs samples as deposited and after annealing at various temperatures.

annealing. However, after 450 °C annealing, additional peaks which were identified as Cu_3Au_2 and CuAu diffraction peaks were found. The formation of Cu_3Au_2 and CuAu after 450 °C annealing suggested that Cu atoms had diffused through the WN_X layer into the Au layer.

The second multilayer structure studied was Cu–WN_X–SiN–GaAs. Fig. 5 shows the sheet resistances of the samples as-deposited and after 400 °C to 600 °C annealing for 30 min. The sheet resistance of the Cu–WN_X–SiN–GaAs film structure decreased after annealed at 400 °C–550 °C, which is probably due to the grain growth and the decrease of the defect density in the Cu and WN_X films after thermal annealing. After 600 °C annealing, the sheet resistance drastically increased, suggesting that atomic diffusion and inter-atomic reactions had occurred between these layers. Additional evidence showing that the Cu–WN_X–SiN–GaAs multiple layer was stable up to 550 °C annealing was obtained from the AES depth profile analysis data shown in Fig. 6. Fig. 6(a) is data of the as deposited films, and Fig. 6(b) is the data of these films after 550 °C 30 min annealing. As can be seen from Fig. 6(b), there is no noticeable diffusion of Cu into the SiN layer after annealing at 550 °C for 30 min. However, after 600 °C

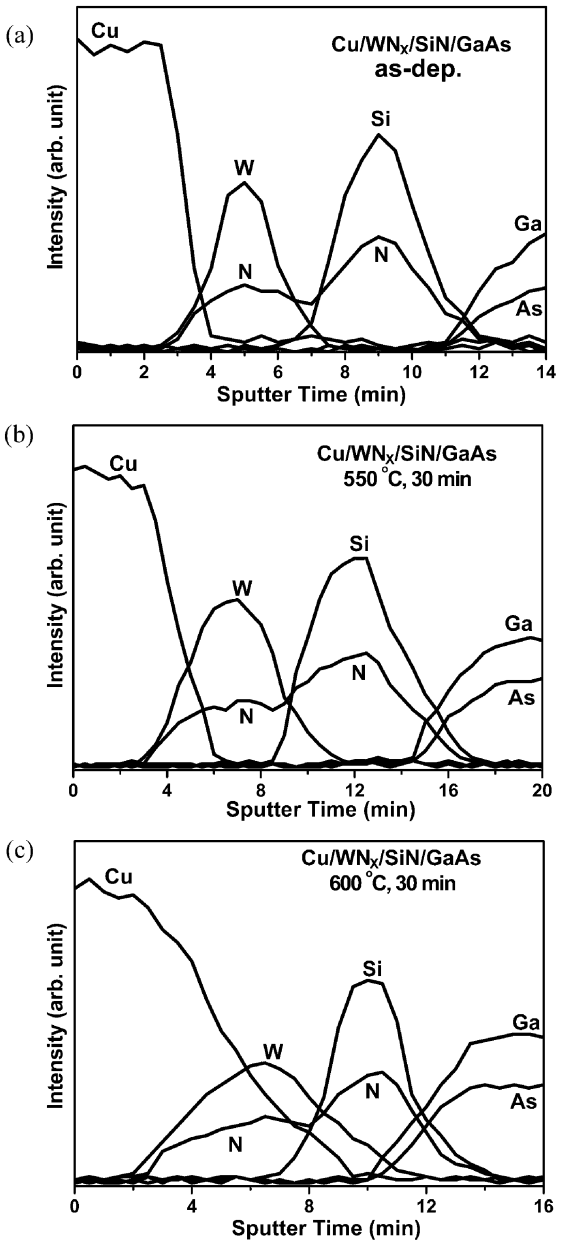

Fig. 6. AES depth profiles of the Cu–WN_X–SiN–GaAs samples (a) as-deposited, (b) after 550 °C annealing, and (c) after 600 °C annealing.

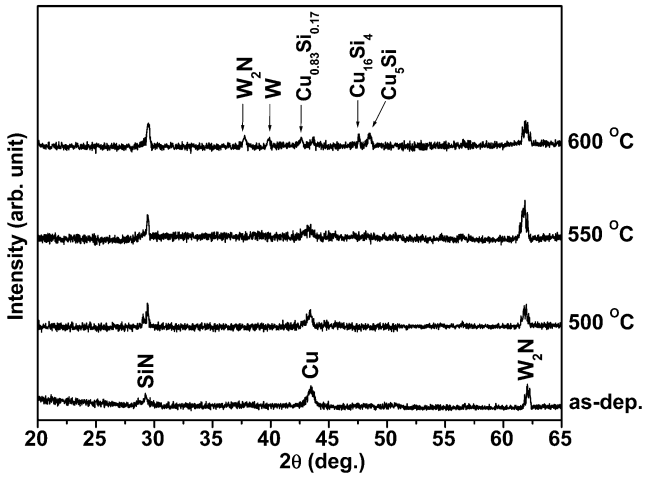

Fig. 7. XRD patterns of the Cu–WN_X–SiN samples as deposited and after annealing at various temperatures.

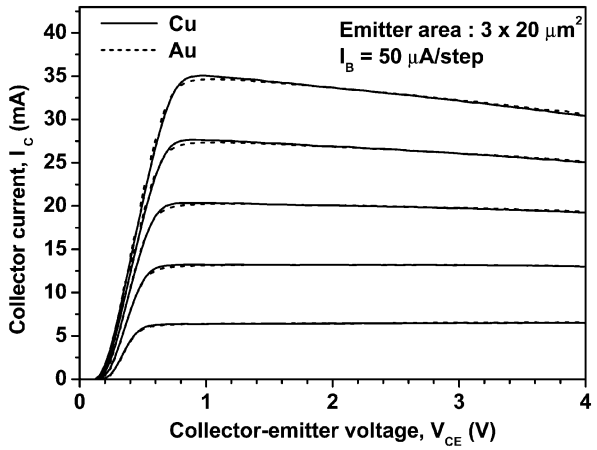

Fig. 8. Comparison of the typical $I_C - V_{\rm CE}$ characteristics for the emitter area ($3 \times 20\ \mu{\rm m}^2$) HBTs with Cu and with Au interconnect metallization.

annealing for 30 min, Cu atoms started to diffuse through the WN_X layer into the SiN layer as can be seen in Fig. 6(c). In addition, Fig. 7 shows the XRD results of the Cu–WN_X–SiN samples as-deposited and after annealed from 500 °C to 600 °C for 30 min. The XRD data clearly show that the peaks of Cu, W_2N, and SiN remained unchanged up to 550 °C annealing, indicating that the Cu–WN_X–SiN structure remained quite stable up to 550 °C. After annealing at 600 °C, peaks from new phases of $Cu_{0.83}\ Si_{0.17}$, $Cu_{16}Si_4$, Cu_5Si, W, and W_2N were identified, suggesting that the reactions between the SiN and the Cu metallization layer had occurred. From the data shown above, it is clear that the Cu–WN_X–Au material system is quite stable up to 400 °C annealing, and the Cu–WN_X–SiN material system is quite stable up to 550 °C annealing.

IV. Device Electrical Characteristics

WN_X diffusion barrier was applied to the InGaP–GaAs HBTs with interconnect copper metallization. InGaP–GaAs HBTs with traditional Ti–Au based interconnect was also processed on half of the same wafer for comparison. The Au thickness for the Au interconnects is the same as the Cu thickness of the Cu interconnects (400 nm). Fig. 8 shows the typical common emitter characteristics for the small emitter area ($3 \times 20\ \mu{\rm m}^2$) HBTs; in this figure, one curve is for the HBT with Cu metallized interconnects and WN_X diffusion barrier, and the other curve is for the HBT with Au metallized interconnects. From Fig. 8, these two devices show similar knee voltage and offset voltage, which indicates that there is no stress effect for the WN_X–Cu–WN_X films, and the quality of the multilayer materials is quite good. The common emitter current gain β was around 140 for both cases. Gummel plots of the HBTs with Cu and Au interconnect metallization were also compared. The results are shown in Fig. 9. The two HBTs show similar behavior, but the HBT with Cu interconnect metal shows slightly higher base and collector currents than the HBT with Au interconnect metal in the high current and high base–emitter voltage region.

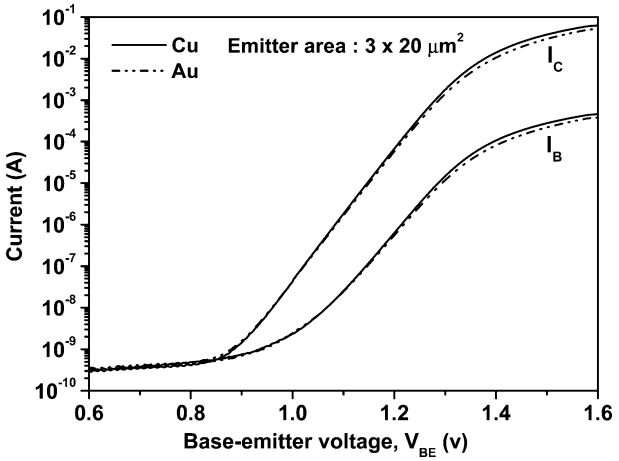

Fig. 9. Comparison of the Gummel plots for the emitter area ($3 \times 20\ \mu\text{m}^2$) HBT with Cu and with Au interconnect metallization.

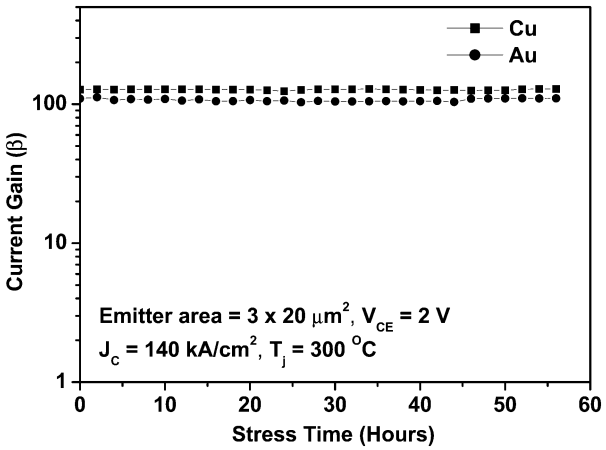

Fig. 10. Current gain as a function of the stress time at a constant I_B for the emitter area ($3 \times 20\ \mu\text{m}^2$) HBTs with Cu and Au interconnect metallization.

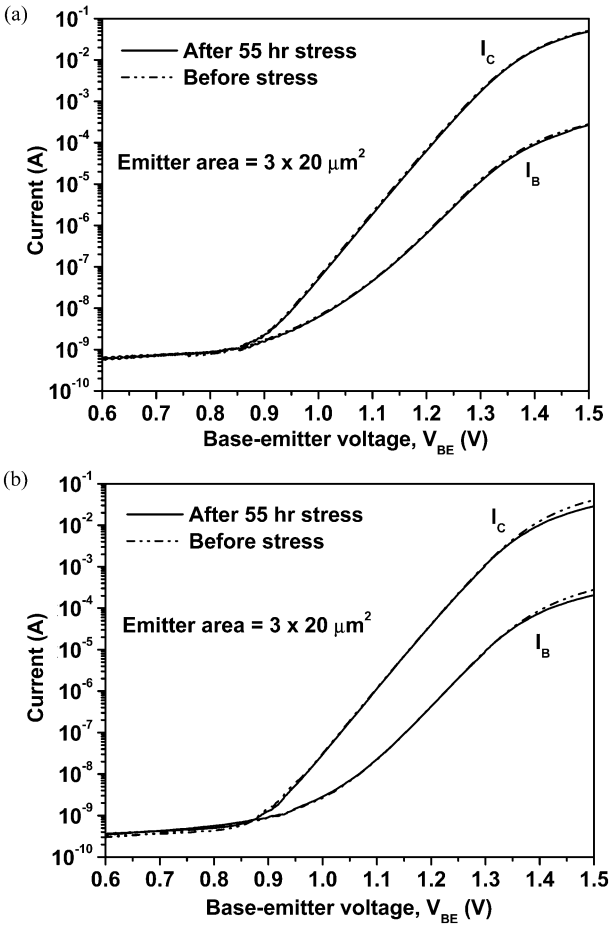

Fig. 11. Gummel plots measured before and after 55-h current-accelerated stress test with high current density of 140 kA/cm^2 for the emitter area $3 \times 20\ \mu\text{m}^2$ HBT devices (a) with Cu interconnect metallization and (b) with Au interconnect metallization.

To test the reliability of the WN_X as the diffusion barrier for the Cu metallized HBTs, both copper and gold metallized HBTs with $3 \times 20\ \mu$m emitter area were subjected to current accelerated stress test with high current density of 140 kA/cm^2. It was much higher than 25 kA/cm^2 required for normal device operation, the purpose is to shorten the stress time so that the stress tests could be performed at wafer level without using any package, and the results could be obtained in a few hours [13]. Fig. 10 plots the current gain (β) of the two kinds of HBTs after stressed at the high current density of 140 kA/cm^2 at V_{CE} of 2 V for a period of 55 h. Under this test condition, the estimated junction temperature T_j was about 300 °C. Both measurements were made at an ambient room temperature of $T_{\text{A}} = 25$ °C. Fig. 11 shows the typical Gummel plots before and after the current accelerated stress. It can be seen from Fig. 11(a) that the Cu metallized HBT device showed only very little change after stress test, and the current gain was still higher than 100 after the stress. Also, almost no significant change in the base and collector ideality factors and no shift in the turn-on voltage were observed. Besides, the collector current (I_C) change was around 3% at 25 kA/cm^2 after the current accelerated stress for the Cu metallized HBT. On the other hand, the emitter and base current of the Au metallized HBT show significant degradation at high base–emitter voltage, as can be seen from Fig. 11(b). The change in the collector current at 25 kA/cm^2 was around 20%. It was caused by the increase in the emitter resistance after an accelerated stress test. This may due to the fact that the heat dissipation of the Cu metallized HBT is better than that of the Au metallized HBT, so the ohmic structure of the Au metallized HBT is easier to degrade during current accelerated stress. This phenomenon was not found for the Cu metallized HBTs.

To study the thermal stability of the WN_X diffusion barrier, the $3 \times 20\ \mu$m emitter area HBTs with Cu metallization were annealed at 250 °C for 25 h and tested for the electrical performance. For comparison, the Au metallized HBTs were also annealed at the same conditions and tested. Fig. 12(a) shows the common emitter *I–V* curves before and after annealing for the copper metallized HBT with WN_X diffusion barrier, and Fig. 12(b) shows the corresponding common emitter *I–V* curves before and after annealing for the gold metallized HBT. As can be seen from the data of Fig. 12, there was no change in the offset voltage, knee voltage, and saturation current after annealing for both types of HBTs. It is suggested that there was no ohmic degradation and copper diffusion for the copper metallized HBTs using WN_X as the diffusion barrier. Fig. 13 shows the Gummel plots before and after 250 °C 25-h annealing for both the copper metallized and gold metallized devices. The

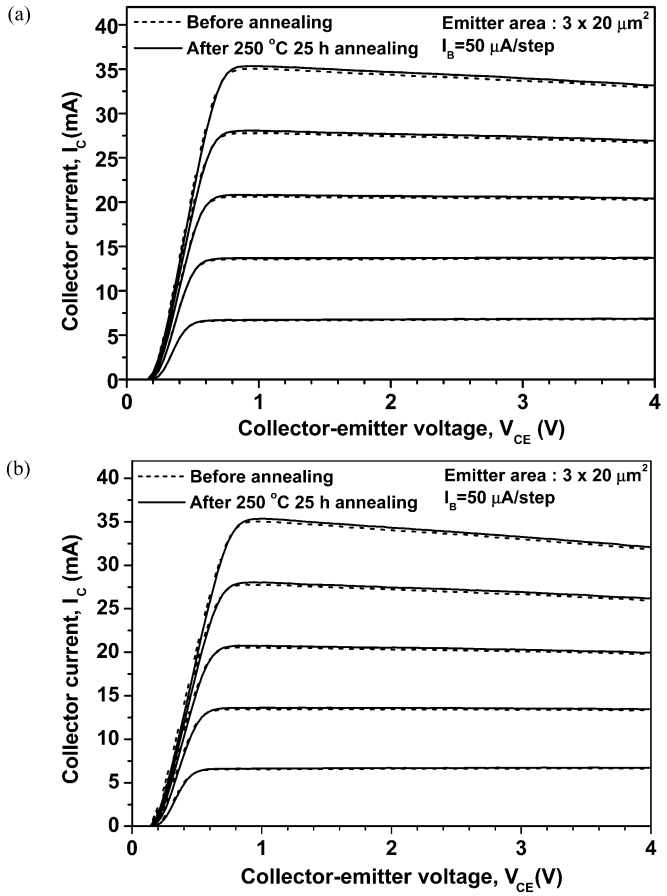

Fig. 12. Common emitter *I–V* curves measured before and after 250 °C 25-h annealing for the emitter area $3 \times 20\ \mu\text{m}^2$ HBT devices (a) with Cu interconnect metallization and (b) with Au interconnect metallization.

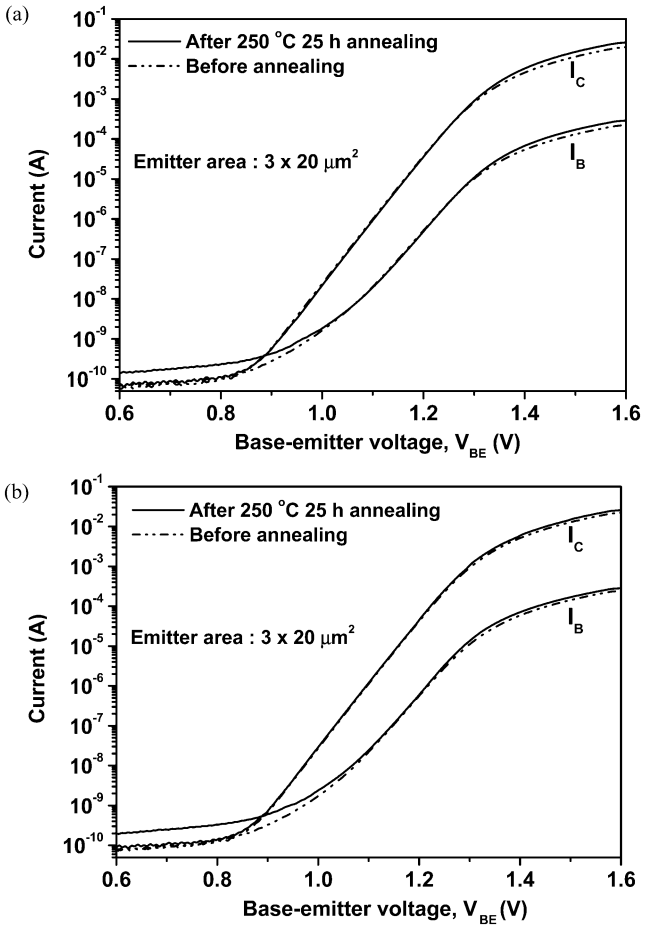

Fig. 13. Gummel plots measured before and after 250 °C 25-h annealing for the emitter-area $3 \times 20\ \mu\text{m}^2$ HBT devices (a) with Cu interconnect metallization and (b) with Au interconnect metallization.

base and collector ideality factors for both HBTs showed little change after the thermal annealing and the base leakage current of the two types of devices remained in the same order. It suggested that no additional degradation mode had occurred and that no copper diffusion into the active device region after the thermal stress, these results are consistent with the material analysis results.

V. Conclusion

Use of WN_X as the diffusion barrier for the interconnect copper metallization of InGaP–GaAs HBTs is reported for the first time. In this paper, InGaP–GaAs HBTs with Cu–WN_X metallization layers were fabricated, and the electrical performance was evaluated. From SEM, XRD, and AES depth profiles and sheet resistance studies, the Cu–WN_X–Au and Cu–WN_X–SiN metallization layers were very stable after annealing at 400 °C and 550 °C, respectively. After applying the Cu–WN_X metallization layers to the HBTs, the common emitter *I–V* curves of these copper-metallized HBTs showed similar electrical characteristics as those for HBTs metallized with conventional Ti–Au layers. Both a current-accelerated stress test (140 kA/cm^2 stress for 55 h) and a thermal stress test (annealing at 250 °C for 25 h) were performed on the Cu–WN_X metallized HBTs, and almost no change in the electrical characteristics were observed for these devices after the tests. The results show that the Cu–WN_X interconnect layers are quite stable and that WN_X can be used as the diffusion barrier for the interconnect copper metallization for the InGaP–GaAs HBTs.

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