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Improved subthreshold slope method for precise extraction of gate capacitive coupling coefficients in stacked gate and source-side injection flash memory cells

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Abstract

Existing subthreshold slope methods are shown to be far from accurate in extracting gate capacitive coupling coefficient α_G in stacked gate flash memory cells. The origin of the error is systematically identified: (i) process variations induced mismatch and (ii) underlying bulk capacitive coupling. To alleviate such drawbacks, a new version of the subthreshold slope method at room temperature is established: $\alpha_G = 0.06(n_f - \alpha_B)/s_f$, where the subthreshold swing s_f is from flash memory cells, the subthreshold slope factor n_f is from dummy transistors via threshold voltage against source-to-substrate bias measurement, and the bulk coupling coefficient α_B is from a linear extension of the dimensional dependencies in the literature. The resulting α_G of around 0.55 again agrees consistently with those dependencies and once drain and source coupling experiment is performed, the relation of $\sum \alpha_i \approx 1$ is achieved for all involved coupling coefficients α_i's.

The sidewall source-side injection flash memory cells are also investigated. With the improved method, this manufacturing process is proved free of process variations issue and is characterized with α_G of 0.374 and fringing capacitance of 0.204 fF.

Keywords: Capacitive coupling; Flash memory; Mismatch; MOSFETs; Process variations; Subthreshold

1. Introduction

Capacitive coupling coefficients are well recognized as a very important device parameter in flash memory cells, among which the most key is gate coupling coefficient α_G. The α_G determines how fast the programming and erasure actions can reach. Thus, precise extraction of α_G in a flash memory manufacturing process is essential. So far, a great number of works devoted to stacked gate flash memory cells have been published [1–11]. In such kind of structures, a pair of test vehicles (i.e., flash memory cells and dummy transistors) [1–8] or even a single memory cell with accompanying sophisticated measurements and procedures [9–11] were exploited. There in turn were plenty of distinct extraction schemes reported, depending upon the regions of operation adopted: subthreshold [1–3], inversion [6–9], and accumulation [10,11]. In addition, the threshold voltage ratio method was also devised [4,5]. However, only the subthreshold slope ratio method and the threshold voltage ratio method [1,4,5] were widely utilized in the industry. There are two plausible reasons to favor both methods. First, the inversion and accumulation schemes relied on complicated measurement set-ups and time-consuming analysis procedures, failing to meet fast extraction

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requirements in a flash memory manufacturing process. Second, the inversion and accumulation schemes involved two or more linear equations; however, potential uncertainties may be introduced when simultaneously solving equations as thoroughly interpreted in [12]. On the other hand, α_G extraction in split-gate and source-side injection cells received relatively little attention [13,14]. Even the threshold voltage ratio method is unable to handle the case of source-side injection. The reason is that long-time UV (ultra-violet) erasure for satisfying precondition of a zero charge on floating gate is improbable to realize for source-side injection structure in this work.

The work is dedicated to a 0.35-μm stacked gate flash memory manufacturing process and a 0.25-μm sidewall source-side injection flash memory process. Obviously, only the subthreshold slope ratio method is potentially suitable for both processes. However, existing subthreshold slope methods [1–3] inadequately deal with one or two of the following vital aspects: process variations [2,3] and bulk capacitive coupling [1], and thus need further substantial improvements.

2. Existing and new subthreshold slope methods

2.1. Subthreshold swing ratio method (SS)

The subthreshold swing ratio method yields α_G in terms of subthreshold swing s_d of dummy transistor divided by subthreshold swing s_f of flash memory cell:

$$\alpha_G = s_d/s_f \tag{1}$$

Despite widely utilized in the industry, the SS method is essentially inaccurate due to lack of bulk capacitive coupling [1]. The precision of the method may further be deteriorated by process variations induced current mismatch between flash memory cell and dummy transistor, which becomes more prominent if biased in subthreshold [15–18]. Actually, ignoring the role of bulk coupling as in (1) has produced a severe error of about 0.2 in a 0.8-μm EPROM process [1]; and the process variations induced error as large as 0.13 has been encountered in a 0.35-μm flash memory process [2].

2.2. Subthreshold swing ratio method involving bulk coupling (SSB) [1]

Wong et al. [1] extended (1) to account for bulk capacitive coupling at room temperature:

$$\alpha_G = s_d/s_f - 0.06\alpha_B/s_f \tag{2}$$

where α_B is the bulk capacitive coupling coefficient. Two extra experiments via drain coupling and source coupling were then carried out to relate α_G to corresponding drain coupling coefficient α_D and source coupling coefficient α_S, respectively. Consequently, α_B was obtained by forcing the ideal relationship of $\sum \alpha_i = 1$ as an auxiliary equation, namely $\alpha_B = 1 - \alpha_G - \alpha_D - \alpha_S$. Unfortunately, the SSB method was recently demonstrated [2] to be sensitive to process variations issue. Even in some cases the extracted α_B was accompanied with a negative sign [2], which is apparently unreasonable physically.

2.3. Process-variation-immunity method (PVI) [2]

To mitigate the effect of process variations, a process-variation-immunity method was devised [2]. In this method, the control gate voltage shift under weak body effect [2] is measured in flash memory cells in subthreshold, while the corresponding subthreshold slope factor is adequately deduced from the threshold voltage versus source-to-substrate bias measurement in dummy devices. Then by incorporating drain and source coupling experiments into equations, three coupling coefficients $(\alpha_G, \alpha_D, \alpha_S)$ can all be solved simultaneously. However, the role of α_B has not been clarified fully yet.

2.4. New method

To alleviate above drawbacks, we replace (2) with a new version [3]:

$$\alpha_G = 0.06(n_f - \alpha_B)/s_f \tag{3}$$

where n_f is the subthreshold slope factor measured from threshold voltage against source-to-substrate voltage in dummy transistor [2]. The α_B in (3) is from a linear extension of the dimensional dependencies recently drawn by Larcher et al. [12] from a comprehensive simulation study. Table 1 lists such dependencies [12] comprising bulk coupling coefficient α_{B0} and gate coupling coefficient α_{G0} corresponding to specific channel width W_0 and length L_0, as well as the dimension dependent factors $(d\alpha_i/dW, d\alpha_i/dL)$ corresponding to a floating gate width W_{FG} of 0.65 μm. The linear expressions involving different combinations of channel width W and length L are thereby written as

Table 1
Simulated gate and bulk capacitive coupling coefficients and their dimensional dependencies [12]

W_0	0.25 μm
L_0	0.4 μm
α_{B0}	0.1
α_{G0}	0.675
$d\alpha_B/dW$	0.27 μm^{-1}
$d\alpha_B/dL$	0.22 μm^{-1}
$d\alpha_G/dW$	−0.96 μm^{-1}
$d\alpha_G/dL$	0.29 μm^{-1}

$$\alpha'_B = \alpha_{B0} + (W - W_0)\mathrm{d}\alpha_B/\mathrm{d}W + (L - L_0)\mathrm{d}\alpha_B/\mathrm{d}L \quad (4)$$

$$\alpha'_G = \alpha_{G0} + (W - W_0)\mathrm{d}\alpha_G/\mathrm{d}W + (L - L_0)\mathrm{d}\alpha_G/\mathrm{d}L \quad (5)$$

The symbols α'_B and α'_G, respectively, represent bulk and gate capacitive coupling coefficients under the same W_{FG} (i.e., 0.65 μm) [12]. In the case of varying W_{FG}, which means a corresponding change in the total capacitance, according to layout pattern consideration we can readily extend (4) to

$$\alpha_B = \alpha'_B[1 - \alpha'_G + (W_{FG}/0.65\ \mu\mathrm{m})\alpha'_G]^{-1} \quad (6)$$

Once α_B in (6) and subsequently α_G in (3) are got, drain and source coupling experiments straightforwardly produce α_D and α_S.

It is needed to address the validity of the method. First of all, one can sum up above four coupling coefficients α_i to see whether the relationship $\sum \alpha_i = 1$ is met. Then one can compare extracted α_G with that from the extension of (5):

$$\alpha_G = \alpha'_G(W_{FG}/0.65\ \mu\mathrm{m})[1 - \alpha'_G + (W_{FG}/0.65\ \mu\mathrm{m})\alpha'_G]^{-1} \quad (7)$$

The aim is to see whether a coincidence is turned out consistently between the two.

3. Stacked gate structure: results and discussion

The NOR-type stacked gate flash memory cells were manufactured in a 0.35-μm process technology. The tunnel oxide thickness was 100 Å; the gate width and length were 0.45 and 0.4 μm, respectively; and the floating gate width W_{FG} was 0.85 μm. Fig. 1 schematically shows cross-section of device under test. According to capacitance model in Fig. 1, the floating gate voltage V_{FG} is given by [5]

$$V_{FG} = \alpha_G V_{CG} + \alpha_D V_D + \alpha_S V_S + \alpha_B \phi_S + Q_{FG}/C_T \quad (8)$$

where V_{CG}, V_D, and V_S are biases applied to control gate, drain, and source, respectively; ϕ_S is the silicon surface potential; Q_{FG} is the charge on the floating gate; and C_T is the sum of the control gate to floating gate capacitance (C_{CF}), drain to floating gate capacitance (C_{DF}), source to floating gate capacitance (C_{SF}), and silicon surface to floating gate capacitance (C_{BF}). The corresponding coupling coefficients are thereby defined as $\alpha_G = C_{CF}/C_T$, $\alpha_D = C_{DF}/C_T$, $\alpha_S = C_{SF}/C_T$, and $\alpha_B = C_{BF}/C_T$. The dummy transistors were also formed; that is, the identically drawn flash memory cells but with control gate shorted to underlying floating gate.

Fig. 2 shows the measured drain currents versus V_{CG} in flash memory cell and V_{FG} in dummy transistor for three different locations on wafer. The corresponding subthreshold swings s_f and s_d are listed in Table 2. The slope factor n_f was measured from threshold voltage V_{TH} against source-to-substrate bias V_{SB} in dummy transistors under weak body effect, as depicted in Fig. 3 for the "Middle" position of the wafer. Both schemes for determination of V_{TH}, namely the maximum transconductance extrapolation and the constant current forcing, were found to produce almost the same results. From Fig. 3, n_f equals $1 + (V_{TH2} - V_{TH1})/0.1$ V, where V_{TH1} and V_{TH2} are threshold voltages of dummy transistor at $V_{SB} = 0$ and 0.1 V, respectively. Fig. 4 depicts threshold voltage versus source-to-substrate voltage for different die positions on wafer. The corresponding n_f values are given in Table 2. During flash memory cells measurements, applied biases were very small in magnitude (i.e., $V_D = 0.1$ V, $V_{SB} = 0.1$ V) and V_{CG} was carefully swept with the aim to ensure that Q_{FG} in floating gate remains considerably unchanged, as judged by monitoring of threshold voltage and subthreshold swing. On the other

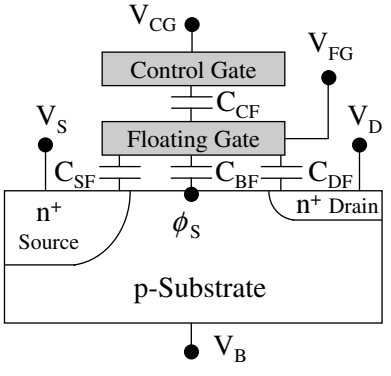

Fig. 1. Schematic cross-section of a stacked gate flash memory cell. During subthreshold slope measurement, $V_S = V_B = 0$ V, and $V_D = 0.1$ V.

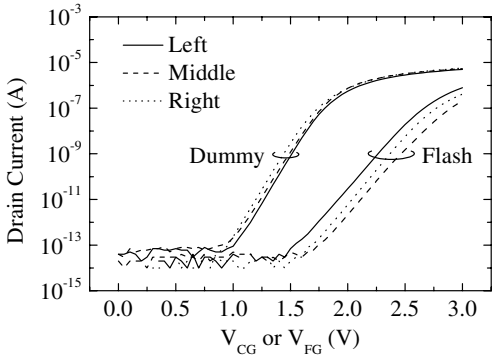

Fig. 2. Drain current measured at three locations on wafer for stacked gate cells, versus control gate voltage (V_{CG}) in flash memory cell and floating gate voltage (V_{FG}) in dummy transistor. The subthreshold swings of flash memory cell (s_f) and dummy transistor (s_d) can be extracted accordingly.

Table 2
Extracted values of subthreshold swing and subthreshold slope factor in three stacked gate cell dies

Sample location	Subthreshold parameter		
	s_f (mV/dec)	s_d (mV/dec)	n_f
Left	174	120	1.67
Middle	170	127	1.74
Right	165	125	1.68

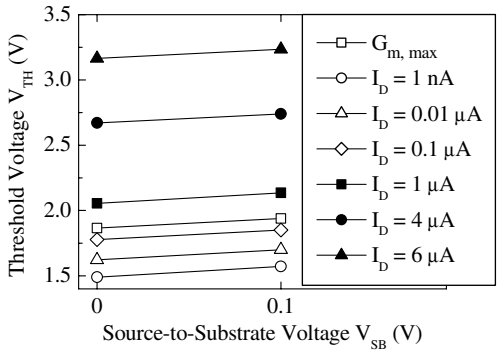

Fig. 3. Extracted threshold voltage V_{TH} of dummy transistor versus source-to-substrate voltage V_{SB} for the position "Middle". A very small standard deviation of 0.01 for α_G was produced between the maximum transconductance extrapolation method and the constant current forcing method. Thus, the maximum transconductance extrapolation method was employed throughout the work.

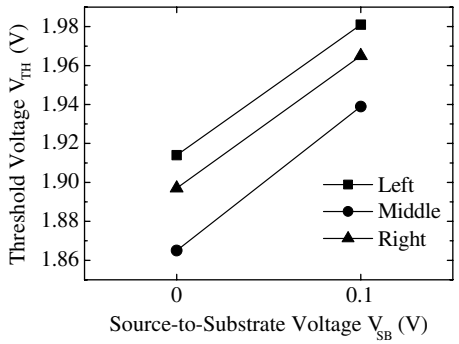

Fig. 4. Extracted threshold voltage V_{TH} of dummy transistor versus source-to-substrate voltage V_{SB}, demonstrating the slope factor (n_f) extraction procedure for three different locations on wafer.

hand, the slope factor n_f values were found to agree closely with that from $n_f = 1 + C_{dep}/C_{ox}$ [18], where C_{dep} and C_{ox} are the silicon depletion capacitance per unit area and the tunnel oxide capacitance per unit area, respectively.

As to bulk coupling coefficient α_B, it was calculated to be 0.134 from (4)–(6). Then the values of α_G were turned out via (3) as plotted in Fig. 5 for three positions. The subsequent experiments via drain and source coupling further yielded α_D and α_S again plotted together in Fig. 5. The corresponding $\sum \alpha_i$ was found to be 0.986, 1.054, and 1.038 for the Left, Middle, and Right position, respectively, indicating that $\sum \alpha_i \approx 1$. The second evidence to confirm the validity of the method is $\alpha_G = 0.55$ stemming from (7). Once we place it on the figure, surprisingly it lies in the close proximity of α_G from the new method. Therefore, it is argued that the proposed method is consistent with the published dimensional dependencies in subthreshold mode [12].

Comparison with the other methods (SS, SSB, and PVI) is displayed in Fig. 6 concerning α_G extraction accuracy. This figure clearly reveals the impact of process variations and bulk capacitive coupling. First of all, the error in the SSB or SS method far exceeds the PVI or improved method. This means that process variations prevail in SSB and SS methods. Second, the SSB method produces larger error than SS method. This is attributed to inadequate determination of α_B in SSB method. In other words, underlying bulk capacitive coupling is not dealt with correctly in SSB method. Third, the PVI method is less precise relative to the new method. This is

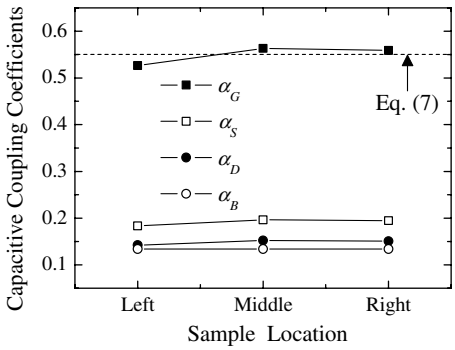

Fig. 5. Four capacitive coupling coefficients of stacked gate cells determined by the new method for three different locations on wafer. The dotted line from (7) is together plotted for comparison.

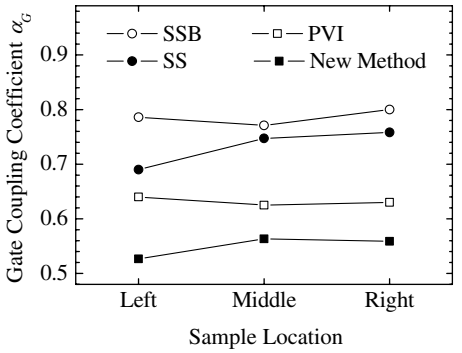

Fig. 6. Gate capacitive coupling coefficient α_G of stacked gate cells for three positions on wafer, determined by the different methods: subthreshold swing ratio (SS), subthreshold swing ratio including bulk coupling (SSB), process-variation-immunity (PVI), and the new one.

because bulk capacitance coupling is not taken into account in the PVI method.

4. Source-side injection structure: results and discussion

Fig. 7 depicts schematic cross-section view of a sidewall select-gate source-side injection (SSI) flash memory cell from a 0.25-μm manufacturing process. The tunnel oxide thickness was 100 Å, the select gate oxide and interpoly oxide (between select gate and floating gate) both were 170 Å thick, and the triple layer dielectric (oxide–nitride–oxide, ONO) between control gate and floating gate had an equivalent oxide thickness of 170 Å. The channel width W and length L were 0.225 and 0.298 μm, respectively; and the floating gate width W_{FG} was 0.594 μm. Relative to stacked gate counterpart in Fig. 1, there are two essential differences in the SSI cell. First, the left sidewall select gate and right sidewall select gate both provide extra couplings. Second, the right sidewall select gate, being preserved for purpose of fabrication convenience, is electrically shorted to the source. The source was defined the grounded junction during read-out for prevention of soft write after repeated read-out operations [13,19], while in the programming phase it was connected to a large bias ($V_S = 6$ V, for example) for creation of extra coupling potential. The dummy transistors were identically drawn flash memory cells with control gate shorted to floating gate.

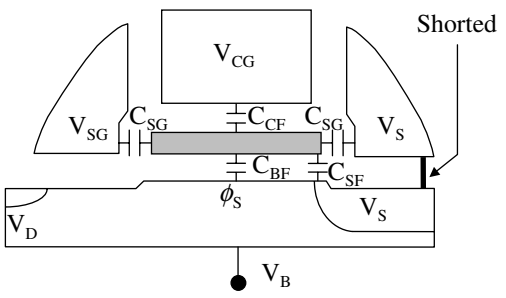

Fig. 7. Schematic cross-section view of a sidewall select-gate source-side injection flash memory cell.

According to capacitance model in Fig. 7, the floating gate voltage can be written as

$$V_{FG} = \alpha_G V_{CG} + \alpha_{SG} V_{SG} + (\alpha_{SG} + \alpha_S) V_S + \alpha_B \phi_S + Q_{FG}/C_T \quad (9)$$

where α_{SG} is the select gate coupling coefficient defined as select gate to floating gate capacitance C_{SG} divided by total capacitance C_T. However, C_T has a different definition from that in stacked gate structure, and it becomes $C_{CF} + 2C_{SG} + C_{SF} + C_{BF}$ to account for additional C_{SG}'s. Note that a small drain voltage of 0.1 V in this work does not constitute significant coupling to floating gate because of the existence of the adjacent select gate, which can effectively isolate the potential coupling [13]. Under the same operation of subthreshold conduction as stacked gate cells (i.e., $V_S = V_B = 0$ V, $V_D = 0.1$ V), the same expression, namely (3), can also be derived from (9). However, (6) has to be corrected in such a way to handle extra sidewall select gate elements:

$$\alpha_B = (1 - 2\alpha_{SG})\alpha'_B[1 - \alpha'_G + (W_{FG}/0.65\ \mu m)\alpha'_G]^{-1} \quad (10)$$

Then substituting (3) into (10), a comprehensive formulation is created for α_B:

$$\alpha_B = \left[1 - \left(\frac{0.12}{s_f}\right)\left(n_f - \frac{\alpha'_B}{1 - \alpha'_G + (W_{FG}/0.65\ \mu m)\alpha'_G}\right) \times \left(\frac{C_{SG}}{C_{CF}}\right)\right]\left(\frac{\alpha'_B}{1 - \alpha'_G + (W_{FG}/0.65\ \mu m)\alpha'_G}\right) \quad (11)$$

Fig. 8 shows the measured drain current versus control gate voltage in SSI flash memory cell and floating gate voltage in its dummy transistor, giving $s_f = 236$ mV/dec and $s_d = 95$ mV/dec, and $n_f = 1.543$ was obtained from threshold voltage versus source-to-substrate bias measurement in dummy transistor. With $W = 0.225$ μm and $L = 0.298$ μm, α'_B and α'_G were calculated to be 0.0708 and 0.6694, respectively. $C_{SG} = 0.077$ fF and $C_{CF} = 0.352$ fF both were drawn from SEM (scanning electron microscope) pictures using a parallel-plate capacitance approximation. As a result of substituting these values into (11), $\alpha_B = 0.063$, which in turn yields $\alpha_G = 0.374$ by (3).

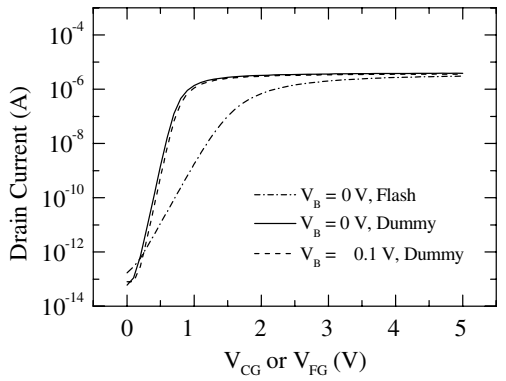

Fig. 8. Drain current measured versus control gate voltage (V_{CG}) in source-side injection flash memory cell and floating gate voltage (V_{FG}) in dummy transistor. The subthreshold swings of flash memory cell (s_f) and dummy transistor (s_d) are 236 and 95 mV/dec, respectively; and the slope factor (n_f) of dummy transistor is 1.543.

The total capacitance C_T consists of the parallel-plate component ($=0.737$ fF) and the fringing component C_{FRG} near the source [4,12]. This leads to $C_{FRG} = 0.204$ fF for $\alpha_G = 0.374$, which is reasonable compared with the range of the fringing capacitance in [12]. On the other hand, using the same α_B ($= 0.063$) from the new subthreshold slope method as input to (2), the resulting α_G is 0.387, quite close to that from the new method. This indicates relatively insignificant mismatch between SSI cell and dummy device. Therefore, the underlying manufacturing process is considerably free of process variations issue.

5. Conclusions

Existing subthreshold slope methods are shown to be inaccurate due to process variations induced mismatch and underlying bulk capacitive coupling. These drawbacks are substantially removed in the new method, achieved in terms of threshold voltage versus source-to-substrate bias measurement in dummy transistors and a linear extension of the published dimensional dependencies for bulk coupling coefficient. The proposed method is practically demonstrated in a 0.35-μm stacked gate flash memory manufacturing process and a 0.25-μm sidewall source-side injection flash memory manufacturing process.

Acknowledgements

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Appendix A. A list of symbols

Symbol	Description	Unit
α_B, α_{B0}, α'_B	Bulk capacitive coupling coefficient	(–)
α_D	Drain capacitive coupling coefficient	(–)
α_G, α_{G0}, α'_G	Gate capacitive coupling coefficient	(–)
α_S	Source capacitive coupling coefficient	(–)
α_{SG}	Select gate capacitive coupling coefficient	(–)
C_{BF}	Silicon surface to floating gate capacitance	(F)
C_{CF}	Control gate to floating gate capacitance	(F)
C_{dep}	Silicon depletion capacitance	(F/m^2)
C_{DF}	Drain to floating gate capacitance	(F)
C_{FRG}	Fringing capacitance near the source side	(F)
C_{ox}	Tunnel oxide capacitance	(F/m^2)
C_{SF}	Source to floating gate capacitance	(F)
C_{SG}	Select gate to floating gate capacitance	(F)
C_T	Total capacitance	(F)
ϕ_S	Silicon surface potential	(V)
L, L_0	Channel length of flash memory cell	(m)
n_f	Subthreshold slope factor	(–)
Q_{FG}	Floating gate charge	(C)
s_d	Subthreshold swing of dummy transistor	(V/decade)
s_f	Subthreshold swing of flash memory cell	(V/decade)
V_B	Applied substrate voltage	(V)
V_{CG}	Applied control gate voltage	(V)
V_D	Applied drain voltage	(V)
V_{FG}	Coupled floating gate voltage	(V)
V_S	Applied source voltage	(V)
V_{SB}	Source-to-substrate voltage	(V)
V_{TH1}	Threshold voltage of dummy transistor when $V_{SB} = 0$ V	(V)
V_{TH2}	Threshold voltage of dummy transistor when $V_{SB} = 0.1$ V	(V)
W, W_0	Channel width of flash memory cell	(m)
W_{FG}	Floating gate width of flash memory cell	(m)

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