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A new fabrication technique for silicon nanowires

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Abstract

A new method is proposed for fabricating silicon nanowires (SiNWs) on silicon substrates instead of on SOI wafers, providing a cheaper process; it also enables their electrical properties to be measured easily. Using scanning probe lithography, mask patterns for SiNWs were defined on a (1 1 0)-oriented bare silicon wafer. Subsequently silicon nitride spacers were produced and utilized to protect SiNWs during a dry-oxidation process, which was applied to isolate the SiNWs from the substrate. The field induced oxide mask patterns generated with a scanning probe microscope were around 50–60 nm in width, and SiNWs with 34 nm in width and 160 nm in height resulted after wet potassium hydroxide (KOH) orientation-dependent etching at 40° for 400 s. SiNWs with line width around 34 nm on the bare silicon wafer were achieved with the scanning probe lithography process and conventional IC processing.

Keywords: Silicon nanowires; Scanning-probe lithography; Orientation-dependent etching; Negative resistance

1. Introduction

Nanofabrication technologies and electric properties of nanometer-scale structures have been considered extensively in recent publications. silicon nanowire (SiNW) has been applied to electron devices with quantization results [1] and to biosensing devices with extremely high sensitivity to conductance [2]. There are two categories of fabrication technologies for SiNWs. The top-down methods use beam-based lithography like electron beams and ion beams, followed by reactive ion etch (RIE) [3,4] or use scanning probe lithography (SPL) and potassium hydroxide (KOH) orientation-dependent etching (ODE) [5], tetra-methyl ammonium hydroxide (TMAH) etching [6] to generate nanopatterns on SOI wafer. The second are bottom-up techniques usually utilizing Au particles as catalysts, with the SiNWs grown from CVD with SiH_4/He as precursors; the widths of SiNWs depending on growth temperature and pressure. Nanowires down to 10 nm have been achieved [7,8]. Recently, atomic force microscopy (AFM) [9–11] with low tip voltage (~10 V) under a controlled humidity environment has been used to oxidize silicon locally on a scale of tens of

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nanometers [12]. The nanoscale patterns were transferred into silicon substrate using the generated oxide as a mask. The transferred silicon patterns can even be shrunk if the crystal orientation is carefully selected and the ODE [13] method with KOH solution is adopted. There have been difficulties in electrical property measurement for SiNWs grown from Au particles, because the SiNWs were hard to align with the metal pads. Some researchers used SPM tips for SiNWs preparation and electrical-property measurement [14].

In top-down methods, SPL provides wide exposure latitude in nanoscale patterning. Also, SPL has been proposed as a simpler and lower-cost alternative to EBL systems for the generation of nanometer-scale patterns for research. In this work, we propose a technique to fabricate SiNWs with SPL and orientation-dependent etching by KOH on bare silicon. The main advantages of this method are that it provides both a cheaper processes as it is based on a bare silicon wafer rather than on a SOI wafer, and that devices whose electrical properties can be measured can be produced with few additional IC process steps.

2. Experiments and results

A p-type (1 1 0)-oriented bare silicon wafer with resistivity of 1–10 Ω cm was used. Before processing, standard RCA clean was employed and followed by 950 °C dry oxidation for 30 min; the thickness of the oxide is about 600 Å. The next process is to form the active area (AA) region with conventional lithography and BOE oxide etching for 1 min, and to identify the {1 1 1}-orientation for ODE with KOH etching. Fig. 1(a) shows the top view after definition of active area; the distance between alignment marks is 50 μm. Before local oxidation process by SPL in contact mode, native oxide was removed again and the silicon surface was hydrogen-passivated by dipping samples in 5% aqueous hydrofluoric (HF) solution. In SPL, a thin water film between tip and sample supplies the OH^- ions for anodic oxidation. The OH^- ions react with holes (h^+) from the Si surface to form silicon dioxide: $Si + 2h^+ + 2OH^- \rightarrow SiO_2 + 2H^+$ by the electric field resulting from the voltage between the tip and the sample. After the local oxidation, orientation-dependent chemical etching results in the slowest etch rate on the (1 1 1)-plane. Fig. 1(b) shows the top view after the ODE process. Fig. 1(c) is a schematic cross-section of SiNW after KOH etching; T is the thickness and W the width of a SiNW. The SiNWs were formed directly from

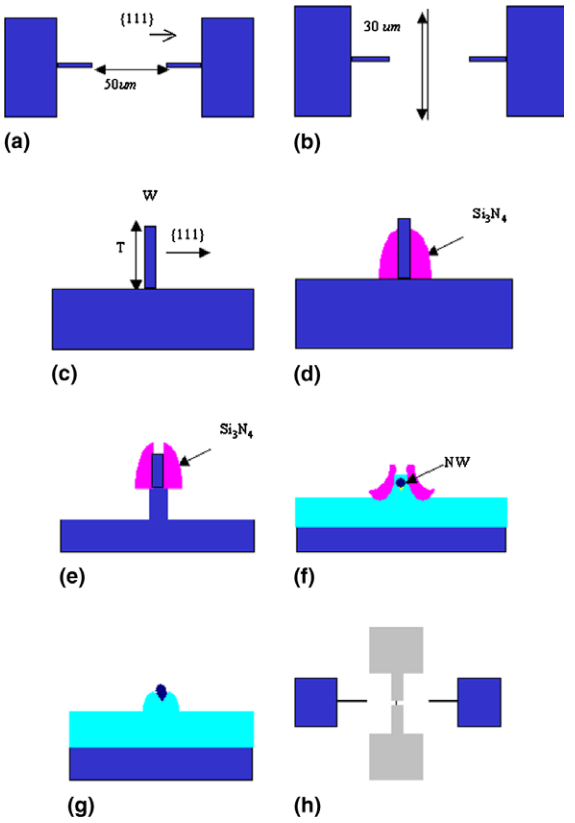

Fig. 1. Schematic of process flows: (a) Active area (AA) region was defined with conventional lithography. The distance of the alignment marks is 50 μm. {1 1 1}-orientation is aligned along the alignment marks. (b) Top view of the SiNW after scanning probe lithography, and KOH wet etching. The dimension of SiNW is controlled by bias voltage and the tip writing speed. (c) Cross-section view of SiNW, where T is the thickness and W is the width of the nanowire. (d) The SiNW were capped with pad oxide and the silicon nitride spacer, which protect the SiNW in the subsequent isolation process. (e) KOH wet etching. The etch time is one half of that in (b). (f) 1050 °C dry oxidation for SiNW isolation. (g) The silicon nitride is stripped by H_3PO_4 at 160 °C. The SiNW is exposed for contact pads patterning. (h) Aluminum contact pads were defined and sintered at 400 °C for 30 min.

the silicon wafer and contact the substrate electrically. The nanowires can now be isolated from the substrate. A standard RCA clean is used again and followed by pad-oxide growth in a furnace at 950 °C for 5 min, so that the SiNWs were capped with 50 Å pad oxide. Low-pressure (LP) chemical vapor deposition (LPCVD) is used for silicon nitride deposition on the wafer. Dry etching is used to remove both LP Si_3N_4 and pad oxide. Anisotropic KOH wet etching {1 1 1}-orientation, the sidewalls of SiNWs were vertical such that pad oxide and silicon nitride spacers were formed after dry etching. In order to clean the nitride on silicon wafer completely, 10% over etching is used. Fig. 1(d) shows a schematic of SiNW with silicon nitride spacer. Then, HF dip for 1 min removed the pad oxide and was followed by 40 °C KOH wet etching for a time is set at one-half the of previous KOH process, to prevent the SiNWs being etched off. Fig. 1(e) shows a schematic after the second KOH etching process. We then isolated the SiNWs with 1050 °C dry oxidation, the oxidation time being strongly dependent on the thickness of silicon nitride spacers. Fig. 1(f) shows a schematic of the SiNWs after isolation. The silicon nitride spacers were removed with 160 °C H_3PO_4 to expose the SiNWs to the contact pads; Fig. 1(g) shows a schematic after stripping the nitride. Aluminum contact pads were defined and sintered at 400 °C for 30 min; Fig. 1(h) shows schematically the aluminum contact-pad pattern. The electrical properties of SiNWs with source and drain, and with the substrate as bottom gate, were then measured.

In SPM local oxidation, the electric field from the tip causes dissociation of water, leading to anodic oxidation of the substrate. Because the oxide has about twice the volume of the silicon, the oxidation region is higher than the rest of the surface. Fig. 2(a) shows the oxidation line of silicon by SPL with tip bias voltage of −8 V and tip writing speed of 1.0 μm/s. The KOH etching temperature is controlled at 40 °C. The etching time is optimized at 400 s because of SiNWs would be etched off if etching time exceeded 450 s. As described, the width of SiNWs can be controlled by proper choice of the applied tip voltage and the scanning speed. Table 1 shows the width of SiNWs

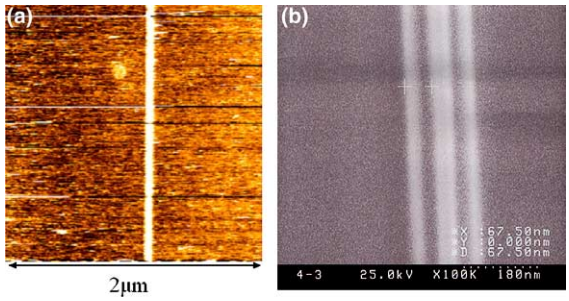

Fig. 2. (a) The AFM topography of SiNW. The height of nanowire is 161 nm. (b) The SiNW with 660 Å LP nitride spacers.

Table 1
Widths of SiNWs generated with SPL at various scanning speeds and voltages, at 39% humidity, followed by KOH etching at 40 °C for 400 s

Tip voltage (V)	Scanning speed (μm/s)		
	0.5 (nm)	1 (nm)	2 (nm)
−7	45	35	30
−8	80	50	40
−9	140	100	80
−10	160	130	90

generated with various speed sand voltages at 39% humidity and etching at 40 °C for 400 s with KOH (34%). A 50 Å pad oxide grown at 950 °C and a 1000 Å LPCVD-deposited Si_3N_4 film were used to protect the SiNWs during dry etching. They also formed spacers after dry etching. With 1050 °C dry oxidation for 60 min, the SiNW is isolated from the substrate electrically. Fig. 2(b) shows the SEM of the spacer is about 660 Å after dry etching. The nitride spacers were removed in 160 °C with H_3PO_4 for the purpose of electric measurement. After deposition of 5000 Å aluminum film, contact pads were defined with conventional lithography and followed by 400 °C sintering for 30 min.

The isolation time is dependent on the width of SiNWs and the thickness of the spacers. With the parameters described above, the SiNW with 160 nm in width was isolated with 1000 Å isolation oxidation. But, if the width of nanowires is over 50 nm, it is difficult to isolate them with the same thickness of oxide when the spacer thickness is larger than 240 nm. In this case, current leaks through the substrate when a voltage is applied between source and drain.

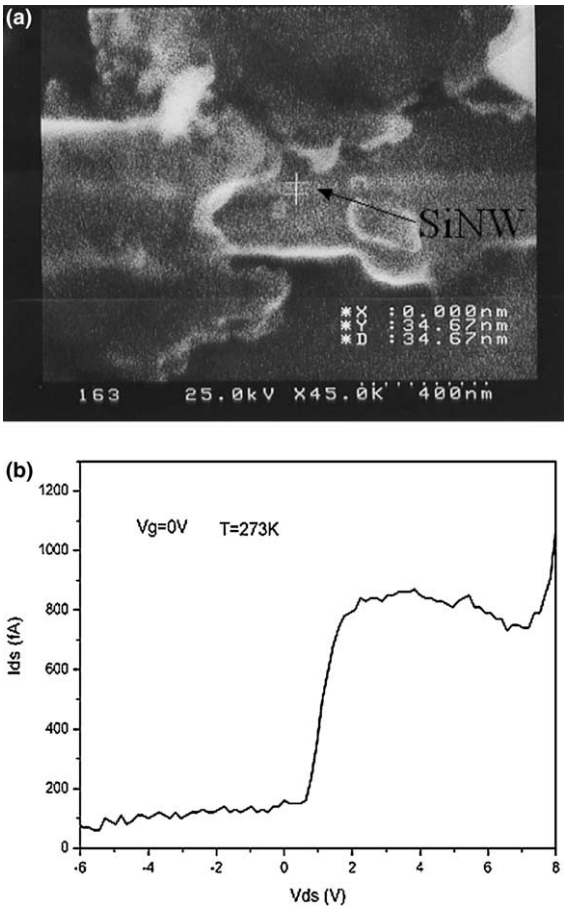

Fig. 3. (a) SEM image of bare SiNW on silicon oxide. (b) I–V characteristic of SiNW at 273 K. The width of SiNW is around 34 nm.

Fig. 3(a) shows SEM image of the SiNW directly on the oxide, and Fig. 3(b) shows the I_{ds}–V_{ds} curve at 273 K without any gate bias for a SiNW 34 nm wide. The small current at 0–8 V is because of Schottky barrier. Fig. 4 shows conductance oscillation at various gate voltages. The electrical-conductance behavior indicates strongly either that there are multiple barriers in the charge transport path or that defects are introduced on the surface of nanowires during dry etching. These barriers could result from defects or impurities in Al/Si interface. The proposed technique although provides a simple way to generate SiNWs, but defects and impurities control at the nanocontact interface should be treated carefully.

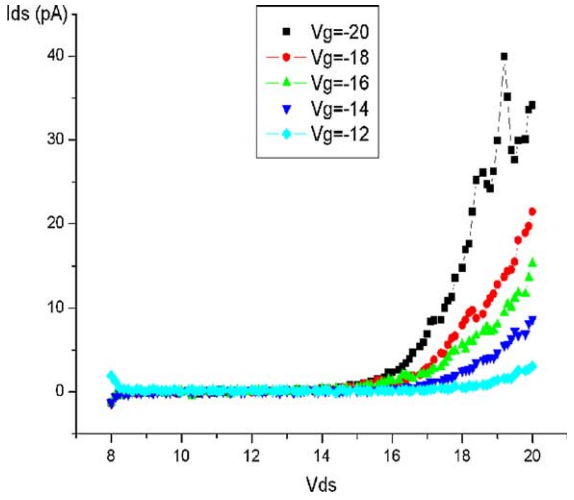

Fig. 4. I–V characteristic of SiNW with various gate voltages at 90 K. The conductance oscillation is observed. The width of SiNW is about 77 nm.

3. Summary

We have successfully fabricated SiNWs on bare silicon wafers using SPL and conventional IC processes. With proper manipulation of parameters in SPL and in KOH wet etching, the dimensions of the SiNWs are controllable. In this technique, LP nitride spacers play important roles for isolating the nanowires from the substrate and also as dimension control factor of nanowires. The diameter of SiNW, the thickness of nitride spacer, and the thickness of isolation oxidation are closely related. The thinner nanowire and the thinner nitride spacer make the isolation substrate easier. This fabrication technique provides simpler and cheaper processes than others, and measurement of electrical properties is also easier as compared to that of devices fabricated with bottom-up process. To avoid the barrier introduced by impurities and defects between nanowires and metal nanocontacts, studies will be conducted.

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