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Modeling the floating-body effects of fully depleted, partially depleted, and body-grounded SOI MOSFETs

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Abstract

This paper describes a unified framework to model the floating-body effects of various SOI MOSFET operation modes, including body-contacted mode, partially depleted mode and fully depleted mode. As the operation mode is dimension and bias dependent, different modes can co-exist in a single SOI technology. A smooth transit from one type of operation mode to another is thus essential and has been included in the model. In addition, the floating-body effects can couple to a number of other SOI specific phenomena such as heating assisted impact ionization, gate tunneling induced dynamic behavior, and operation mode dependent small signal output resistance. A methodology to model the overall SOI MOSFET behavior due to the combination of multiple floating-body related effects will also be described.
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Keywords: SOI; SOI devices; Circuit simulation; Device model; SPICE; BSIMSOI

1. Introduction

As mainstream bulk CMOS technology scales to sub-100 nm, it becomes more challenging to keep up with the continuous reduction of device dimensions as predicted by the Moore's Law. Silicon-on-insulator (SOI) technology has emerged as an alternative to bulk CMOS technology to address the performance requirements for sub-100 nm devices. It has been demonstrated that SOI CMOS and its derivatives such as double-gate MOSFETs can provide better performance with lower power consumption, making it very attractive for DRAM and microprocessor applications [1]. A major barrier to fully exploit the performance provided by SOI technology is the immature design tool for designing circuit applications. An important link between SOI technology and application design is a SPICE friendly compact SOI MOSFET model. A lot of efforts have been devoted to SOI modeling and a number of compact models have been made available in the public domain [2–4]. Among them, BSIMSOI developed by Pin Su [4] at UC Berkeley has been chosen by the Compact Modeling Council [5] to be the industrial standard model adopted by major technology provide such as IBM. The selection is not totally based on model accuracy, but the flexible architecture that makes it easy to be adopted during process development even before device data is available [6].

While SOI MOSFETs have a lot of common features in terms of structure and behavior with mainstream bulk CMOS devices, they also have many subtle differences that require particular attention. In particular, the floating-body effect is the key to understand the unique behavior in SOI MOSFETs. In this paper, the

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methodology used in BSIMSOI to model the floating-body effect is described. To be concise, only the features unique to SOI devices will be presented, and we assume the readers to be familiar with to the formulation of MOSFET model, which can be found in other publication such as [7]. The paper first describes the different device structures available in SOI technology including body-contacted (BC) SOI MOSFET, partially depleted (PD) SOI MOSFET and fully depleted (FD) SOI MOSFETs and how the floating effects in these structures are modeled. While the "structural" classification is conceptually simple, the different device types are actually categorized by operation modes rather than physical device structures. And different operation modes can co-exist in a single technology when dimensions and bias are varied. As a result, a unified floating-body model with smooth transition between different modes of operation is desired. As SOI technology is supposed to be meaningful only in small dimensions and low supply voltages, a number of device phenomena that are ignored in conventional MOSFETs can become significant and couple to the floating-body effects. This includes self-heating assisted impact ionization, gate current induced dynamic effects and frequency dependent performance parameters. A methodology to model these behaviors together with the floating-body effects will also be described.

2. Modeling floating-body effect in different SOI MOSFETs

2.1. Body-contacted MOSFET

BC MOSFETs is widely used in critical analog circuits like phase-lock loop. There are a number of ways to provide body contact, but the most common one resemble the structure shown in Fig. 1. Unlike the substrate contact in bulk device, the body contact in SOI MOSFETs has a high resistance distributed along the width of the device due to the short channel length and thin body [8,9] as shown in the figure. The body resistance (R_B) can be calculated by $R_B = R_{body} \times W/L$, where R_{body} is the resistivity per unit silicon film thickness of the body. While there have been proposal to use an effective resistance to approximate the body resistance, the approach cannot produce the gradual turn-on of the kink effect [10]. To fully account for the distributed effect of the body resistance, a wide SOI MOSFET has to be broken down into a number of smaller transistors in parallel as shown in Fig. 1(b) [11]. From a modeling perspective, a mechanism is required to contact the body terminal and turn-off related narrow width effect when decomposing the transistor into narrower ones. This option has been made available in BSIMSOI.

In addition to distributed-body resistance, the extra device area used to provide body contact creates an extra capacitive current path from drain to the body. This results in an enhanced frequency dependent output resistance (R_{out}) as shown in Fig. 2. For MOSFETs without floating-body effects, the drain-to-body and body-to-source capacitances behave like a short circuit at high frequency and provide a second conductive path connect the drain-to-source through the body resistance. Hence, a decrease in R_{out} is expected at high frequency. However, the frequency drop appears at around 1 kHz, which is much lower than that required to turn-on the second conduction path through the substrate. A different mechanism is responsible for this observation.

The decrease of R_{out} is attributed to the influence of floating-body effect, which can be explained by the small

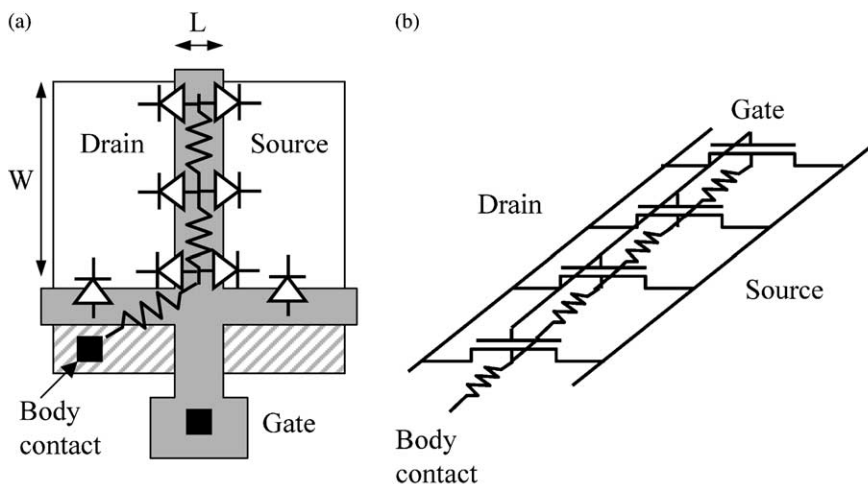


Fig. 1. (a) Common layout of a four-terminal side-body SOI MOSFET and (b) method to simulate distributed effect of body resistance. An accessible B node is provided in BSIMSOI to facilitate the simulation.

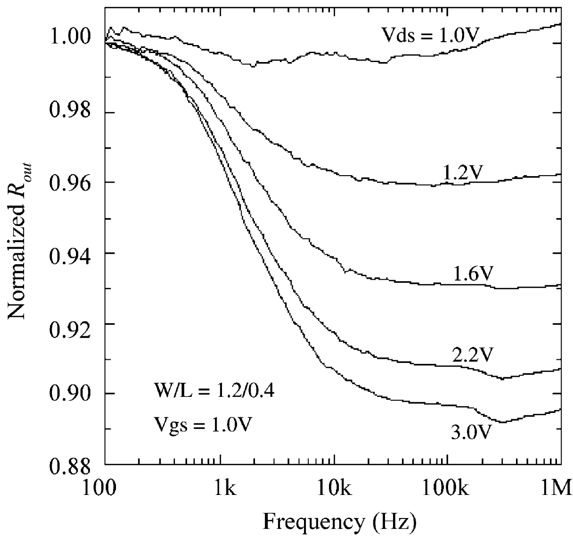


Fig. 2. Characteristics of output resistance (R_{out}) versus frequency at different drain voltage. R_{out} is normalized to by its DC value to observe the frequency dependence.

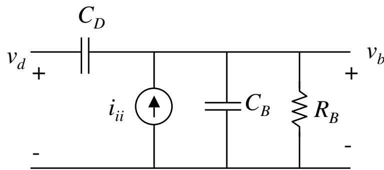


Fig. 3. Small signal equivalent circuit for the floating body. C_D is dominated by the capacitance between the drain and body contact. C_B represents the equivalent capacitance from body to AC ground. R_B is the body resistance and I_{ii} is the impact ionization current.

signal equivalent circuit shown in Fig. 3 [12]. The body potential is supposed to be connected to ground by the body contact, but it cannot be completely grounded due to the distributed-body resistance R_B. When a small signal drain voltage v_d is applied, the body potential v_b is modulated, which in term causes V_T to fluctuate. It provides a mechanism for the drain voltage to modulate V_T which shows up in the R_{out} characteristics. The small signal model given in Fig. 3 can be used to track the fluctuation of v_b as a result of v_d variation which is then fed back to the calculation of V_T. At low frequency, this drain coupling effect is insignificant when the body resistor R_B can still provide an effective discharging path for the capacitive current from the drain. So, the value of R_B will affect the frequency at which R_{out} degradation appears. The model has been extensively verified by measurement data from many devices with different dimensions and under various bias conditions.

2.2. Partially depleted SOI MOSFET

While a BC SOI MOSFET can produce bulk MOSFET like *I–V* characteristics that we are familiar with, the use of substrate contact consumes extra area, and is generally not desirable in circuit applications. PD MOSFETs with floating body are still the most popular technology used in manufacturing ICs in company like IBM. The accurate modeling of PD MOSFETs again has to do with the modeling the impact of floating body on the device behaviors. In BSIMSOI, an equivalent circuit as shown in Fig. 4 is used to calculate the floating-body voltage under the influence of various body currents.

In DC operation, the impact ionization current (I_{ii}) [13] at the drain flows to the body and forward biases the source-to-body diode so that the diode current is equal to the I_{ii}. Thus the floating-body potential is dictated by the *I–V* characteristic of the source to body diode. The diode voltage between the body and source increases the body voltage (V_B), which in turn cause a reduction in threshold voltage V_T. The change in V_T causes a sudden increase in drain current when the impact ionization becomes significant. It results in the famous kink effect in the drain current versus V_D curve as shown in Fig. 5. This effect can be modeled effectively by monitoring the degree of forward bias of the body-to-source junction as a function of I_{ii}, which is a strong function of V_D. The diode model has to include a number of non-uniform lateral doping effects due to the use of halo (pocket implant) in most of the industrial process. The calculated V_{BS} is used to modify V_T using the body effect

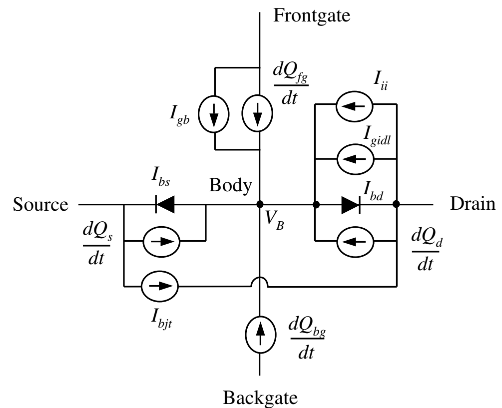


Fig. 4. Circuit representation of the floating-body potential calculation under the influence of various DC and charging currents: I_{gb}—oxide tunneling current; I_{ii}—impact ionization current; I_{gidl}—gate induced drain leakage; I_{bjt}—bipolar current; I_{bs}—recombination current; I_{bd}—junction leakage. Q_g, Q_{bg}, Q_d and Q_s represent the frontgate charge, back charge, drain charge and source charge respectively. Q_d and Q_{rms} mainly arise from the drain and source to body diodes.

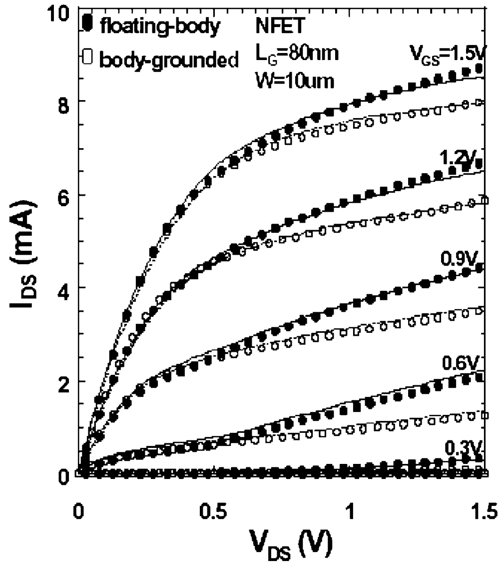


Fig. 5. *I–V* characteristics of a PD SOI MOSFET with excess current due to the kink effects when the body is floating. The lines indicate the fitting from BSIMSOI with the floating-body effects included.

equation $V_T = V_{T0} + \gamma(\sqrt{2\phi_B - V_{BS}} - \sqrt{2\phi_B})$, which will then be used to calculate the drain current.

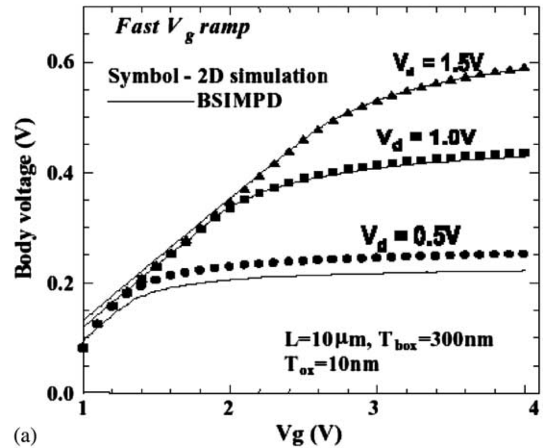
During time domain simulation, transient charge and capacitive coupling between all the terminals have to be accounted for in the calculation of the body potential. V_{BS} is determined by the initial body charge as well as the displacement current resulting from capacitive coupling of the body node to other terminals. For example, when the gate is switched from low to high, it causes an initial increase in the body voltage beyond the equilibrium value. The body voltage will then settle to the equilibrium value governed by a time constant determined by the combined effects of carrier generation/recombination rate, gate-induced-drain-leakage, impact ionization current, gate tunneling current, and body-to-source diode current. Various body leakage and displacement currents that determine the floating-body potential are included in the body voltage model shown in Fig. 4. From the equivalent circuit, a nodal equation at the body node can be written as:

$$\left(\frac{dQ_g}{dt}+\frac{dQ_{bg}}{dt}+\frac{dQ_d}{dt}+\frac{dQ_s}{dt}\right)+(I_{ii}+I_{gidl}+I_{bs}+I_{bd})+I_{gb}=0 \quad (1)$$

The SPICE solution to the differential equation at the body node depends not only on the present terminal voltages, but also the initial conditions of the body charge (past history). The behaviors of the body potential with respect to V_G and V_D switching from the model and 2-D device simulation are compared and the results are shown in Fig. 6 with an input ramp much fast that the RC time constant o the subcircuit given in Fig. 4. The model can predict the correct behavior of the body potential as a function of both V_D and V_G switching.

2.3. Fully depleted SOI MOSFET

In order to suppress short channel effects, the silicon film thickness has to be scaled together with the channel length in advanced device structure. As the silicon thickness becomes thinner than the depletion depth of the body, it operates in the FD mode and the observed floating-body effect decreases. FD mode is not too much different from PD mode except (1) the threshold voltage becomes silicon film thickness and back-gate bias dependent [14]; (2) backgate can be more effectively coupled to the frontgate [15]; (3) close to ideal subthreshold swing of 60 mV/dec at room temperature [16];



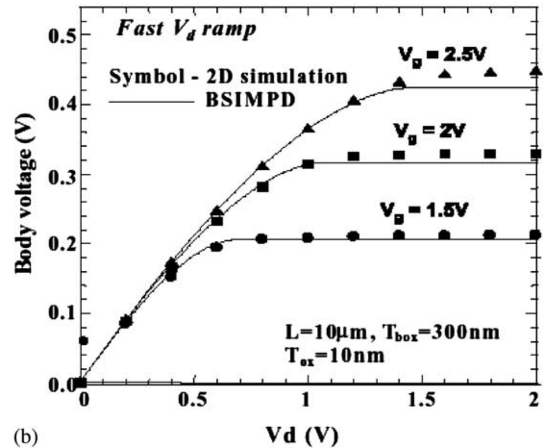


Fig. 6. The body potential predicted by BSIMPD in (a) fast gate voltage ramp and (b) fast drain voltage ramp compared with result from 2-D device simulation.

and (4) reduction of kink effect [17]. All these effects can be handled in a unified way using the body-to-source barrier-lowering concept.

The main operational difference between PD mode and FD mode operation is the body-to-source potential barrier at the backgate. In the PD mode at equilibrium, it is the same as the built-in potential of the body-to-source diode as shown in Fig. 7. When the film thickness is reduced and the device starts to operate in the FD mode, the potential barrier between the source and body at the backside is lowered by ΔV_{bi} as shown in Fig. 7, which is equivalent to the source-to-body diode in the PD mode is forward biased. This lowering also depends on the backgate bias. Using this ΔV_{bi}, the threshold voltage lowering with reference to the PD MOSFET case can be modeled. In practice, the V_{T} used in compact model is usually extracted rather than calculated and thus is absolute value is not very important in a practical modeling framework. The more important effect is the modulation of ΔV_{bi} under different terminal biases that affect the device output characteristics. The diode characteristic between the body and source is determined by ΔV_{bi} as shown in Fig. 8, where $\Delta V_{\mathrm{bi}} = 0$ correspond to the PD case. ΔV_{bi} as a function of silicon film thickness and back gate bias, which can be expressed as

$$\Delta V_{\mathrm{bi}}(\phi_{\mathrm{S}}) = \frac{C_{\mathrm{Si}}}{C_{\mathrm{Si}} + C_{\mathrm{box}}}\left(\phi_{\mathrm{S}} - \frac{qN_{\mathrm{ch}}}{2\varepsilon_{\mathrm{Si}}}t_{\mathrm{Si}}^2 + \Delta V_{\mathrm{DIBL}}\right) + \eta_{\mathrm{e}}(L_{\mathrm{eff}})\frac{C_{\mathrm{box}}}{C_{\mathrm{Si}} + C_{\mathrm{box}}}(V_{\mathrm{bgs}} - V_{\mathrm{fbb}}) \quad (2)$$

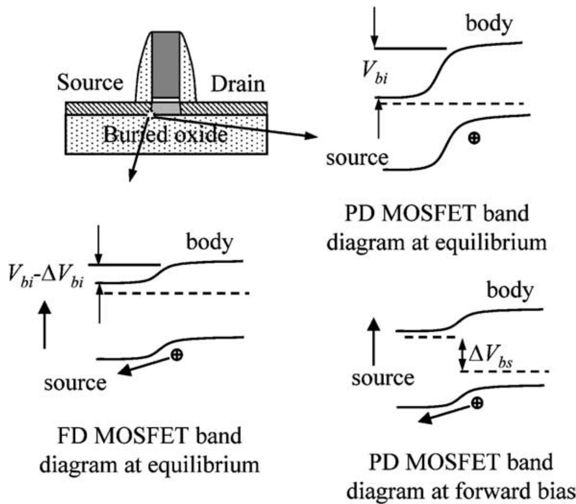


Fig. 7. Body-to-source band diagram at the back side indicating the lowering of built-in potential relative to the value calculated from the body/source PN junction. FD devices has a lower barrier (larger ΔV_{bi}) to begin with and more stable under the influence of external currents.

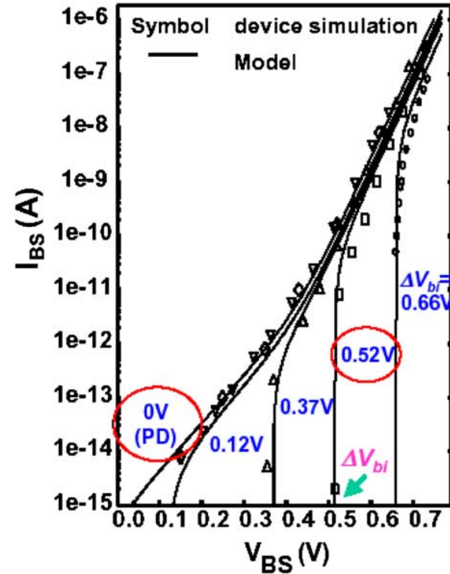


Fig. 8. The source-to-body diode characteristics as a function of ΔV_{bi} from a generic SOI NMOSFET with different channel doping of 1×10^{17} cm^{-3} with different film thickness to give the corresponding ΔV_{bi}. FD device can accommodate larger current (I_{BS}) before a change in V_{BS} is necessary due to its higher initial ΔV_{bi}. As V_{BS} in FD devices varies at a smaller range than in the PD case, the floating-body effect is less significant.

where ϕ_{S} is the surface band bending that can be approximated by

$$\phi_{\mathrm{S}} = \begin{cases} \phi_{\mathrm{ON}} - \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} + \left(C_{\mathrm{Si}}^{-1} + C_{\mathrm{ox}}^{-1}\right)^{-1}}(V_{\mathrm{T}} - V_{\mathrm{GS}}) & \text{for } V_{\mathrm{GS}} < V_{\mathrm{T}} \\ \phi_{\mathrm{ON}} & \text{for } V_{\mathrm{GS}} \geqslant V_{\mathrm{T}} \end{cases} \quad (3)$$

ϕ_{ON} in generally can be represented by $2\phi_{\mathrm{B}}$. ΔV_{DIBL} and η_{e} are correction terms due to drain-induced-barrier-lowering and short channel effects. In BSIMSOI, they are given by

$$\Delta V_{\mathrm{DIBL}} = D_{\mathrm{vbd0}}\left(\exp\left(-D_{\mathrm{vbd1}}\frac{L_{\mathrm{eff}}}{2l}\right) + 2\exp\left(-D_{\mathrm{vbd1}}\frac{L_{\mathrm{eff}}}{2l}\right)\right)(V_{\mathrm{bi}} - 2\phi_{\mathrm{B}}) \quad (4)$$

$$\eta_{\mathrm{eff}}(L_{\mathrm{eff}}) = K_{1b} - K_{2b}\left(\exp\left(-D_{k2b}\frac{L_{\mathrm{eff}}}{2l}\right) + 2\exp\left(-D_{k2b}\frac{L_{\mathrm{eff}}}{2l}\right)\right) \quad (5)$$

The values of the parameters can be referred from the BSIMSOI manual [18]. The first term in the equation represents the frontgate coupling. N_{ch} is the effective channel doping, which may vary with channel length due to non-uniform lateral doping. The second term of

the equation represents the backgate coupling. The minimum value of ΔV_{bi} is fixed at zero, as it is physically impossible to go negative.

From the expression, FD devices with thin silicon film thickness give higher ΔV_{bi}. As a result, higher impact ionization current from the drain (I_{bs}) can be accommodated before it causes a change in V_{BS} as shown in Fig. 8. The reduced sensitivity of V_{BS} to impact ionization current gives a reduced floating-body effect. According to Fig. 8, ΔV_{bi} can be used to indicate the degree of full depletion of a SOI MOSFET. For FD devices with small ΔV_{bi}, floating body induced phenomena like the kink effects can still be observed.

2.4. Transition for PD and FD including dynamic depletion

State-of-the-art SOI technology requires FD devices with extremely thin silicon film thickness to suppress SCE. At the same time, devices with multiple V_T's are often used to optimize the tradeoff between speed and standby power. It is then possible or even preferred to have devices with different T_{Si} in a process. When combined with the use of pocket implants, it is generally observed that FD and PD devices co-exist in the same technology. Furthermore, the same devices can behave as either PD or FD depends on bias conditions. As observed from the transistor characteristics shown in Fig. 9, the device can operate at PD mode (with subthreshold swing of 102 mV/dec) or FD mode (with subthreshold swing of 67 mV/dec) depends on the backgate bias. A dynamic transition with the gate voltage can also be observed, which is referred as dynamic depletion (DD) [19]. It occurs because at a low gate voltage, the depletion width from front oxide interface to the silicon film is small and the device operates at the PD mode. When the gate voltage increases, the depletion region extends to the back gate and eventually becomes FD [20].

The three modes of operation (FD, PD and DD) can be captured in a unified way by modeling the body-to-source built-in potential lowering using the concept of ΔV_{bi}. First, ΔV_{bi} is calculated and using Eq. (2) with known T_{Si}, t_{ox} and gate voltages. Then, assumes the film thickness is infinite in PD model and calculates the corresponding V_{BS} when the device is operating in PD mode using the equivalent circuit given in Fig. 4. ΔV_{bi} is then compared with the V_{BS} in PD. If this V_{BS} becomes smaller than ΔV_{bi}, then the body-to-source barrier lowering is mainly caused by ΔV_{bi} and the FD characteristics of the device dominates. If some mechanism, such as impact ionization at high V_{DS}, gives a higher V_{BS}, the FD mode with the calculated ΔV_{bi} can no longer accommodate the currents from the body-to-source as shown in Fig. 8. In this case, the body potential is modulated by the V_{BS} in the PD mode rather than maintaining a constant value at ΔV_{bi}. Therefore, an effective body potential can be formulated by selecting the smaller V_{BS} and ΔV_{bi} as shown in Fig. 10 to monitor the body potential. The effective V_{BS} concept provides a unified approach to model the characteristics of floating-body effects due to fluctuation of body potential in PD, FD and DD devices.

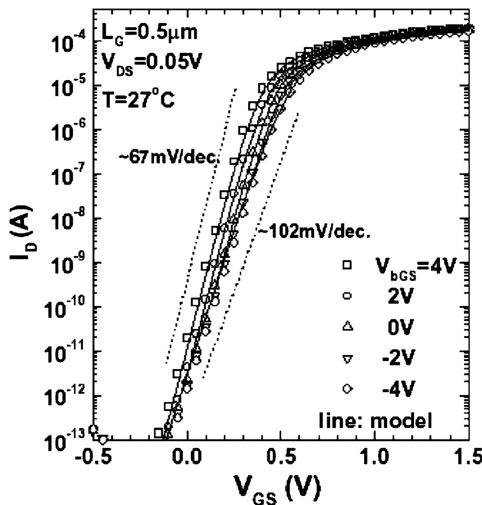


Fig. 9. The PD/FD transition under different backgate biases for a MOSFET with 60 nm silicon film thickness and 10 nm of t_{ox}. Correctness in calculating the ΔV_{bi} can accurately predict the observed effect.

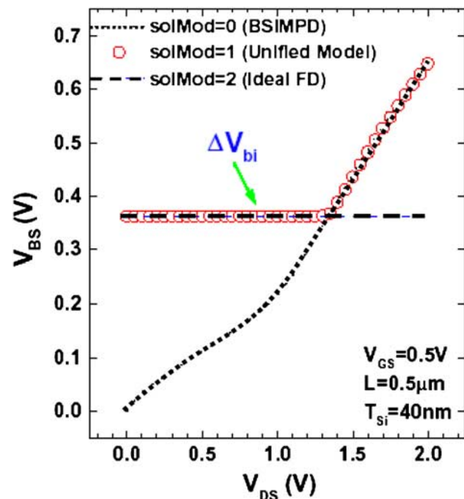


Fig. 10. The body potential in the unified model approaches. V_{BS} is first solved as in PD model, which return to ΔV_{bi} for ideal FD more operation.

3. Advanced models for floating-body effects in deep-submicron SOI MOSFETs

In the state-of-the-art SOI process, a number of newly observed behaviors cannot be explained using some commonly known theories. New physics have to be included before these observations can be explained. All these observations, however, are still directly or indirectly linked to the floating-body effect and they are explained below.

3.1. Thermal related effects

The kink effect has been regarded as the signature of PD SOI MOSFET, and it has been attributed to impact ionization induced substrate current. With the reduction of power supply voltage to below 1 V according to the technology scaling roadmap, the impact ionization theory predicts that the kink effect will be eliminated because the carrier acceleration energy becomes less than the bandgap energy of silicon, which is around 1.1 V. However, the kink effect can still be observed in SOI MOSFETs operating at a drain voltage below 1 V. It requires a correction to the existing substrate current model.

The observed kink effect can be explained by the lattice temperature assisted subbandgap impact ionization [21]. In SOI MOSFET, this effect is enhanced due to self-heating. The Arrhenius plot given in Fig. 11 shows the relationship between impaction ionization current (normalized by I_D) and the reciprocal of temperature. The required activation energy to cause impact ionization under a given drain voltage is given by $E_a = E_g - qV_D$, and this E_a has to be supplied by the lattice temperature. The smaller the E_a, the larger the impact ionization current at a given temperature. Thus, the thermally assisted impact ionization model at $qV_D < E_g$ is given by:

$$\frac{I_{sub}}{I_D} \propto \exp\left[\frac{-(E_g - qV_D)}{kT}\right] \quad (6)$$

where I_{sub} is the substrate current. The model has been verified by a lot of experimental data and the results are also plotted in Fig. 11, indicating the correct dependents of impact ionization current with respect to temperature. The thermal driven sub-E_g impact ionization model predicts a linear dependent between $\ln(I_{sub})$ and V_D. On the other hand, the traditional theory predicts that $\ln(I_{sub})$ depends on $1/V_D$ when the impact ionization is electric-field driven. In some immediate V_D, a smooth transition from thermal driven impaction to electric-field driven impact ionization is required. In BSIMSOI, this is modeled by

$$\frac{I_{sub}}{I_D} \propto \exp\left(\frac{V_D}{\beta_0 + \beta_1 V_D + \beta_2 V_D^2}\right) \quad (7)$$

where β_0, β_1, β_2 are fitting parameters. At low temperature region, we observed the experimentally determined activation energy is smaller than the theoretical prediction, which indicates other energy gain mechanisms are involved in the process. One of these mechanisms is

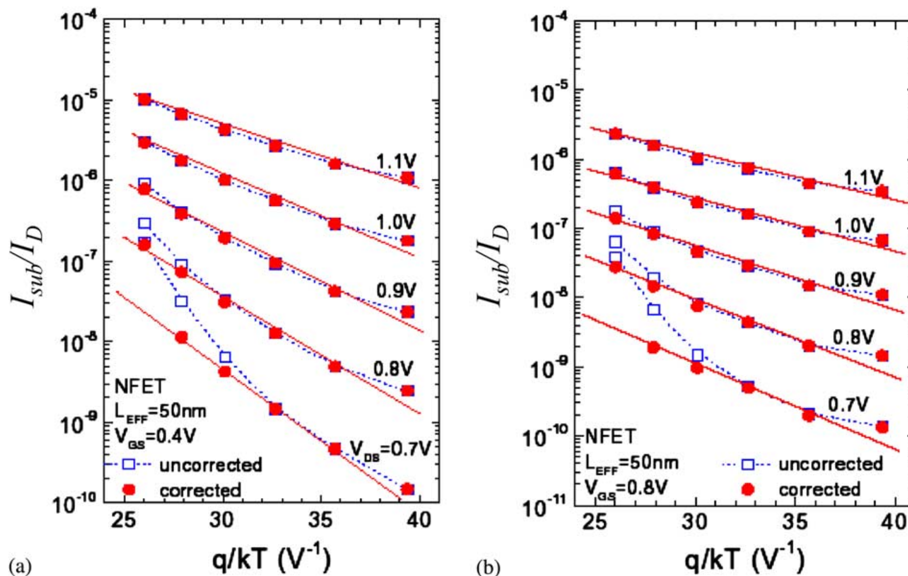


Fig. 11. Measured I_{sub}/I_D versus reciprocal temperature at (a) $V_{GS} = 0.4$ V and (b) $V_{GS} = 0.8$ V of a SOI NMOSFET. The uncorrected curves are the total measured substrate current while the corrected curves have the temperature dependent junction leakage currents subtracted to display the intrinsic characteristics of the impact ionization current.

electron–electron scattering that provide an additional source for carrier heating as proposed in [22–24]. This phenomenon is more prominent when the channel electron concentration is high at large V_{GS}. It agrees with the observation that the deviation between experimental data and model prediction at low temperature becomes larger when the gate voltage is increased from 0.4 to 0.8 V as shown in Fig. 11.

3.2. Impact of gate tunneling current on floating-body effect

In bulk MOSFET, the gate tunneling current adds an additional component to the DC currents that in most cases, can be handled by simple superposition of all currents. In a SOI MOSFET, the gate tunneling current contributes a conduction path to the floating body and modulates the body-to-source voltage [25]. As a result, it affects the intrinsic value of the drain-to-source current. The effect have to be modeled by adding the impacts of various gate leakage currents to the floating-body potential, which have been included in the equivalent circuit given in Fig. 4. This body voltage is used to calculate V_{BS} in PD operation, or the equivalent body voltage in the unified PD/FD model.

To investigate the impact of the gate tunneling current on the behavior of a SOI MOSFET, the turn-on responses by a step gate voltage input are simulated with and without the gate tunneling model activated. The results are shown in Fig. 12. Without gate tunneling, body charge decreases due to carrier recombination once inversion layer is formed and shield the gate-to-body coupling. With oxide tunneling, the gate current continues charging the body even after the formation of the inversion layer. The body potential continues to increase until the forward diode current from the body-to-source becomes equal to the gate current. The time to reach this equilibrium depends on the forward bias characteristics of the body-to-source diode. In this particular simulation, the time constant (t_p) for PMOSFET to reach steady state is longer than that of NMOSFET (t_n) due to smaller recombination current at the junction and net

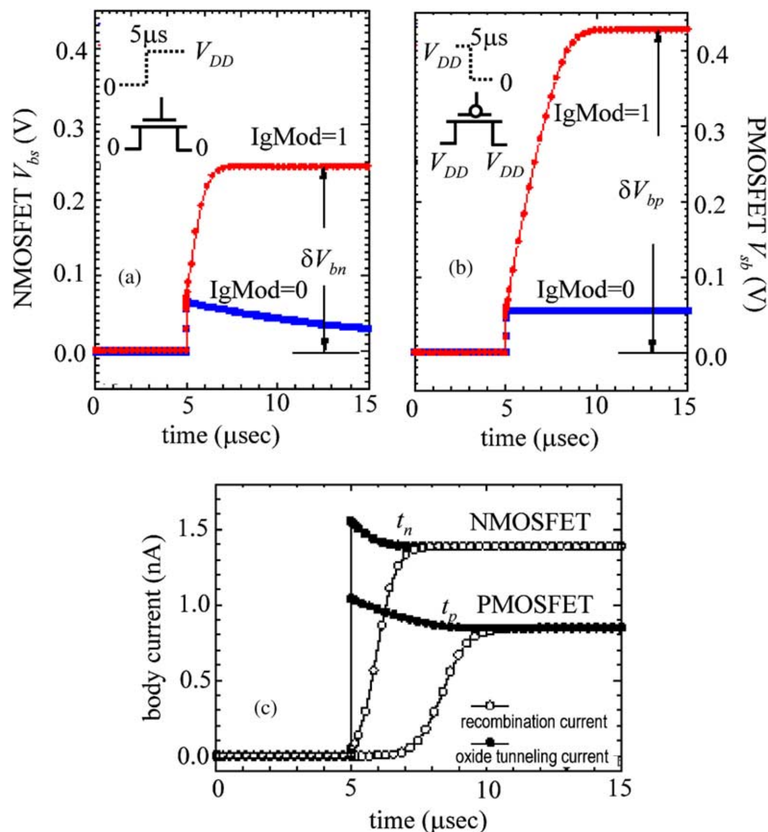


Fig. 12. Impact of gate tunneling (IgMod = 1) on the transient behavior of (a) NMOSFET; (b) PMOSFET; and (c) body current. Simulation results without body current (IgMod = 0) are also included for comparison. Simulation parameters are $V_{DD} = 1.5$ V, $t_{ox} = 1.5$ nm, $W = 5$ μm.

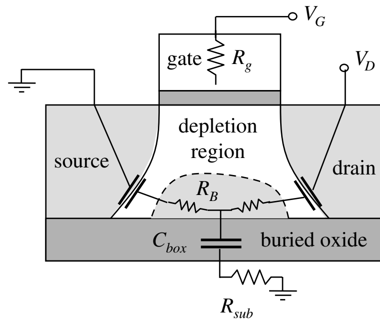


Fig. 13. A model to display the equivalent RC network in high frequency operation. The output resistant reduction depends on the body resistance R_B which is determined by the gate voltage and silicon film thickness.

charge injection to the source. Thus, the induced forward body potential for PMOSFET (δV_{bp}) is larger than of the NMOSFET (δV_{bn}).

3.3. Modeling output resistance SOI MOSFET at high frequency

At high frequency, it is observed that FD devices have a higher output resistance than PD devices and the drain voltage has a strong influence at the output resistance [26]. The observation can be explained by the schematic shown in Fig. 13. At high frequency, the drain-to-body and source-to-body capacitor behavior like a short circuit and create another current path from the drain-to-source. However, the resistance from the drain-to-source is under the influence of the terminal bias and mode of operations. In particular, the body resistance become very large and can be regarded as infinite in FD mode.

Besides the additional current path, a more important effect is the modulation of body-to-source potential though this new current path. A good representation of the physical structure is the addition of a series RC branch in parallel to C_D in Fig. 13.

4. Conclusion

In this paper, a framework to model the floating-body effect of SOI MOSFETs has been described in detail. The approach has been used to formulate the BSIMSOI model, which is the current industrial standard SOI MOSFET model. The behavior of SOI MOSFETs, in a large part, is governed by the floating-body effect. The accurate modeling of the floating-body effect is essential to capture a number of unique characteristics of SOI MOSFETs.

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