A Novel 25-nm Modified Schottky-Barrier FinFET With High Performance

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***Abstract*—High-performance modified Schottky barrier (MSB) FinFET with 25-nm channel length and fully silicided source/drain (S/D) is proposed for the first time. Using an implant-to-silicide technique, an ultrashort and defect-free S/D extension can be formed at temperature as low as 600 °C. The MSB FinFET exhibits better current–voltage characteristics than those of published Schottky barrier devices and FinFETs. With 4-nm-thick gate oxide, the I_{on}/I_{off} current ratio higher than 10^9 is achieved. The subthreshold swing of 25-nm and 49-nm MSB FinFETs is 83 and 64.5 mV/dec at room temperature. The advantage of low thermal budget relaxes the thermal stability issue for metal gate/high-κ dielectric integration. It is believed that the proposed MSB FinFET would be a very promising nano device.**

***Index Terms*—FinFET, Schottky barrier, silicon-on-insulator (SOI).**

I. Introduction

SCHOTTKY-BARRIER (SB) source/drain (S/D) silicon-on-insulator (SOI) MOSFETs have been proposed for future nanoscale devices because of easy process and small external resistance of S/D [1]–[5]. However, the SB MOSFETs still have some drawbacks. The first drawback is the smaller on-state driving current (I_{on}) than that of the conventional pn junction MOSFETs due to the Schottky barrier between the silicide and the inverted channel. In the previous study, a method of using complementary low-barrier silicide : PtSi for pMOS and ErSi for nMOS, has been suggested to reduce this barrier [2], [3]. The problem of high I_{off} of SB-SOI MOSFETs comes from the thermionic emission at the drain contact has been confirmed [6]. Kedzierski *et al.* introduced the FinFET architecture on SOI and demonstrated low $I_{off} \sim \ln A/\mu m$ for 20×25 nm^2 devices [7]. Adding a metal field-plate over the MOSFETs has been shown to be effective in reducing the I_{off} by suppressing back-injection from the drain contact, but it requires an additional voltage supply and sacrifices device density [8].

In this letter, to overcome the drawbacks of SB MOSFETs while keeping the effect of Schottky contact on the low S/D external resistance and the low temperature process, we propose a modified SB FinFET (MSB FinFET) with ultrashort S/D extension (SDE) at the interface of silicide and inverted channel. Adding an extension doping in the silicon drastically improves Schottky limit for I_{on} by thinning and reducing the SB at the source/body junction at on-state. The proposed MSB devices also show significant lower I_{off} than the conventional SB devices because of the high and wide Schottky-barrier at drain/body junction at off-state. Therefore, it is demonstrated that the driving current of the proposed MSB FinFET can be higher than 250 μA/μm (or 750 μA/μm dependsing on the definition of the channel width) and the I_{on}/I_{off} current ratio can be higher than 10^9.

Manuscript received February 17, 2004; revised March 25, 2004. This work was supported by the National Science Council of Taiwan, R.O.C., under Contract NSC-91-2215-E-009-018. The review of this letter was arranged by Editor B. Yu.

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Digital Object Identifier 10.1109/LED.2004.828980

II. Device Fabrication

Fig. 1 shows the main fabrication process flow of the proposed MSB FinFET. The starting material was boron-doped 6-in SOI wafers with background doping of around 1×10^{15} cm^{-3}. The nominal Si layer and buried oxide layer thickness were 40 and 150 nm. The device island (including S/D region and Si fins) was defined by electron-beam (e-beam) lithography and plasma etching. A 4-nm-thick SiO_2 was thermally grown as gate dielectric. Poly-Si film of 150 nm thick was deposited and doped by BF_2^+ ion implantation at 40 KeV to a dose of 5×10^{15} cm^{-2}. After a rapid thermal activation at 1025 °C, 50-nm-thick TEOS oxide was deposited with low-pressure chemical vapor deposition (LPCVD) as hard mask. E-beam lithography was employed again to define gate pattern as shown in Fig. 1(a). Following gate patterning, a SiO_2 (10 nm)/Si_3N_4 (30 nm) composite spacer was formed and is shown in Fig. 1(b). The hardmask on poly-Si was etched away during spacer etching. Ni film of 22 nm thick was then deposited in a sputtering system. To convert Si layer at S/D region into silicide completely with suitable lateral growth, a two-step annealing process was performed. At first, the wafer deposited with Ni was annealed in vacuum chamber at 300 °C for 80 min. After the unreacted Ni was selectively removed by wet chemical etching with H_2SO_4/H_2O_2 solution, the wafer was annealed in N_2 ambient at 600 °C for 30 s [Fig. 1(c)]. Ni-silicide was formed on poly-Si gate simultaneously. BF2 $^+$ ions were implanted to silicide (ITS) at 30 KeV to a dose of 3×10^{15} cm^{-2} followed by a furnace annealing at 600 °C for 30 min. Monte Carlo simulation shows that the ions straggle distribution is only 8 nm, which is shorter than the lateral growth of silicide [9]. Because of the low solid-state solubility of boron in Ni silicide, boron atoms diffused out and piled up at the Si–silicide interface to form an ultrashort SDE as shown in Fig. 1(d). It has been reported that ITS process forms a modified Schottky junction with characteristics between pn junction and Schottky junction [10], [11]. Since the ion implantation process does not damage

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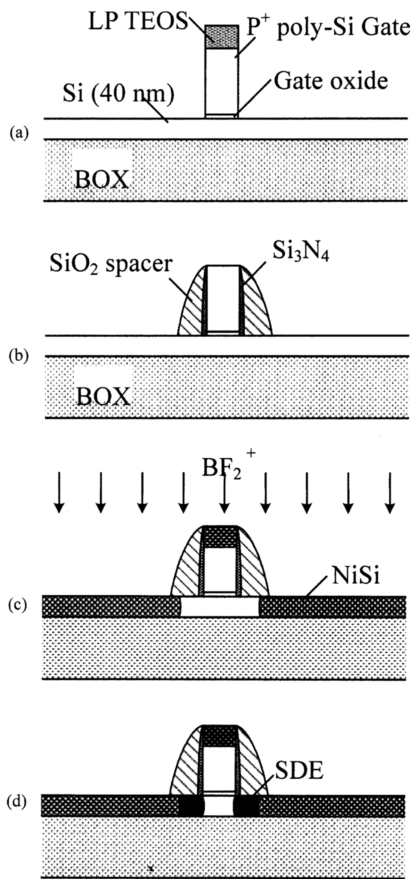

Fig. 1. Main process flow of the modified Schottky barrier FinFET.

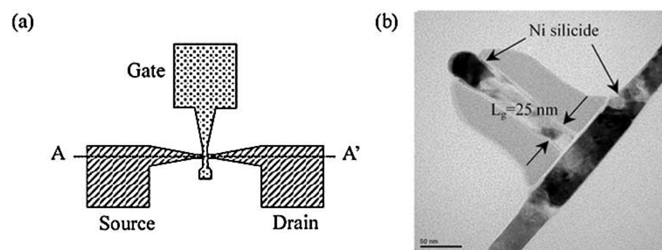

Fig. 2. (a) Schematically layout and (b) TEM micrograph of the MSB FinFET with $L_g = 25$ nm, $W_f = 40$ nm and $T_{\rm si} = 40$ nm.

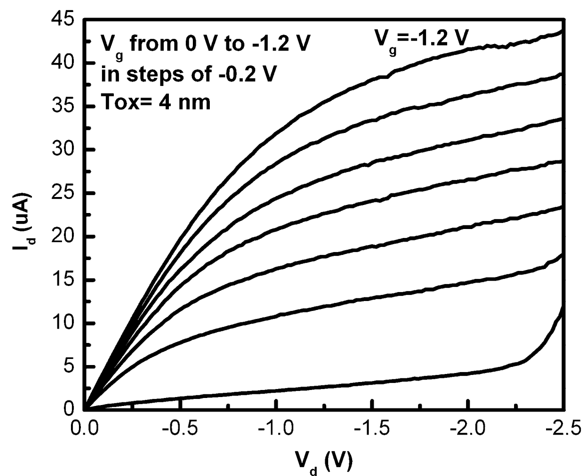

Fig. 3. Output characteristic of the MSB FinFET with $L_g = 25$ nm, $W_f = 40$ nm and $T_{\rm si} = 40$ nm.

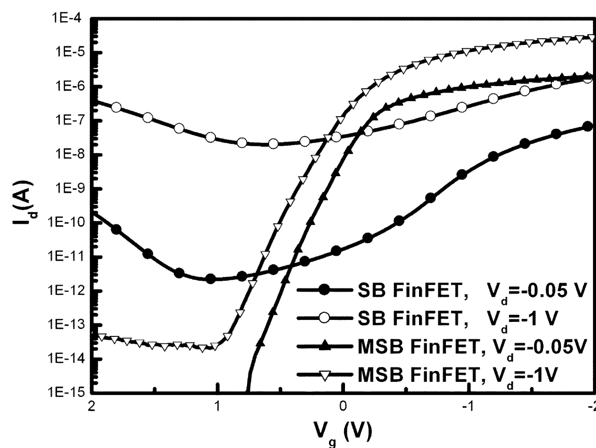

Fig. 4. Subthreshold characteristics of MSB and SB FinFETs with $L_g = 25$ nm, $W_f = 40$ nm and $T_{\rm si} = 40$ nm.

Si layer directly, the junction would be free of crystalline defects and low junction leakage current could be expected [12]. Typical inter layer dielectric deposition, contact hole patterning, and Al metallization completed the fabrication process. For comparison, simple SB FinFETs were fabricated with the same process but neglecting the ITS process step.

Fig. 2 shows the schematically layout and transmission electron microscopy (TEM) micrograph of the MSB FinFET in the A-A' direction with gate length (L_g) of 25 nm, fin thickness (W_f) of 40 nm, and fin height $(T_{\rm si})$ of 40 nm. The fin thickness (W_f) represents the fin width perpendicular to A-A' in Fig. 2(a). Fully silicided S/D and free crystalline defects are confirmed.

III. Results and Discussion

Fig. 3 shows the output characteristic of the MSB FinFET with $L_g = 25$ nm, fin thickness $(W_f) = 40$ nm, and fin height $(T_{\rm si}) = 40$ nm. It is known that for conventional SB devices,"sublinear"phenomenon is pronounced at linear region due to the Schottky barrier and the channel-S/D offset. For our SB FinFET, the large offset should be the dominant mechanism although the effect of Schottky barrier cannot be ignored. For the MSB FinFET, the ultrashort SDE bridges channel and S/D silicide. Furthermore, the Schottky barrier thickness, i.e., the carrier injection resistance from source to channel, is reduced by the high concentration ultrashort SDE. Therefore, the sublinear phenomenon is not observed. The driving current of the 25 nm MSB FinFET at $V_d = -1$ V is about 250 μA/μm under the definition of channel width $= 2 * H_{\rm Si} + W_f$ or 750 uA/um under the definition of channel width $= W_f$. It should be noted that the $I_{\rm on}$ could be further improved by shorter spacer length and thinner gate-oxide thickness.

Fig. 4 compares the transfer characteristics of the MSB FinFET and the SB FinFET. In the case of SB FinFET, a typical ambipolar operation is observed. For p-channel operation, the SB FinFET has poor subthreshold swing and $I_{\rm on}/I_{\rm off}$ current ratio of lower than 10^3. The small $I_{\rm on}/I_{\rm off}$ current ratio is attributed to the high Schottky barrier at on-state and low Schottky barrier at off-state. By inserting a ultrashort SDE to

modify the Schottky barrier property, the MSB FinFET can be turned on more steeply and had extremely high $I_{\rm on}/I_{\rm off}$ current ratio ($>10^9$). The 25-nm MSB FinFET also shows superior subthreshold characteristics with swing of 83 mV/dec and drain-induced barrier lowering (DIBL) of 235 mV/V. The low $V_{\rm th}$ (-61 mV) comes from the $\rm p^+$ poly gate; it could be adjusted using a mid-gap gate material such as $\rm p^+$ SiGe or Ta–Pt alloy, etc [13], [14]. For thinner gate oxide and smaller fin height/channel length ratio, better short channel characteristics could be expected [8]. In fact, subthreshold swing of 64.5 mV/dec and DIBL of 39 mV/V are obtained at $L_g = 49$nm. These results are better than those reported conventional FinFETs and SB FinFETs.

IV. Conclusion

High-performance MSB FinFETs with several unique features such as fully silicided S/D, ultrashort SDE, defect-free S/D junction, and low-temperature process is proposed. This device exhibits better current–voltage characteristics than those of published SB devices and FinFETs. With 4-nm-thick gate oxide, the $I_{\rm on}/I_{\rm off}$ current ratio higher than 10^9 is achieved. The subthreshold swing of 25 and 49 nm MSB FinFETs is 83 and 64.5 mV/dec at room temperature, respectively. These values are close to the theoretical limitation. The $I_{\rm on}$ of the 25-nm MSB FinFET is higher than 250 or 750 μA/μm, which depends on the definition of channel width. It is expected that the device characteristics can be further improved by thinner gate-oxide thickness and shorter spacer length.

The low-temperature process of MSB FinFET is an important advantage. Beyond 65-nm technology node, it is predicted that metal gate and high dielectric constant gate dielectric, must be employed to improved device performance continuously. Thermal stability between metal gate and a high-κ dielectric is a critical issue because the conventional S/D process acquires a high temperature annealing at least 900°. On the contrary, the process temperature of MSB process is around 600 °C. The thermal stability issue is relaxed and the interfacial layer formation at high-κ dielectric and Si interface is also reduced. Furthermore, the ultrashort SDE also helps device scale down.

Acknowledgment

The authors would like to thank the National Nano Device Laboratory staff for their support in device fabrication.

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